HP 37717C
Communications Performance Analyzer

Service Manual

SERIAL NUMBERS

This manual applies directly to modules with serial numbers GB000.

For additional information about serial numbers, see Instruments Covered By Manual in Chapter 1, page 1-8.

HP Part No. 37717-90432

Printed in UK, July 1999

Warranty

This Hewlett-Packard product is warranted against defects in materials and workmanship for a period of three years from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from:

1. Improper or inadequate maintenance, adjustment, calibration, or operation by Buyer;
2. Buyer-supplied software, hardware, interfacing or consumables;
3. Unauthorized modification or misuse;
4. Operation outside of the environmental and electrical specifications for the product;
5. Improper site preparation and maintenance; or
6. Customer induced contamination or leaks.

THE WARANTY SET FORTH IS EXCLUSIVE AND NO OTHER WARRANTY, WHETHER WRITTEN OR ORAL, IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Limitation of Remedies and Liability

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. IN NO EVENT SHALL HP BE LIABLE FOR DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES (INCLUDING LOSS OF PROFITS) WHETHER BASED ON CONTRACT, TORT OR ANY OTHER LEGAL THEORY.

Responsibilities of the Customer

The customer shall provide:

1. Access to the products during the specified periods of coverage to perform maintenance.
2. Adequate working space around the products for servicing by Hewlett-Packard personnel.
3. Access to and use of all information and facilities determined necessary by Hewlett-Packard to service and/or maintain the products. (Insofar as these items may contain proprietary or classified information, the customer shall assume full responsibility for safeguarding and protection from wrongful use.)
4. Routine operator maintenance and cleaning as specified in the Hewlett-Packard Operating and Service Manuals.
5. Consumables such as paper, disks, magnetic tapes, ribbons, inks, pens, gases, solvents, columns, syringes, lamps, septa, needles, filters, frits, fuses, seals, detector flow cell windows, etc.

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility and to the calibration facilities of other International Standards Organization members!

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

Notice

The information contained in this document is subject to change without notice.

Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance or use of this material.

Restricted Rights Legend

Use, duplication, or disclosure by the government is subject to restrictions as set forth in subdivision (b)(3)(ii) of the Rights in Technical Data and Computer Software clause at 52.227-7013. Hewlett-Packard Company; 3000 Hanover Street; Palo Alto, California 94304.

Statement of Compliance

This instrument has been designed and tested in accordance with IEC Publication 1010-1 + A1:1992 Safety requirements for Electrical Equipment for Measurement, Control and Laboratory Use, and has been supplied in a safe condition. The instruction documentation contains information and warnings which must be followed by the user to ensure safe operation and to maintain the instrument in a safe condition.

Electromagnetic Compatibility (EMC) Information

This product has been designed to meet the protection requirements of the European Communities Electromagnetic Compatibility (EMC) directive 89/336/EEC. In order to preserve the EMC performance of the product, any cable which becomes worn or damaged must be replaced with the same type and specification.

Safety Information

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

General

This is a Safety Class I instrument (provided with terminal for protective earthing) and has been manufactured and tested according to international safety standards.

DO NOT operate the product in an explosive atmosphere or in the presence of flammable gasses or fumes.

DO NOT use repaired fuses or short-circuited fuseholders: For continued protection against fire, replace the line fuse(s) only with fuse(s) of the same voltage and current rating and type.

DO NOT perform procedures involving cover or shield removal unless you are qualified to do so: Operating personnel must not remove equipment covers or shields. Procedures involving the removal of covers and shields are for use by service-trained personnel only.

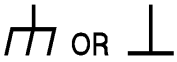
DO NOT service or adjust alone: Under certain conditions, dangerous voltages may exist even with the equipment switched off. To avoid dangerous electrical shock, service personnel must not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT operate damaged equipment: Whenever it is possible that the safety protection features built into this product have been impaired, either through physical damage, excessive moisture, or any other reason, REMOVE POWER and do not use the product until safe operation can be verified by service-trained personnel. If necessary, return the product to a Hewlett-Packard Sales and Service Office for service and repair to ensure the safety features are maintained.

DO NOT substitute parts or modify equipment: Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to a Hewlett-Packard Sales and Service Office for service and repair to ensure the safety features are maintained.

Safety Symbols

The following symbols on the instrument and in the manual indicate precautions which must be taken to maintain safe operation of the instrument.

Safety Symbols	
	The Instruction Documentation Symbol. The product is marked with this symbol when it is necessary for the user to refer to the instructions in the supplied documentation.
	Indicates the field wiring terminal that must be connected to earth ground before operating the equipment - protects against electrical shock in case of fault.
	Frame or chassis ground terminal - typically connects to the equipment's metal frame.
	Alternating current (AC)
	Direct current (DC)
	Indicates hazardous voltages
WARNING	Warning denotes a hazard. It calls attention to a procedure, which if not correctly performed or adhered to could result in injury or loss of life. Do not proceed beyond a warning note until the indicated conditions are fully understood and met.
CAUTION	Caution denotes a hazard. It calls attention to a procedure, which if not correctly performed or adhered to could result in damage to or destruction of the instrument. Do not proceed beyond a warning note until the indicated conditions are fully understood and met.
	The CE mark shows that the product complies with all relevant European legal Directives accompanied by a year, it's when the design was proven).
ISM 1-A	This is a symbol of an Industrial Scientific and Medical Group 1 Class A product.
	The CSA mark is a registered trademark of the Canadian Standards Association.
	Indicates that a laser is fitted. The user must refer to the manual for specific Warning or Caution information to avoid personal injury or damage to the product.

Laser Safety

To avoid hazardous exposure to laser radiation, it is recommended that the following practices are observed during system operation:

- **ALWAYS DEACTIVATE THE LASER BEFORE CONNECTING OR DISCONNECTING OPTICAL CABLES.**
- When connecting or disconnecting optical cables between the module and device-under-test, observe the connection sequences given below:

  Connecting: Connect the optical cable to the input of the device-under-test **before** connecting to the module's *Optical Out* connector.

  Disconnecting: Disconnect the optical cable from the module's *Optical Out* connector **before** disconnecting from the device-under-test. Always ensure the shutter (if fitted) closes properly and covers the laser aperture.

- NEVER examine or stare into the open end of a broken, severed, or disconnected optical cable when it is connected to the module's *Optical Out* connector.
- Arrange for service-trained personnel, who are aware of the hazards involved, to repair optical cables.

CAUTION

1. Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

2. Always leave the fibreoptic connector dust caps on each connector when not in use. Before connection is made, *always* clean the connector ferrule tip with acetone or alcohol and a cotton swab. Dry the connector with compressed air. Failure to maintain cleanliness of connectors is liable to cause excessive insertion loss.

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General Information

This section contains general information concerning the HP 37717C Communications Performance Analyzer.

Safety Considerations

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Options

Accessories

Safety Considerations

The HP 37717C Communications Performance Analyzer is a Safety Class 1 (IEC) product (provided with a protective earthling ground incorporated in the power cord).

This instrument has been designed and tested in accordance with IEC Publication 1010-1 (1990) with Amendment 1 (1992), Safety Requirements for Electronic Measuring Apparatus, and has been supplied in a safe condition. The instruction documentation contains information and warnings which must be followed by the user to ensure safe operation and to maintain the instrument in a safe condition.

Manual Safety Markings

WARNING **THE WARNING SIGN DENOTES A HAZARD TO THE OPERATOR. IT CALLS ATTENTION TO A PROCEDURE, PRACTICE, OR THE LIKE, WHICH IF NOT CORRECTLY PERFORMED OR ADHERED TO, COULD RESULT IN INJURY OR LOSS OF LIFE. DO NOT PROCEED BEYOND A WARNING SIGN UNTIL THE INDICATED CONDITIONS ARE FULLY UNDERSTOOD AND MET.**

CAUTION The CAUTION sign denotes a hazard to the instrument. It calls attention to an operating or maintenance procedure, practice, or the like, which if not correctly performed or adhered to, could result in damage to or destruction of part or all of the instrument. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

Instrument Safety Markings

Refer To Manual: This symbol on the instrument means the user must refer to the Calibration and Service Manuals to protect the instrument from damage.

Laser Warning Label - Hazard Symbol

WARNING **NO OPERATOR SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED PERSONNEL. TO PREVENT ELECTRICAL SHOCK DO NOT REMOVE COVERS.**

Laser Safety

WARNING **To prevent personal injury, avoid use which may be hazardous to others, and maintain the module in a safe condition, ensure the information given below is reviewed before operating the module.**

Laser Product Classification

All Options UH1, UH2, URU, USN and UKT, 130, 131 are classified as Class I (non-hazardous) laser product in the USA which complies with the United States Food and Drug Administration (FDA) Standard 21 CFR Ch.1 1040.10. Options UH1, UH2 and UKT are classified as Class 1 (non-hazardous) laser products in Europe which complies with EN 60825-1 (1994).
Options URU and USN are classified as a Class 3A laser product in Europe, which complies with EN 60825-1 (1994).
Laser classification is based on the ability of the optical beam to cause biological damage to the eye or skin. The EN 60825-1 (1994) definition of Class 3A is:

"Any laser product which permits human access to laser radiation in excess of the accessible emission limits of Class I and Class 2 as applicable, but which does not permit human access to laser radiation in excess of the accessible emissions of Class 3A and Class 3B (respectively) for any emission duration and wavelength."

Options URU and USN fall into this category, under the EN 60825-1 (1994) (European) standard, because they have a maximum output power of 19.5 me (under fault conditions), with a wavelength of 1550 nm.

To avoid hazardous exposure to laser radiation, it is recommended that the following practices are observed during system operation:

- **ALWAYS DEACTIVATE THE LASER BEFORE CONNECTING OR DISCONNECTING OPTICAL CABLES.**
- When connecting or disconnecting optical cables between the module and device-under-test, observe the connection sequences given below.

Connecting: Connect the optical cable to the input of the device-under-test **before** connecting to the module's *Optical Out* connector.

Disconnecting: Disconnect the optical cable from the module's *Optical Out* connector **before** disconnecting from the device-under-test. Always ensure the shutter closes properly and covers the laser aperture.

- NEVER examine or stare into the open end of a broken, severed, or disconnected optical cable when it is connected to the module's *Optical Out* connector.
- Arrange for service-trained personnel, who are aware of the hazards involved, to repair optical cables.

CAUTION Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Laser Warning Symbols

Options UH1, UH2 and UKT optical module's front panel contains the following label:

CLASS 1 LASER PRODUCT

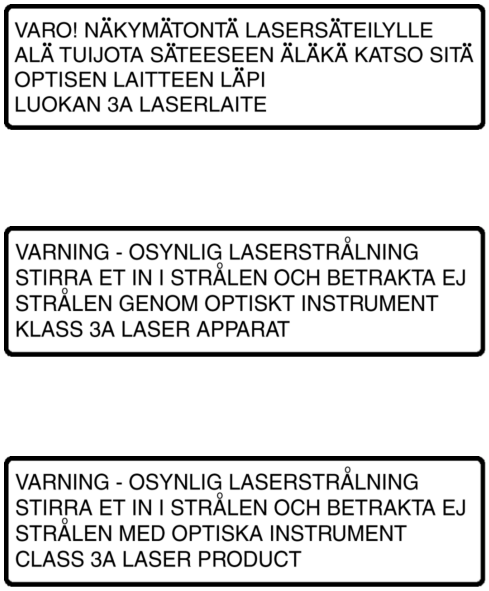
This label indicates that the radiant energy present in this instrument is non-hazardous.

Option USN optical module's front panel contains the following labels:

CLASS 3A LASER PRODUCT

CLASS 3A: Lasers which are safe for viewing with the unaided eye. For laser emitting in the wavelength range from 400 nm to 700 nm, protection is afforded by aversion responses including the blink reflex. For other wavelengths the hazard to the unaided eye is no greater than for Class I. Direct antiurban viewing of Class 3A lasers with optical aids (e.g. binoculars, telescopes, microscopes) may be hazardous.

Swedish and Finnish Labels



Location of Laser Apertures

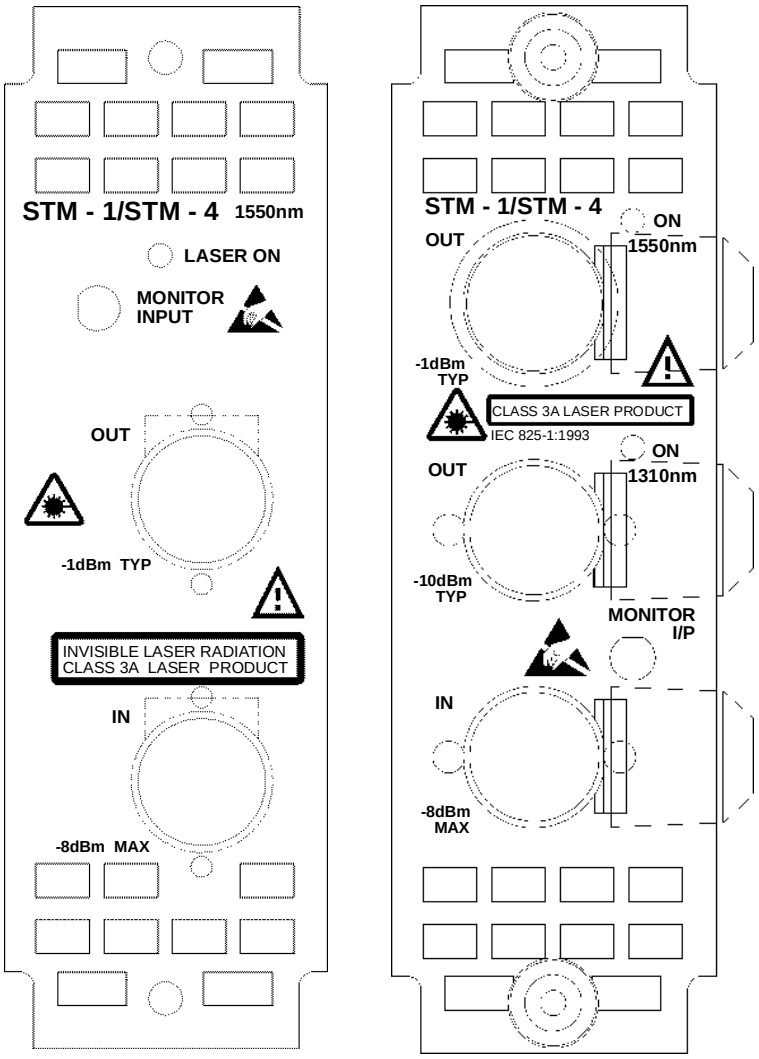


Figure 1-1 **Option 131** **Option USN**

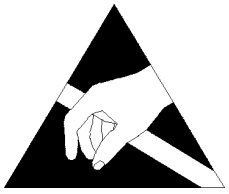
ESD Precautions

CAUTION The module contains components sensitive to electrostatic discharge. To prevent component damage, carefully follow the handling precautions presented below.

The smallest static voltage most people can feel is about 3500 volts. It takes less than one tenth of that (about 300 volts) to destroy or severely damage static sensitive circuits. Often, static damage does not immediately cause a malfunction but significantly reduces the component's life. Adhering to the following precautions will reduce the risk of static discharge damage.

- Keep the module in its conductive storage box when not installed in the Mainframe. Save the box for future storage of the module.
- Before handling the module, select a work area where potential static sources are minimized. Avoid working in carpeted areas and non-conductive chairs. Keep body movement to a minimum. Hewlett-Packard recommends that you use a controlled static workstation.
- Handle the module by its front-panel. Avoid touching any components or edge connectors. When you install the module, keep one hand in contact with the protective bag as you pick up the module with your other hand. Then, before installing the module, make contact with the metal surface of the Mainframe with your free hand to bring you, the module, and the mainframe to the same static potential. **This also applies whenever you connect/disconnect cables on the front-panel.**

CAUTION The connectors on the front-panel of the module remain susceptible to ESD damage while the module is installed in the Mainframe, as indicated by the label:



Electromagnetic Compatibility

Radiated Emissions

To ensure compliance with EN 55011 (1991) a category 5, FTP patch lead, RJ45 cable should be used to connect the LAN port on the processor module marked "10 Base-T".

Electrostatic Discharge

When air discharges, according to IEC801-2 (1991), of up to 8 kV are applied to specific areas of the product occasional errors may be counted.

Operators Maintenance

WARNING **NO OPERATOR SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED PERSONNEL. TO PREVENT ELECTRICAL SHOCK DO NOT REMOVE COVERS.**

Cleaning

Clean the cabinet using a dry cloth only.

Optical Fibre Cleaning

It is recommended that the optical connectors be cleaned at regular intervals using the following materials:

Description	HP Part Number
Blow Brush	**9300-1131**
Isopropyl Alcohol	**8500-5344**
Lens Cleaning Paper	**9300-0761**
Adhesive Tape Kit	**15475-68701**

CAUTION Do not insert any tool or object into the IN or OUT ports of the instrument as damage to or contamination of the optical fibre may result.

1. Recall Default settings (STORED SETTINGS 0) and remove the power from the HP 37717C.

2. Remove the adapters from the IN and OUT ports.

3. Using the blow brush with the brush removed blow through the ferrule of the standard flexible connector and the adapter.

CAUTION If the optical fibre of the fixed connector requires further cleaning this entails disassembly of the module which should only be carried out by suitably trained service personnel.

4. Apply some isopropyl alcohol to a piece of the cleaning paper and clean the barrel of the adapter. Using a new piece of cleaning paper, clean the face of the adapter. Repeat this operation, using a new piece of cleaning paper each time.

5. Lightly press the adhesive side of the tape provided against the front of the adapter, then remove it quickly - repeat twice. This removes any particles of cleaning paper which may be present.

6. Replace the adapters on the flexible connector.

Instruments Covered By Manual

Attached to the rear panel of the instrument is a serial number plate. The serial number plate has a two letter reference denoting country of origin (GB = Great Britain) and an eight digit serial number. The serial number is unique to each instrument and should be quoted in all correspondence with Hewlett-Packard, especially when ordering replacement parts.

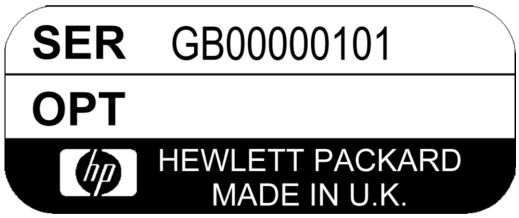


Figure 1-2 Serial Number Plate

Table 1-1 Recommended Test Equipment

Instrument	Critical Specification	Recommended Model
Oscilloscope	400 MHz Bandwidth, 1 MΩ Input Termination, Telecom mask meas function	HP 54520A Opt 001 or HP 54810A Opt 001
Spectrum Analyzer	200 MHz Bandwidth, 75Ω Input, -70 to +20 dBm	HP 8568B Opt 001
Frequency Synthesizer	75Ω Output, Sinewave to 80 MHz, Amplitude to 2.5 V pk-pk, 1 Hz resolution	HP 3335A Opt 001
Frequency Synthesizer	Sinewave to 2.5 MHz, Amplitude to 5 V pk-pk, 1 Hz Resolution	HP 3325B (Qty 2)
Signal Generator	Sinewave 700 kHz to 170 MHz, Amplitude 500 mV	HP 8657B
Frequency Counter	Range 0 to 200 MHz, 2 channels with accuracy <0.1 ppm. (Ratio Mode)	HP 5335A Opt 010
Optical Power Meter and Sensor Module	Range -8 dBm to -15 dBm, Wavelength 1270-1340 nm	HP 8153A and HP 81536A
Power Supply	Multi-Output System 0-50 V, 0-500 mA, 25 watts o/p	HP 6621A
Lightwave Convertor	Wavelength 1200 - 1600 nm and Bandwidth from dc. 15 GHz Optical	HP 11982A
Optical Attenuator	Wavelength 1200 - 1600 nm, Range 0 - 30 dB	HP 8157A
FC/PC Optical Interface Connector	Unique	HP 81000FI
Optical Cables	Unique	HP 11871A (Qty 2)
PDH Structured Test Set or Digital Transmission Frame Generator	Unique	HP 37717C Opt UKJ or HP 37729A
Jitter Measurement Module	Unique	HP 37717C Opt UHN or any Jitter Rx
Attenuator	6 dB, 50Ω, 0 to 200 MHz	HP 8491A Opt 006
Attenuator	3 dB, 50Ω, 0 to 200 MHz	HP 8491A Opt 003
Cable Simulator #1	80 metres of 75Ω coaxial cable	8120-0049 (80 m)
Cable Simulator #2	60 metres of 75Ω coaxial cable	8120-0049 (60 m)
Cable Simulator #3	70 metres of 75Ω coaxial cable	8120-0049 (70 m)
Cable Simulator #4	30 metres of 75Ω coaxial cable	8120-0049 (30 m)
Converter	75Ω Unbalanced to 120Ω Balanced	HP 15508C

Table 1-1 Recommended Test Equipment, continued

Instrument	Critical Specification	Recommended Model
ECL Termination	Unique	HP 10086A
Blocking Capacitor	0.18 µf	HP 10240A
Cable Attenuator	Unique	HP 8120-0039 (70 m)
75Ω/50Ω Matching Pad	Insertion Loss 5.7 dB	HP 11852B (Qty 2)
75Ω Termination	0 to 200 MHz	HP 15522-80010
T Connector	BNC to Dual BNC	HP 1250-0781
Adaptor	N Type (f) to BNC (m)	1250-1534 (Qty 2)
Adaptor	N Type (m) to N Type (m)	1250-1475 (Qty 2)
Adaptor	SMA to BNC	1250-1787 (Qty 2)
RS-232-C Loopback	Unique	5060-4462
Oscilloscope Pod	10kΩ	HP 54001A

2

Installation

This section contains information and instructions required to prepare the HP 37717C Communications Performance Analyzer for use. Included in this section are the initial inspection procedures, power and grounding requirements, fuse selection procedure, installation information, operators maintenance and instructions on repackaging for shipment.

Initial Inspection

Preparation for Use

Operators Maintenance

Hewlett-Packard Interface Bus

Operating Environment

Storage and Shipment

Initial Inspection

WARNING **TO AVOID HAZARDOUS ELECTRICAL SHOCK, DO NOT PERFORM ELECTRICAL TESTS WHEN THERE ARE SIGNS OF SHIPPING DAMAGE TO ANY PORTION OF THE OUTER ENCLOSURE (COVERS, PANELS, METERS).**

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked both mechanically and electrically. Procedures for checking electrical operation are given in The Calibration Manual. If the contents of the shipment are incomplete, if there is mechanical damage or defect, notify the nearest Hewlett-Packard Office. If the instrument does not pass the electrical performance tests given in the Calibration Manual, notify the nearest Hewlett-Packard office. If the shipping container is also damaged, or the cushioning material shows signs of stress, notify the carrier as well as the nearest Hewlett-Packard office. Keep the shipping materials for the carrier's inspection. The Hewlett-Packard office will arrange for repair or replacement without waiting for claim settlement.

Preparation for Use

WARNING **IF THIS INSTRUMENT IS NOT USED AS SPECIFIED, THE PROTECTION PROVIDED BY THE EQUIPMENT COULD BE IMPAIRED. THIS INSTRUMENT MUST BE USED IN A NORMAL CONDITION (IN WHICH ALL MEANS OF PROTECTION ARE INTACT) ONLY.**

WARNING **FOR CONTINUED PROTECTION AGAINST FIRE HAZARD REPLACE FUSE ONLY WITH SAME TYPE AND RATINGS (SEE TABLE 2-1).**

Power Requirements

The HP 37717C Communications Performance Analyzer requires a power source of 90 V to 132 V ac and 198 V to 264 V ac at a frequency between 47 Hz and 63 Hz (nominal).

Total power consumption is 450 VA (maximum).

The fuse rating for the power source is given in Table .

Table 2-1 Fuses

Line Voltage	Fuse Rating	HP Part Number
90V to 264V	5A Timed, 250V	2110-1120

Power Cord

The power cord supplied with each instrument varies with the country of destination. Figure 2-1 illustrates the standard power plug and cord configurations that are commonly used. The part number shown beneath each plug is the part number of the appropriate power cord and plug. If the appropriate power cord is not included with the instrument notify the nearest Hewlett-Packard office and a replacement will be provided.

WARNING **TO AVOID THE POSSIBILITY OF INJURY OR DEATH, THE FOLLOWING PRECAUTIONS MUST BE FOLLOWED BEFORE THE INSTRUMENT IS SWITCHED ON:**

(a) Note that the protection provided by grounding the instrument cabinet may be lost if any power cable other than the three-pronged type is used to couple the ac line voltage to the instrument.

(b) If this instrument is to be energized via an auto-transformer to reduce or increase the line voltage, make sure that the common terminal is connected to the neutral pole of the power source.

(c) The power cable plug shall only be inserted into a socket outlet provided with a protective ground contact. The protective action must not be negated by the use of an extension cord without a protective conductor (grounding).

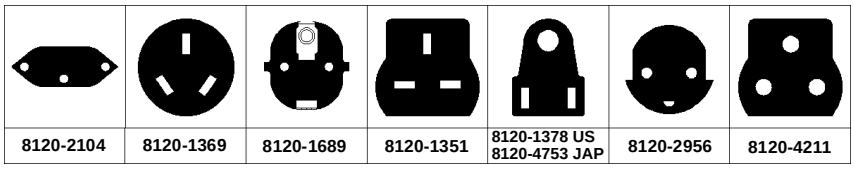


Figure 2-1 Power Cord Part Numbers

Operators Maintenance

Fuse Replacement

Only the ac line fuse located at the side of the instrument may be replaced by the operator.

WARNING

ALL OTHER FUSE REPLACEMENT SHOULD ONLY BE CARRIED OUT BY SUITABLY TRAINED SERVICE PERSONNEL AWARE OF THE HAZARDS INVOLVED.

BEFORE REMOVING THE FUSE, THE AC LINE POWER CORD SHOULD BE DISCONNECTED FROM THE POWER SOURCE AND THE OTHER END DISCONNECTED FROM THE INSTRUMENT.

ONLY USE A FUSE OF THE CORRECT RATING AS LISTED IN TABLE 2-1.

Use a small flat bladed tool to remove the fuse holder from the Power Supply Line Filter Assembly (located between the Power ON /OFF switch and the Power Input connector. The cap and the fuse can then be removed and the fuse changed for another of the correct rating. The fuse rating and HP part number are listed in Table 2-1.

Line Voltage Selector Switch

The Line Voltage Selector switch has 2 positions:

100 - 120 V
200 - 240 V

CAUTION

Before switching on this instrument, make sure that the line voltage selector switch is set to the voltage of the power supply. Ensure the supply voltage is in the specified range.

Hewlett-Packard Interface Bus

The HP 37717C (Option A3B or A3D) is connected to the HP-IB by means of an appropriate HP-IB cable. The HP-IB interconnecting cables available are listed in Table 2-2.

Table 2-2 HP-IB Interconnecting Cables

Length	Accessory Number
1 meter	HP 10833A
2 meters	HP 10833B
4 meters	HP 10833C
0.5 meter	HP 10833D

To achieve interface design performance standards, restrictions are placed on the HP-IB system cable lengths. These restrictions allow the bus interface electronics to maintain correct line voltage levels and timing relationships.

When connecting an HP-IB system the following rules should be observed:

The total HP-IB cable length used must be less than or equal to 20 meters (65.6 feet).

The total HP-IB cable length used must be less than or equal to 2 meters (6 feet) × the total number of devices connected to the bus.

A standard HP-IB connector is provided on the instrument CPU front panel. The connections and HP-IB logic levels are shown in Figure 2-2. The mating connector part number is HP 1251-0293 or Amphenol 57-30240.

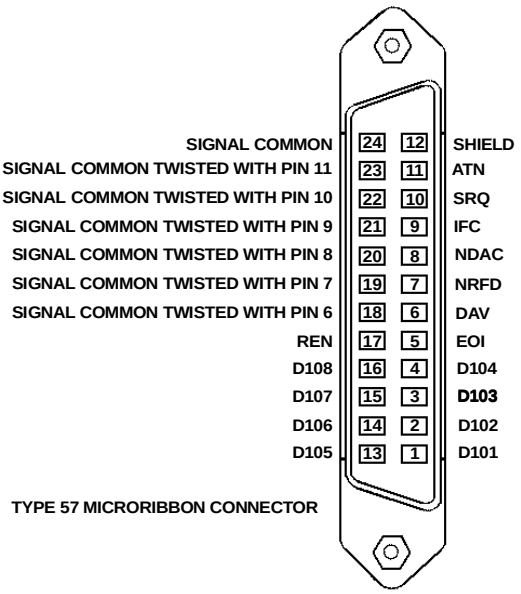


Figure 2-2 HP-IB Connections and Logic Levels

HP-IB Address Selection

The HP 37717C (Option A3B or A3D) HP-IB address is accessed on the OTHER display under the COMMS CONTROL function.

The address can be set to any value between 0 and 30 inclusive using ⇦ ⇨ and the display softkeys.

Operating Environment

The instrument may be operated in temperatures within the range 0 degrees to +45 degrees centigrade at altitudes up to 3,050 meters (10,000 feet). At all times the instrument should be protected from temperature extremes and environments which could cause condensation within the instrument.

CAUTION VENTILATION REQUIREMENTS: When installing the instrument in a cabinet, the convection into and out of the instrument must not be restricted. The ambient temperature (outside the cabinet) must be less than the maximum operating temperature of the instrument by 4^0C for every 100 watts dissipated in the cabinet. If the total power dissipated in the cabinet is greater than 800 watts, then forced convection must be used.

Storage and Shipment

The instrument may be stored or shipped in environments within the following limits:

Temperature. -40^o C to $+65^o$ C

Altitude. Up to 15,200 meters (50,000 feet)

The instrument should also be protected from temperature extremes which could cause condensation within the instrument.

Repackaging for Shipment

Tagging for Service. If the instrument is being returned to Hewlett- Packard for service, please complete a repair tag and attach it to the instrument.

Original Packaging. Containers and materials identical to those used in factory packaging are available from Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

Other Packaging. The following general instructions should be followed when repackaging with commercially available materials:

Wrap instrument in heavy paper or plastic. If the instrument is being shipped to Hewlett-Packard, attach a tag indicating the type of service required, return address, model number and full serial number.

Use a strong shipping container. A double wall carton made of 350 pound test material is adequate.

Use a layer of shock absorbing material 70 to 100 mm (3 to 4 inch) thick, around all sides of the instrument to provide firm cushioning and prevent movement inside the container. Protect the Front Panel controls and Rear Panel connectors with cardboard.

Seal shipping container securely.

Mark shipping container FRAGILE to ensure careful handling.

In any correspondence, refer to instrument by model number and full serial number.

3

Adjustments

Introduction

This section contains the adjustment procedures required for the HP 37717C. These procedures will allow the instruments to be adjusted to meet the published specifications.

Safety Considerations

The HP 37717C is a Safety Class 1 (IEC) instruments. (This means that the instruments are provided with protective earth terminals.) This section contains warnings and cautions which must be followed for your protection and safety and to avoid damage to the instruments.

WARNING **MAINTENANCE DESCRIBED HEREIN IS PERFORMED WITH POWER SUPPLIED TO THE INSTRUMENT AND PROTECTIVE COVERS REMOVED. SUCH MAINTENANCE SHOULD ONLY BE PERFORMED BY SERVICE TRAINED PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED (e.g. FIRE AND ELECTRICAL SHOCK). WHERE MAINTENANCE CAN BE PERFORMED WITHOUT POWER APPLIED, THE POWER SHOULD BE REMOVED.**

Requirements for Adjustments

Before carrying out any adjustments, check the Time and Date logged for each of the Calibration item adjustments as follows:

1. Switch on the instrument then press the OTHER key.
2. Press the MORE softkey. select the CALIBRATION function.
3. Select Calibration password and set to [1243] using the INCREASE DIGIT and DECREASE DIGIT softkeys.
4. Select each Calibration item in turn and note the Time and Date of the last valid Calibration. If any of these are invalid or greater than 1 year, it is recommended that the soft adjustments associated with that item are carried out.

It is also recommended that adjustments be performed if a failure occurs in one or more of the Performance Tests. Performance Tests are provided in the HP 37717C Calibration manual. The Performance Test failure will usually indicate which parameter needs to be adjusted, but if in doubt, or if the adjustment does not bring the parameter within specification, refer to the Service Section in this Manual.

Adjustment Type

The HP 37717C contain two types of adjustments.

Hard Adjustment - this is done using an analog on-board component such as a variable resistor or capacitor.

Soft Adjustment - this may be automatic or semi-automatic. When the adjustment is completed calibration data is stored in a special Ram on the module or the CPU. The instrument will also log the Time and Date of the adjustment in the Calibration Menu.

List of Soft Adjustments

The following table provides a list of all "Soft" adjustments (stored in the memory) in the HP 37717C.

Adjustment Title	Page No	Where Required
10 MHz Reference Clock Frequency	3-8	All Units

NOTE The Internal Clock Time and Date must be set up before carrying out any "soft" adjustment (Refer to Operating Manual).

List of Adjustable Components

The following table provides a list of all adjustable components (hard adjustments) within the HP 37717C.

Table 3-1 Adjustable Components

Adjustable Component	Page No	Adjustment Title
A4R25	3-8	10 MHz Reference Clock Frequency & VCXO CAL Disk-Drive
UPDH Transmitter (Option UKK)		
A7R1	3-10	CMI Tx Pulse Amplitude
A7R2	3-10	CMI Tx Eye-Diagram Symmetry
A7R3	3-10	CMI Pulse Mark : Space Ratio
A7R4	3-10	Ternary Pulse Amplitude (positive)
A7R5	3-10	Ternary Pulse Amplitude (negative)
UPDH Receiver (Option UKK)		
A6R1	3-13	PDH 704 kHz Rx Recovered Clock
A6R2	3-13	PDH 2048 kHz Rx Recovered Clock
A6R3	3-13	PDH 8448 kHz Rx Recovered Clock

Table 3-1 Adjustable Components, continued

Adjustable Component	Page No	Adjustment Title
A6R4	3-13	PDH 34368 kHz Rx Recovered Clock
A6C154	3-13	PDH 139264 kHz Rx Recovered Clock
SDH Transmitter (Option A1T)		
A9R53	3-17	STM-1 All Zeros Pulse Mark:Space Ratio
A9R38	3-17	STM-1 All Ones Pulse Mark:Space Ratio
A9R22	3-17	STM-1 Tx Pulse Amplitude
SDH Receiver (Option A1T)		
A9C230	3-20	STM-1 Rx CMI Clock Recovery
SDH Standard Clock (Options A1T)		
A8C104	3-22	SDH Rx Offset Clock Recovery
STM-1 Optical Transmitter (Option UH1)		
A11R1	3-25	STM-1 Optics Modulation Depth
1310 nm STM1/4 Optical Transmitter (Options USN and UKT)		
A63R26	3-27	STM4 Optical Power Level
1550 nm STM1/4 Optical Transmitter USN		
A67R42	3-29	STM4 Optical Power Level
Jitter Transmitter (Option UHK)		
A12R136	3-31	34 MHz Duty Cycle
A12R135	3-31	140 MHz Duty Cycle
A12R2	3-31	DC Offset
A12R5	3-31	Residual Amplitude
A12R1	3-31	Control Loop Gain
Jitter Generator (Options A3K, 140)		
R69	3-40	2 MHz VCO Duty Cycle
R47	3-40	8 MHz VCO Duty Cycle
R40	3-40	34 MHz VCO Duty Cycle
R56	3-40	140 MHz VCO Duty Cycle
R53	3-40	Control Loop DC Offset
R39	3-40	Control Loop DC Offset
R21	3-40	Loop Gain
L2	3-40	2 MHz Ref Input Min. Jitter

Table 3-1 Adjustable Components, continued

Adjustable Component	Page No	Adjustment Title
Jitter Receiver (Option UHN)		
R2, R4	3-44	Measurement Loop Offset
R1	3-44	Jitter Hits Threshold Level
R68	3-44	Demod Jitter Output Amplitude
L21	3-44	Wander Reference Recovered Clock
Jitter Receiver (Options A3L, A3M)		
A18R159	3-50	Recovered Clock
A18L9	3-50	Wander Reference Recovered Clock
Jitter Receiver (Options A1M, A1N, A1P)		
R40	3-54	False Lock Set
R31	3-54	Jitter Hits Level
R3	3-54	Demod. Jitter Output
Jitter Receiver Setup (Options A3L, A3M, A3N, A3P, A3V, A3W)		
R157	3-61	Meas Loop Offset
R120	3-61	Meas Loop Offset
R73	3-61	Narrowband Det. Leakage
R54	3-61	Narrowband Det. Leakage
R2	3-61	Demod Jitter Output
R79	3-61	Main Lock Detect
SPDH Transmitter (Options UKJ and USA)		
A17R39	3-67	CMI Tx Pulse Amplitude
A17R47,55	3-67	CMI Tx Mark Space Ratio
A17R46	3-67	Ternary Pulse Amplitude (positive)
A17R54	3-67	Ternary Pulse Amplitude (negative)
SPDH Receiver (Options UKJ, USA)		
A16R30	3-71	2048 kHz Recovered Clock frequency
A16R38	3-71	8448 kHz Recovered Clock frequency
A16R46	3-71	34368 kHz Recovered Clock frequency
A16C154	3-71	139,264 kHz Recovered clock frequency
Multiple Outputs (Option UHC)		

Table 3-1 Adjustable Components, continued

Adjustable Component	Page No	Adjustment Title
A7R189	3-74	VCO Duty Cycle (Unstructured PDH Module fitted)
A17R38	3-74	VCO Duty Cycle (Structured PDH Module fitted)
A14R8	3-74	CMI Tx Pulse Amplitude (Output 2)
A14R10	3-74	CMI Tx Pulse Amplitude (Output 3)
A14R12	3-74	CMI Tx Pulse Amplitude (Output 4)
ATM Cell Layer Transmitter (Option UKZ)		
R44	3-77	Term Pulse Amplitude +ve
R50	3-77	Term Pulse Amplitude -ve
ATM Cell Layer Receiver (Option UKZ)		
R43	3-83	1.544 MHz Recovered Clock
R52	3-83	2 MHz Recovered Clock
R53	3-83	34 MHz Recovered Clock
R8	3-83	44 MHz Recovered Clock
Binary Interface (Option UH3)		
R3	3-88	-5.2 V Supply
STM Clock Setup (Option A3R)		
C38	3-94	Transmitter Minimum Jitter
C42	3-94	Receiver Minimum Jitter
SDH Setup (Option A3R)		
R39	3-101	Mark/Space Adjust

Warm-Up Time

To ensure adjustment accuracy, the equipment must be switched on for a minimum of 30 minutes before carrying out any adjustment.

Adjustment Sequence

The adjustments should be performed in the sequence given in Table above. The 10 MHz Reference Clock frequency adjustment and VCXO Calibration must always be performed first.

Access to Adjustable Components

To gain access to adjustable components, proceed as follows;

1. Switch off the instrument and disconnect the power cord and any interconnecting cables.
2. Place the instrument face down on the workbench.
3. Remove the 4 screws securing the rubber feet to the rear panel.
4. If Optical Modules are fitted unscrew the optical shield from the input and output connectors.
5. Withdraw the outer cabinet sleeve back, and out of the instrument.

Most adjustable components may now be accessed through the slots in the top or bottom of the instrument chassis. Where an Extender Card is required, this will be covered in the particular adjustment procedure. When all adjustments have been completed, re-assemble the instrument as a reversal of the above procedure.

Equipment Required

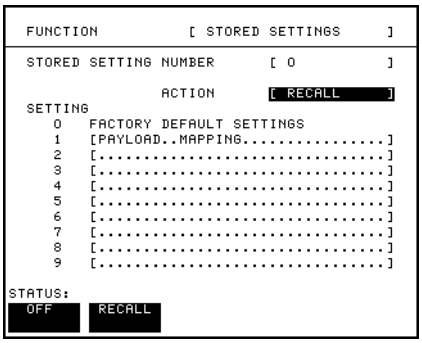
Equipment required to perform these adjustments is listed on page 1-9. Equipment required to make an individual adjustment is listed in the particular adjustment procedure. Any equipment which meets or exceeds the listed critical specification may be substituted.

Recall Default Settings

Some adjustments require the HP 37717C to be set to a pre-defined (default) state at the beginning of each test. The pre-defined default settings are listed in Appendix A.

1 Press OTHER; then use the ⇧ and ⇩ keys to select and set up the **STORED SETTINGS** as shown below.

.



2 Press **RECALL** to recall the instrument default settings.

The instrument display will blank for a few seconds while the settings are recalled and the status display will indicate stored settings number 0 recalled.

10 MHz Reference Clock Frequency and VCXO

Adjustment Reference

10 MHz Reference Clock Source	**A4R25**

Description

The 10 MHz Reference Clock Source is calibrated by connecting to a Frequency Counter and adjusting within limits.

The VCXO's are calibrated by running the instrument automatic calibration items.

Equipment Required

Frequency Counter	**HP 5335A Opt 001**
10:1 Oscilloscope Probe	**HP 10435A**

Procedure

10 MHz Reference Clock Frequency

1. Recall the HP 37717C Default settings with the following key sequence: OTHER, then select STORED SETTINGS , set STORED SETTING NUMBER to 0 and ACTION to RECALL.
2. Select the CALIBRATION function on the OTHER display.
3. Using ⇩, DECREASE DIGIT and ⇧, INCREASE DIGIT set the CALIBRATE PASSWORD to [1243].
4. Select CALIBRATION ITEM to 10 MHz REF and MODE to MANUAL.
5. Select Frequency A and 1 MΩ input impedance on the Frequency Counter.
6. Connect the Frequency Counter Input A, via the Oscilloscope probe, to TP15 on the A4 Processor Assembly. Ground the probe on TP13 (ground) on this assembly. These Test Points are accessible through a slot in the bottom of the instrument.
7. Adjust A4R25 to obtain a Counter reading of 10,000,000 Hz.
8. Select the MEASURED FREQUENCY field on the HP 37717C display and enter the counter frequency reading using ⇩, DECREASE DIGIT and ⇧, INCREASE DIGIT keys.
9. You must change the displayed frequency or the new Calibration Time and Date will not be entered in memory. The Time and Date must be correctly set up - see Operating Manual.

VCXO Calibration (PDH Options)

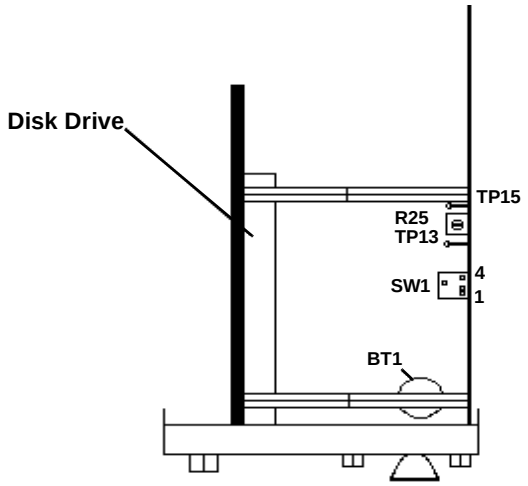


Figure 3-1 Processor Module (underside) Adjustable Components

10 Set the CALIBRATION to VCXOs and press RUN/STOP to start the calibration routine.

11 When Calibration is finished, the Calibration Time and Date will appear next to each VCXO on the display.

12 Disconnect all test equipment.

Unstructured PDH Transmitter (Option UKK)

A7 PDH Transmitter Assembly.

Adjustment Reference

CMI Tx Pulse Amplitude	**A7R1**
CMI Tx Eye-diagram Symmetry	**A7R2**
CMI Tx Mark:Space Ratio	**A7R3**
Ternary Pulse Amplitude (positive)	**A7R4**
Ternary Pulse Amplitude (negative)	**A7R5**

Description

An Oscilloscope is connected to the Data Output port and A7R1, R2 and R3 are adjusted to optimize the displayed CMI pulse Amplitude, Mark to Space Ratio and Eye-Diagram. The positive and negative ternary pulse amplitudes are also set using R4 and R5 on this assembly.

Equipment Required

Oscilloscope	**HP 54520A**
75/50Ω Matching Pad	**HP 11852B**

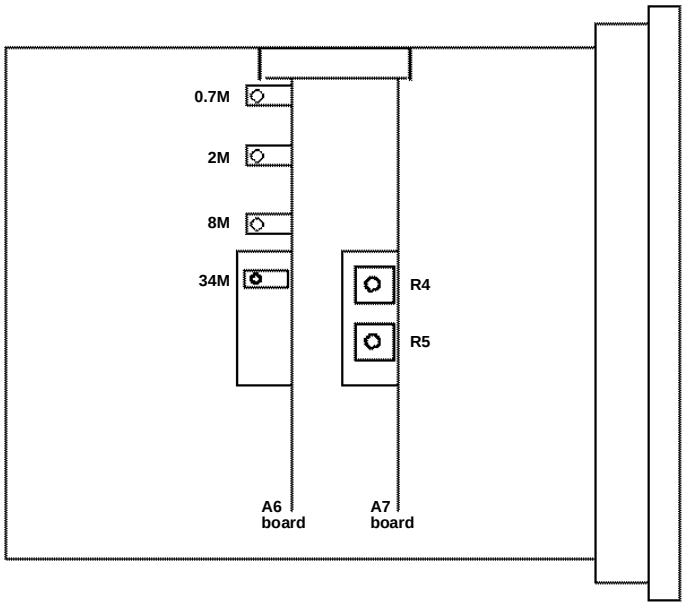


Figure 3-2 UPDH Module (topside) Adjustable Components

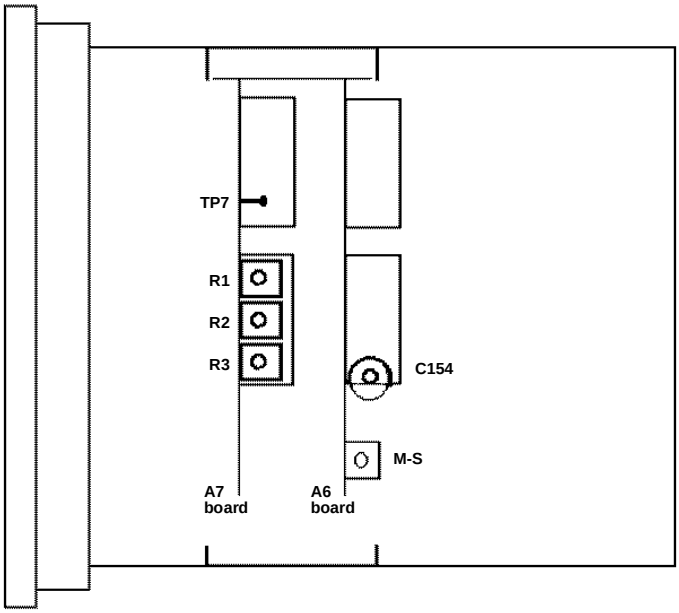


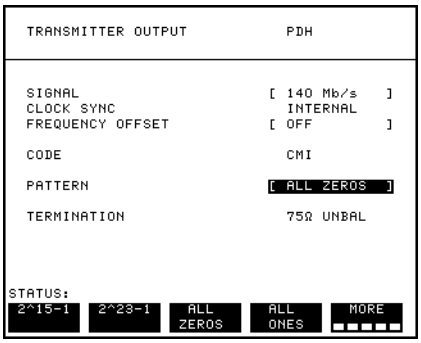
Figure 3-3 UPDH Module (underside) Adjustable Components

Procedure

CMI Pulse Amplitude

1 Recall the HP 37717C Default settings with the following key sequence:
Press OTHER, STORED SETTINGS Set the STORED SETTING NUMBER to 0 and set ACTION to RECALL.

2 Press TRANSMIT and setup the display as shown below.



3 Connect the HP 37717C Unbalanced 75Ω PDH OUT port to the Oscilloscope INPUT 1 via the 75/50Ω Matching Pad - set the Oscilloscope termination to 50Ω

4 Set the Oscilloscope Channel 1 Probe Attenuation factor to X 2.40 (equivalent to 7.6 dB) to compensate for the Matching Pad attenuation.

5 Press AUTOSCALE on the Oscilloscope and adjust the timebase and Delay to display a single CMI pulse.

6 Using the Oscilloscope, measure the peak amplitude of this pulse.

7 Adjust A7R1 to obtain a maximum pulse amplitude of 1 Volt pk-pk.

CMI Pulse Mark:Space Ratio

8 Using the Oscilloscope, measure the pulse Mark to Space Ratio.

9 Adjust A7R3 to obtain a Mark to Space Ratio of 1:1.

CMI Pulse Eye-Diagram

10 Select PATTERN [USER WORD] [1111111000000100].

11 Set the Oscilloscope Timebase to 200 ps/Div and adjust the Delay to display an Eye-Diagram as shown on the next page.

12 Adjust A7R2 to obtain a symmetrical trace above and below the Eye Diagram cross-over point.

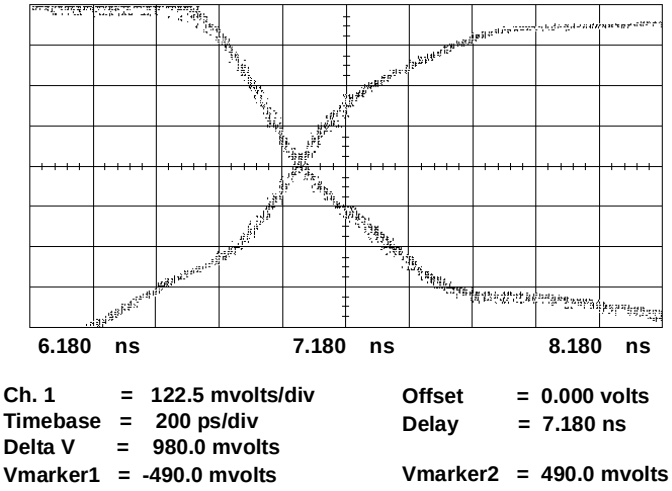


Figure 3-4 CMI Pulse Eye Diagram

Ternary Pulse Amplitude

13 Set the BIT RATE to 704 kb/s and PATTERN to ALL ONES on the HP 37717C.

14 Press AUTOSCALE on the Oscilloscope and adjust the Timebase and Delay to position the positive ternary pulse in the centre of the screen.

15 Using the Oscilloscope, measure the peak amplitude of this pulse.

16 Adjust A7R4 to obtain a maximum positive pulse amplitude of 2.37 Volts.

17 Adjust the Oscilloscope Timebase and Delay to position the negative ternary pulse in the centre of the screen.

18 Using the Oscilloscope, measure the peak amplitude of this pulse.

19 Adjust A7R5 to obtain a maximum negative pulse amplitude of 2.37 Volts.

Unstructured PDH Receiver (Option UKK)

A6 PDH Receiver Assembly.

Adjustment Reference

704 kHz Recovered Clock frequency	**A6R1**
2,048 kHz Recovered Clock frequency	**A6R2**
8,448 kHz Recovered Clock frequency	**A6R3**
34,368 kHz Recovered Clock frequency	**A6R4**
139,264 kHz Recovered Clock frequency	**A6C154**

Description

A frequency counter is used to measure the recovered clock frequency at all rates. The recovered clock frequency rates are then adjusted to be within specification.

Equipment Required

Extender Card	**HP 37714-60099**
Frequency Counter	**HP 5335A Option 010**
75 Ohm Termination	**HP 1522-80010**
T Connector	**HP 1250-0781**

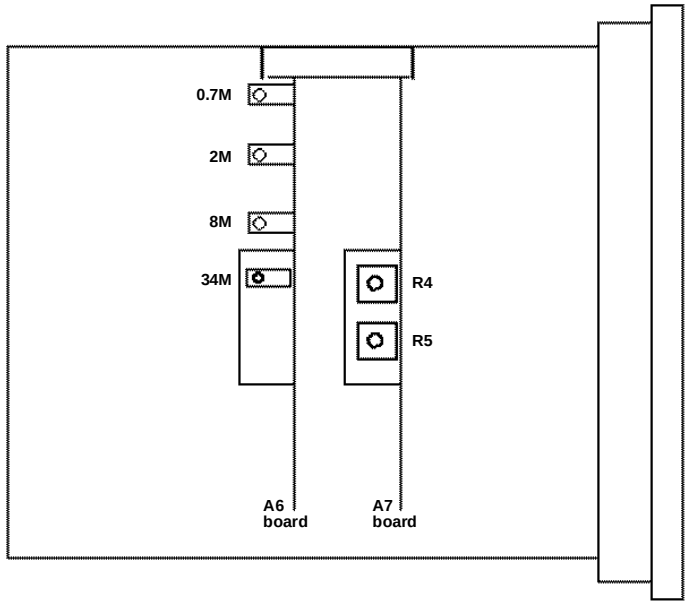


Figure 3-5 UPDH Module (topside) Adjustable Components

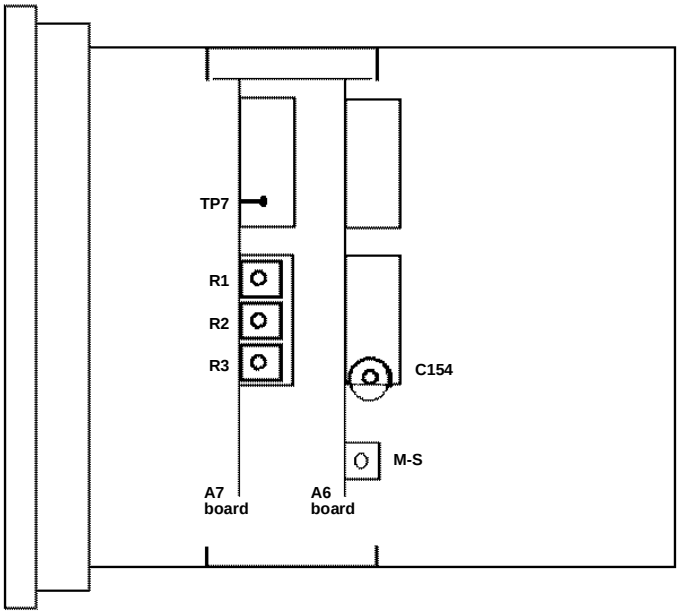


Figure 3-6 UPDH Module (underside) Adjustable Components

Procedure

34 Mb/s Recovered Clock Frequency

1 Select the **CALIBRATION** function on the OTHER display.

2 Using ↓, **DECREASE DIGIT** and ↑, **INCREASE DIGIT** keys, set the CALIBRATE PASSWORD to [1243].

3 Set the CALIBRATION ITEM to CLOCK EXTRACT and SELECTED RATE to 34 Mb/s.

4 Press RUN/STOP.

5 Adjust A6R4 (34M) to obtain a displayed TARGET FREQUENCY between 34,361,200 Hz and 34,374,800 Hz.

6 Once set, press RUN/STOP.

140 Mb/s Recovered Clock Frequency

7 Set the CALIBRATION ITEM to CLOCK EXTRACT and SELECTED RATE to 140 Mb/s.

8 Press RUN/STOP.

9 Adjust A6C154 (139M) to obtain a displayed TARGET FREQUENCY between 139,125,000 Hz and 139,403,000 Hz.

10 Once set, press RUN/STOP.

NOTE The remaining Clock Recovery adjustments can only be performed with the PDH Module fitted on a special extender card. When removing the Module to use the Extender Card, you MUST follow the Module Removal and Replacement procedure given in the Service Section of this manual.

704 kb/s Recovered Clock Frequency

11 Remove the PDH Module (see NOTE above), fit the Extender Card into the A6 slot in the Mainframe, then plug the A6 Assembly onto the Extender Card.

12 Set the CALIBRATION ITEM to CLOCK EXTRACT and SELECTED RATE to 704 kb/s.

13 Press RUN/STOP.

14 Adjust A6R1 (0.7M) to obtain a displayed TARGET FREQUENCY between 703,860 Hz and 704,140 Hz.

15 Once set, press RUN/STOP.

2 Mb/s Recovered Clock Frequency

16 Set the CALIBRATION ITEM to CLOCK EXTRACT and SELECTED RATE to 2 Mb/s.

17 Press RUN/STOP.

18 Adjust A6R2 (2M) to obtain a displayed TARGET FREQUENCY between 2,047,590 Hz and 2,048,410 Hz.

19 Once set, press RUN/STOP.

8 Mb/s Recovered Clock Frequency

20 Set the CALIBRATION ITEM to CLOCK EXTRACT and SELECTED RATE to 8 Mb/s.

21 Press RUN/STOP.

22 Adjust A6R3 (8M) to obtain a displayed TARGET FREQUENCY between 8,446,310 Hz and 8,449,690 Hz.

23 Once set, press RUN/STOP.

SDH Transmitter (Options US1 and AIT)

A9 SDH Assembly.

Adjustment Reference

	US1	A1T
CMI ZEROS Pulse Mark:Space Ratio	A9R1	A9R53
CMI ONES Pulse Mark:Space Ratio	A9R2	A9R38
CMI Tx Pulse Amplitude	A9R3	A9R22

Description

An Oscilloscope is connected to the Data Output port and A9R1 and R2 are adjusted to optimize the displayed CMI pulse Mark to Space Ratio on both All Zeroes and All Ones Patterns. The pulse Amplitude is measured on the Oscilloscope and set using R3.

Equipment Required

Oscilloscope	HP 54520A
75/50Ω Matching Pad	HP 11852B

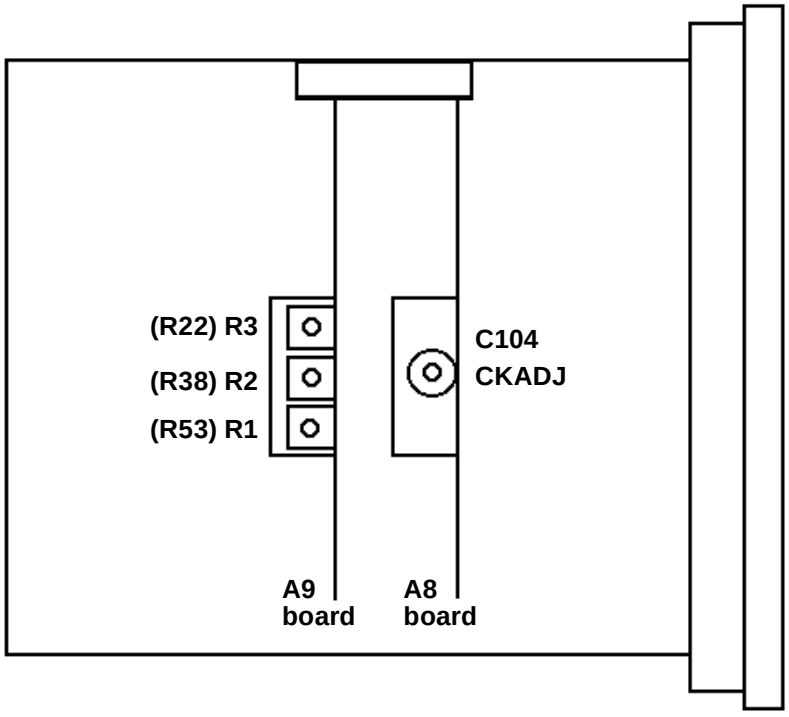


Figure 3-7 SDH Module (topside) Adjustable Components

Procedure

CMI Pulse Amplitude

1 Connect up the equipment as shown below.

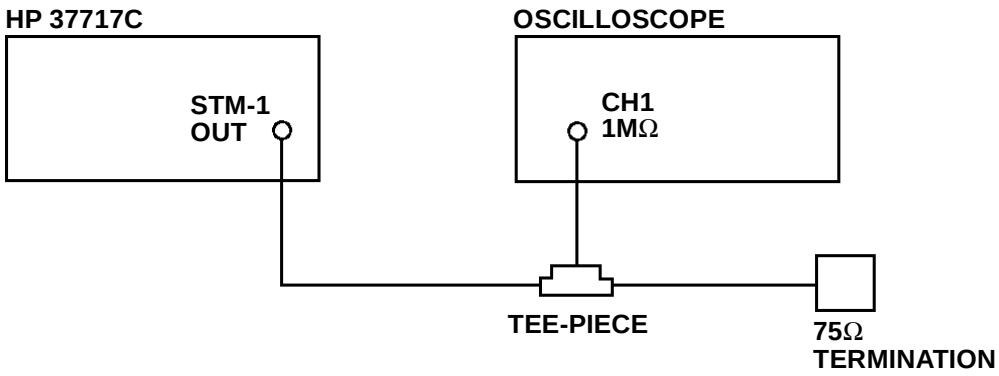
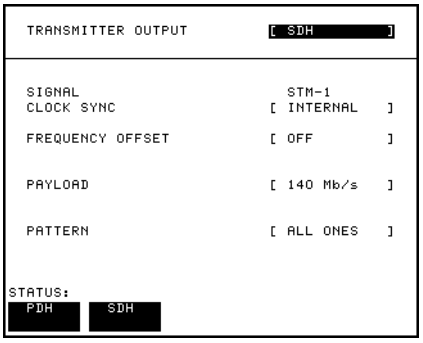


Figure 3-8 STM-1 Transmitter Output Waveshape, Test Setup

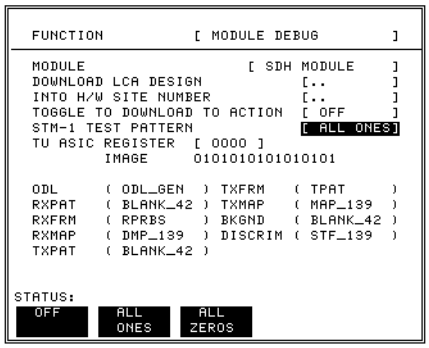
2 Press TRANSMIT and set up the display as shown below.



3 Make the following key sequence on the HP 37717C to obtain the special MODULE DEBUG display.

Press OTHER, ⇦, MORE, ⇦, MORE, ⇦, MORE and OTHER.

Press MORE until MODULE DEBUG appears in the softkey menu.
Press MODULE DEBUG and set up the display as shown below.



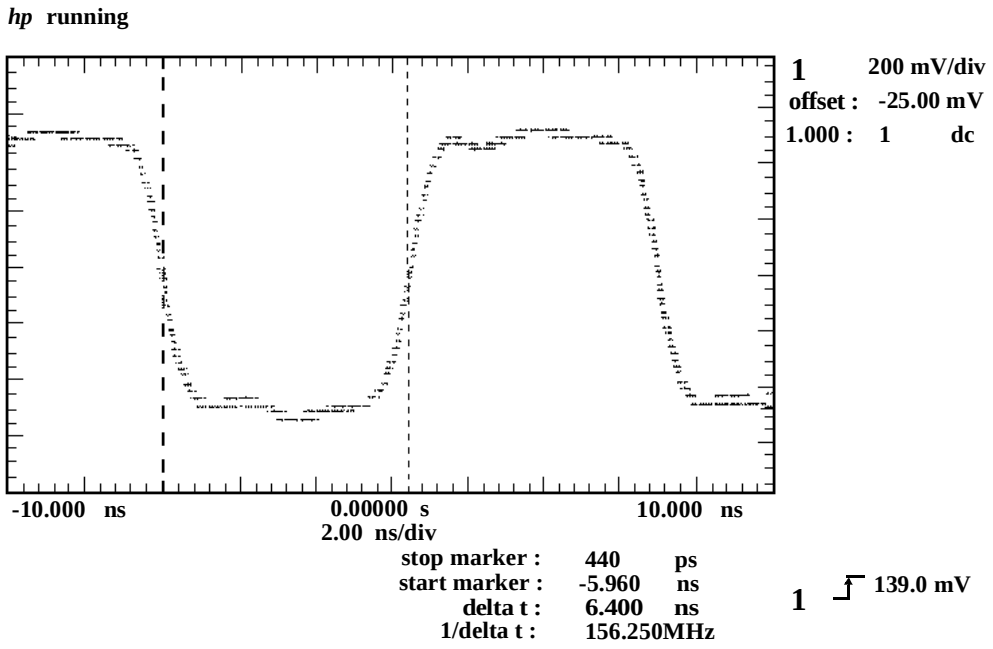
CAUTION When using the MODULE DEBUG display, ONLY modify the STM-1 TEST PATTERN. Altering other parameters can damage instrument firmware - exit this display after setup to eliminate any possibility of accidental modification.

4 Set the Oscilloscope Channel 1 Probe Attenuation factor to X 2.40 (equivalent to 7.6 dB) to compensate for the Matching Pad attenuation.

5 Press AUTOSCALE on the Oscilloscope and adjust the timebase and Delay to display a CMI pulse as shown below.

6 Using the Oscilloscope, measure the pulse amplitude at the half-width point.

7 Adjust A9R3, R22 to obtain a pulse amplitude of 1 Volt pk-pk.



8 STM-1 All Ones Pattern

CMI All Ones Pulse Mark:Space Ratio

9 Using the Oscilloscope, measure the pulse Mark to Space Ratio.

10 Adjust A9R2, R38 to obtain a Mark to Space Ratio of 1:1.

CMI All Zeros Pulse Mark:Space Ratio

11 Set the STM-1 TEST PATTERN to ALL ZEROS on the HP 37717C MODULE DEBUG display.

12 Using the Oscilloscope, measure the pulse Mark to Space Ratio.

13 Adjust A9 R1, R53 to obtain a Mark to Space Ratio of 1:1.

14 Repeat steps 8 to 12 until no further adjustment is required.

SDH Receiver (Option AIT)

A9 SDH Assembly.

Adjustment Reference

155.52 MHz Recovered Clock frequency	**A9C230**

Description

A Frequency Counter is connected to the Recovered Clock Oscillator output Probe Point and A9C230, C21 is adjusted to bring the clock free-run frequency within specified limits.

Equipment Required

Frequency Counter	**HP 5335A Opt 001**
10:1 Oscilloscope Probe	**HP 10435A**
Extender Card	**HP 37714-60099**

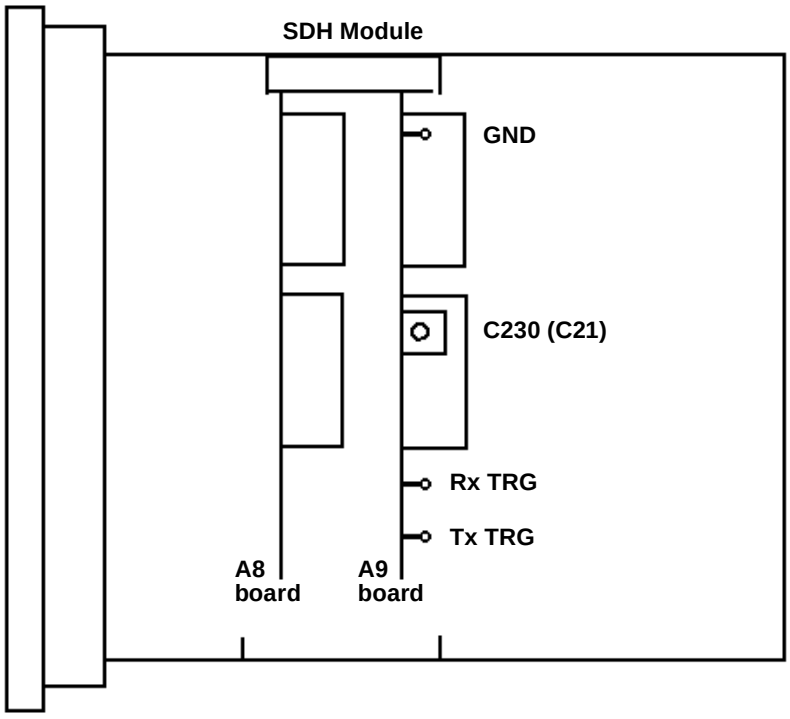


Figure 3-9 SDH Module (underside) Adjustable Components

Procedure

NOTE The probe points for this adjustment can only be accessed with the SDH Module fitted on a special Extender Card. When removing the Module to use the Extender Card, you MUST follow the procedure in Module Removal and Replacement given in the Service Section of this manual.

155.52 MHz Recovered Clock Frequency

1. Remove the SDH Module (see NOTE above), fit the Extender Card into the A9 slot in the Mainframe, then plug the A9 Assembly onto the Extender Card.
2. Select Frequency A and 1MΩ input impedance on the Frequency Counter.
3. Connect the Frequency Counter Input A to probe point E6 on the A9 Assembly using the 10:1 probe (ground the probe on the pad beside E6).
4. Adjust A9C230, C21 to obtain a reading on the Counter between 154,520,000 Hz and 156,520,000 Hz.
5. Disconnect all test equipment.

External Clock (Option A1T)

A8 Offset Clock Assembly.

Adjustment Reference Offset Clock Assembly.

External MTS Recovered Clock frequency	**A8C104 (CK ADJ)**

Description

A 2 MB/s PRBS Data signal from the HP 37717C Communications Performance Analyzer is applied to the External MTS Reference port on the HP 37717C. The Recovered Clock frequency is optimized by monitoring the clock oscillator output on an Oscilloscope and adjusting A8C104 to minimize the displayed jitter.

Equipment Required

Digital Transmission Test Set	**HP 37717C**
Oscilloscope	**HP 54520A**
10:1 Oscilloscope Probe	**HP 10435A**

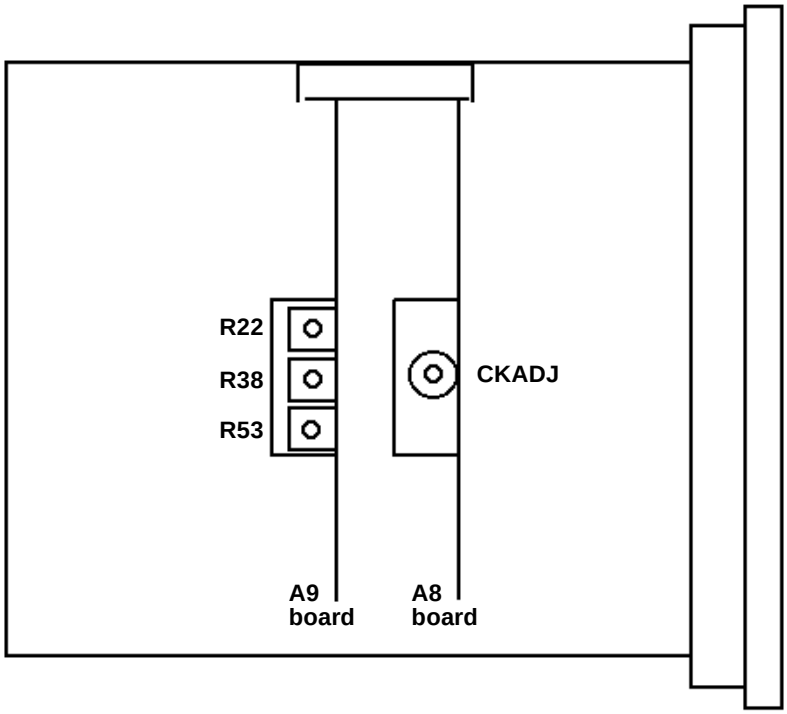
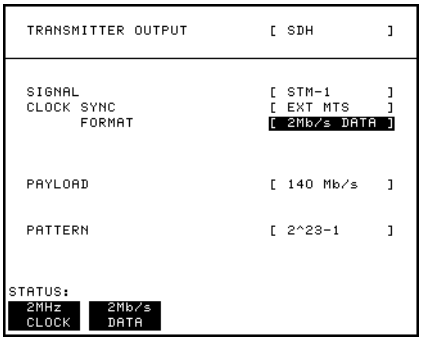


Figure 3-10 SDH Module (topside) Adjustable Components

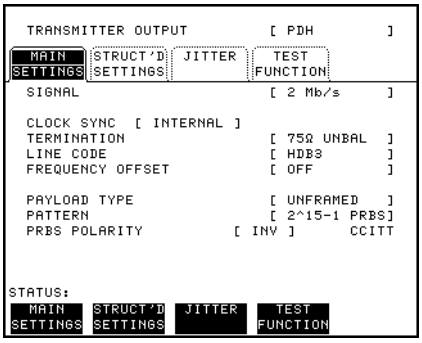
Procedure

External MTS Recovered Clock Frequency

1 Set the HP 37717C as follows:



2 Set the Test Set as shown and connect the 2 Mb/s output to the External MTS Clock IN 75Ω Unbalanced port on the HP 37717C SDH module.



3 Connect the Oscilloscope Probe to TP3 (Clock Out) on the A8 Assembly using the 10:1 probe (ensure probe is properly grounded). TP3 is accessible through a slot in the bottom of the instrument.

4 Press AUTOSCALE on the Oscilloscope and adjust the Timebase and Delay to display a waveform similar to that shown on Page 3-24 in Figure 3-11.

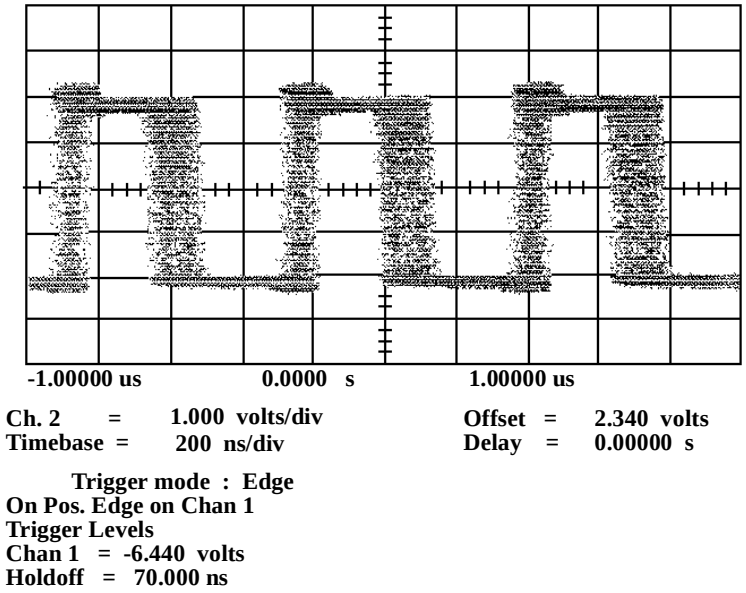


Figure 3-11 External MTS Clock Minimum Jitter Adjustment

5 Adjust A8C104 (CKADJ) to obtain minimum jitter on the displayed waveform.

6 Disconnect all test equipment.

1310 nm STM-1 Optical Transmitter (Option UH1 Only)

A11 Optical Assembly.

Adjustment Reference

Optical Tx Power Output Level	**A11 R1**

Description

An Optical Power Meter is connected to the output of the 155 Mb/s Optical Transmitter and the power output is adjusted to the correct level using A11R1.

Equipment Required

Power Meter	**HP 8153A**
Power Meter Sensor Module	**HP 81536A**
FC/PC Connector Interface	**HP 81000F1**
Optical Cables (quantity 2)	**HP 11871A**
Extender Card	**HP 37714-60099**

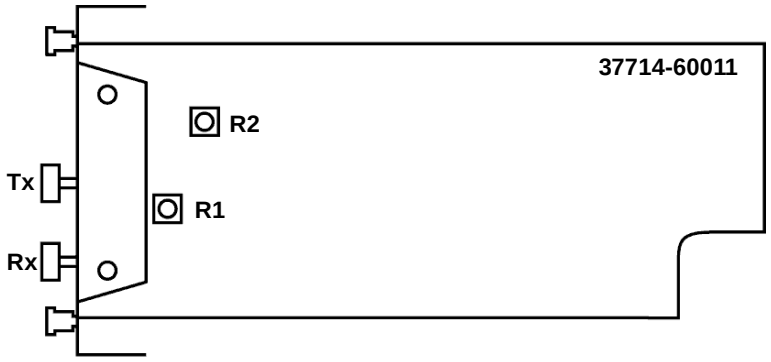


Figure 3-12 STM-1 Adjustable Components

Procedure

WARNING

The following safety precautions must be observed when servicing the optical module. The optical modules generate laser signals which can cause serious injury. The following instructions must be followed:

Check the connector configuration of the Fibre Optic Interfaces. If these are fitted with a connector interface other than FC/PC then remove the existing connector interface and fit the FC/PC connector interface.

Check for any damage to the HP 37717C Fibre Optic Interface spring-loaded aperture covers and connectors. Do not power up the instrument if in any doubt about the integrity of these connectors.

Make all connections to the HP 37717C Fibre Optic Interfaces before powering up the instrument.

STM-1 Optical Tx Power Output Level

NOTE

This adjustment can only be performed with the Module fitted on a special extender card. When removing the Optical Module to use the Extender Card, you MUST follow the procedure in Module Removal and Replacement given in the Service Section of this manual.

1. Connect the STM-1 Optical Out port to the HP 8153A Power Meter via the Power Sensor Module, (ensure that all connections are tight and that the cable has no twists).
2. Switch on the HP 37717C and check immediately that on power-up that the LASER ON LED on the front panel illuminates for a few seconds.
3. Recall the Default Settings on the HP 8153A.
   Press [MODE] to select MENU on the HP 8153A.
   Press [SYSTEM] to display RECALL.
   Press [EDIT], select 0 — -> A and press [EXEC] to recall the default settings (wavelength = 1310 nm, measurement time = 200 ms, autorange).
4. Press [MODE] then [dBmw] to select the Power Level measurement on the HP 8153A.
5. Press [TRANSMIT] on the HP 37717C and set SIGNAL to STM-1 OPT.
6. Verify that the Front Panel LASER ON LED is lit indicating that the laser is enabled.
7. Adjust A11R1 to obtain a Power Meter reading of –9.1 dBm.
8. Press [OTHER], set STORED SETTINGS NUMBER to 0 (Default Settings) and press [RECALL].
9. Verify that the Front Panel LASER ON LED is NOT lit indicating that the laser is disabled.
10. Disconnect all test equipment.

1310 nm STM1/4 Optical Transmitter (Option USN and UKT)

Adjustment Reference

1310 nm Optical Tx Power Output Level	A63R26

Description

An Optical Power Meter is connected to the output of the 622 Mb/s Optical Transmitter and the power output is adjusted to the correct level using R26.

Equipment Required

Power Meter	HP 8153A
Power Meter Sensor Module	HP 81536A
FC/PC Connector Interface	HP 81000F1
Optical Cables (quantity 2)	HP 11871A
Extender Card	HP 37714-60099

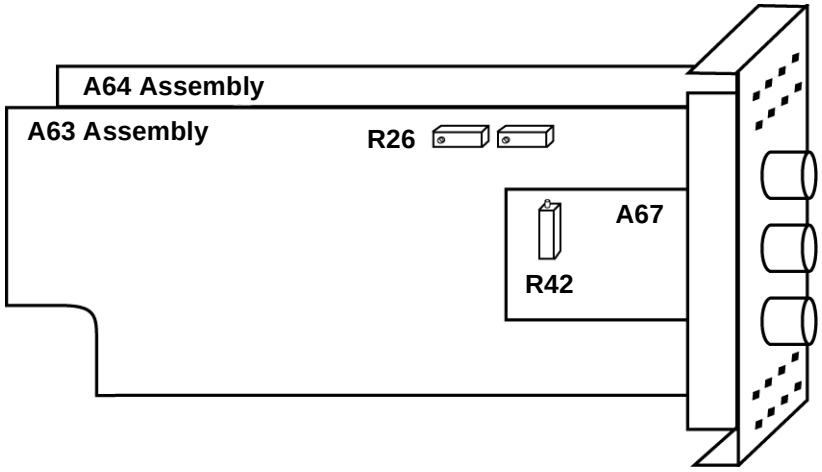


Figure 3-13 STM1/4 Adjustable Components

Procedure

WARNING

The following safety precautions must be observed when servicing the optical module. The optical modules generate laser signals which can cause serious injury. The following instructions must be followed:

Check the connector configuration of the Fibre Optic Interfaces. If these are fitted with a connector interface other than FC/PC then remove the existing connector interface and fit the FC/PC connector interface.

Check for any damage to the HP 37717C Fibre Optic Interface spring-loaded aperture covers and connectors. Do not power up the instrument if in any doubt about the integrity of these connectors.

Make all connections to the HP 37717C Fibre Optic Interfaces before powering up the instrument.

STM-4 Optical Tx Power Output Level

NOTE

This adjustment can only be performed with the Module fitted on a special extender card. When removing the Optical Module to use the Extender Card, you MUST follow the procedure in Module Removal and Replacement given in the Service Section of this manual.

1 Connect the 1310 nm Optical Out port to the HP 8153A Power Meter via the Power Sensor Module, (ensure that all connections are tight and that the cable has no twists).

2 Switch on the HP 37717C and check immediately that on power-up that the LASER ON LED on the front panel illuminates for a few seconds.

3 Recall the Default Settings on the HP 8153A.
Press [MODE] to select MENU on the HP 8153A.
Press [SYSTEM] to display RECALL.
Press [EDIT], select 0 — -> A and press [EXEC] to recall the default settings (wavelength = 1310 nm, measurement time = 200 ms, autorange).

4 Press [MODE] then [dBmw] to select the Power Level measurement on the HP 8153A.

5 Press [TRANSMIT] on the HP 37717C and set SIGNAL to STM-4 OPT.

6 Verify that the Front Panel LASER ON LED is lit indicating that the laser is enabled.

7 Adjust A63R26 to obtain a Power Meter reading of –10dBm.

NOTE

A63 is the full-length board on the left side of the module.

8 Press [OTHER], set STORED SETTINGS NUMBER to 0 (Default Settings) and press [RECALL].

9 Verify that the Front Panel LASER ON LED is NOT lit indicating that the laser is disabled.

10 Disconnect all test equipment.

1550 nm STM1/4 Optical Transmitter (Option USN Only)

Adjustment Reference

1550 nm Optical Tx Power Output Level	A67R42

Description

An Optical Power Meter is connected to the STM1/4 Optical Tx and the power output is adjusted to the correct level using and marked (OPT PWR) A67R42.

Equipment Required

Power Meter	HP 8153A
Power Meter Sensor Module	HP 81536A
FC/PC Connector Interface	HP 81000F1
Optical Cables (quantity 2)	HP 11871A
Extender Card	HP 37714-60099

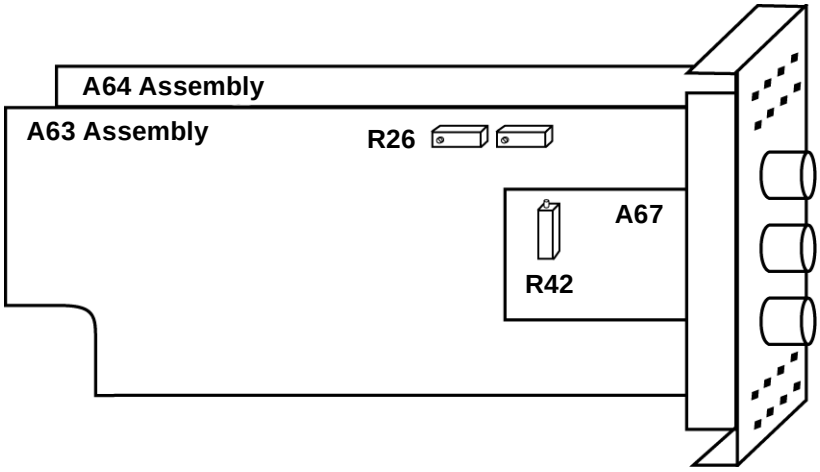


Figure 3-14 STM1/4 (1550 nm) Adjustable Components

Procedure

WARNING

The following safety precautions must be observed when servicing the optical module. The optical modules generate laser signals which can cause serious injury. The following instructions must be followed:

Check the connector configuration of the Fibre Optic Interfaces. If these are fitted with a connector interface other than FC/PC then remove the existing connector interface and fit the FC/PC connector interface.

Check for any damage to the HP 37717C Fibre Optic Interface spring-loaded aperture covers and connectors. Do not power up the instrument if in any doubt about the integrity of these connectors.

Make all connections to the HP 37717C Fibre Optic Interfaces before powering up the instrument.

STM-4 Optical Tx Power Output Level

NOTE

This adjustment can only be performed with the Module fitted on a special extender card. When removing the Optical Module to use the Extender Card, you MUST follow the procedure in Module Removal and Replacement given in the Service Section of this manual.

1. Connect the 1550 nm Optical Out port to the HP 8153A Power Meter via the Power Sensor Module, (ensure that all connections are tight and that the cable has no twists).
2. Switch on the HP 37717C and check immediately that on power-up that the LASER ON LED on the front panel illuminates for a few seconds.
3. Recall the Default Settings on the HP 8153A.
   Press [MODE] to select MENU on the HP 8153A.
   Press [SYSTEM] to display RECALL.
   Press [EDIT], select 0 — -> A and press [EXEC] to recall the default settings (wavelength = 1550 nm, measurement time = 200 ms, autorange).
4. Press [MODE] then [dBmw] to select the Power Level measurement on the HP 8153A.
5. Press [TRANSMIT] on the HP 37717C and set SIGNAL to STM-4 OPT.
6. Verify that the Front Panel LASER ON LED is lit indicating that the laser is enabled.
7. Adjust A67R42 to obtain a Power Meter reading of –1 dBm.

NOTE

A67 is a small board attached to A63 board.

8. Press [OTHER], set STORED SETTINGS NUMBER to 0 (Default Settings) and press [RECALL].
9. Verify that the Front Panel LASER ON LED is NOT lit indicating that the laser is disabled.
10. Disconnect all test equipment.

Jitter Transmitter (Option UHK)

A12 Jitter Transmitter Assembly

In order to set up the Jitter Transmitter, the reference 37717C must be fitted with known good PDH Tx and Rx cards (37714-60006 and 37714-60007).

Adjustment Reference

34 MHz Duty Cycle	**A12R136**
140 MHz Duty Cycle	**A12R135**
DC Offset	**A18R2, R3**
Residual Amplitude	**A12R5**
Control Loop Gain	**A12R1**

Description

Duty Cycles - An Oscilloscope is used to monitor the output from the PDH Transmitter and the Duty Cycles of both 34 Mb/s and 140 Mb/s data are adjusted on an all ones pattern. Both these adjustments are critical to the operation of the jitter transmitter.

Control Loop Adjustments - The DC offset and residual amplitude of the jitter transmitter control loop are minimized using R2, R3 and R5. With 0.76 UI set up on the jitter transmitter display, the loop gain is set by monitoring the jitter output with a spectrum analyzer and adjusting R1 to minimize the carrier Bessel Null. This sets the transmitted jitter to exactly 0.765 UI.

The Jitter Transmit Modulation Depth adjustment is semi-automatic and is performed by using a special internal calibration routine and a Spectrum Analyzer. The HP 37717C TX PDH OUTPUT is connected to the Analyzer (via 75/50Ω Matching Pad) and set to the first calibration point in the routine. With the Analyzer set to display the transmitted data spectrum, a Bessel Null should be observed. The HP 37717C DAC output is adjusted using the calibration routine to optimize this Bessel Null. This sets the transmitted jitter to exactly 0.765 UI. This process is repeated for all other Calibration points in the routine. These calibration points have been determined to optimize jitter accuracy over a wide range of frequencies and amplitudes.

Equipment Required

Oscilloscope	**HP 54520A**
Spectrum analyzer	**HP 8568B**
75/50Ω Matching Pad	**HP 11852B**

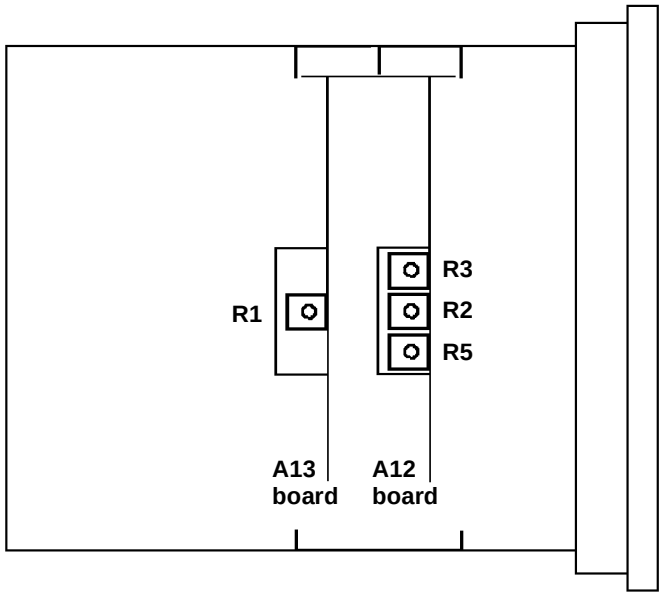


Figure 3-15 Jitter Rx Module, Jitter Tx Module (topside) Adjustable Components

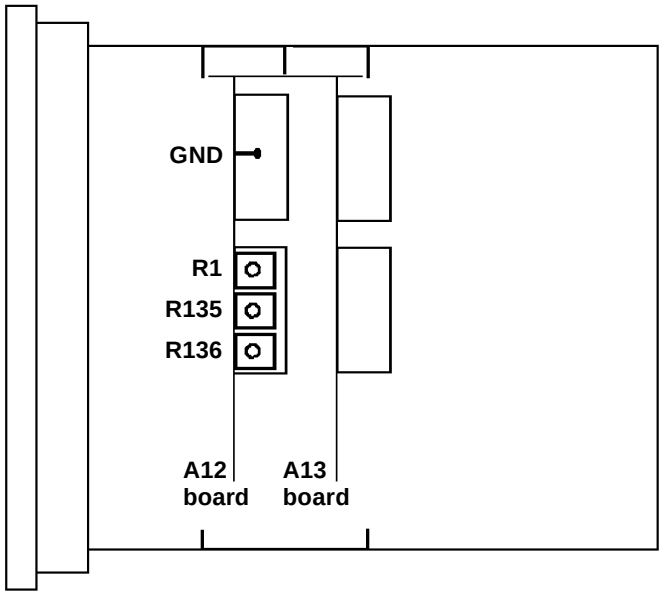


Figure 3-16 Jitter Rx Module, Jitter Tx Module (underside) Adjustable Components

Pre-Adjustment Setup

Before carrying out any adjustment to the HP 37717C Jitter Transmitter Module, perform the following pre-adjustment setup.

CAUTION This procedure uses the special MODULE DEBUG display on the HP 37717C. When using the MODULE DEBUG display, ONLY modify parameters shown. Altering other parameters can damage instrument firmware - exit the Debug Display after setup to prevent accidental damage.

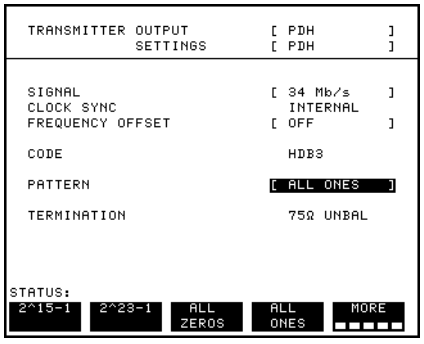
1. Press the [OTHER] key then select the **SETTINGS CONTROL** softkey.
2. Select Transmitter and Receiver to COUPLED.
3. Make the following key sequence on the HP 37717C to obtain the special MODULE DEBUG display. Press [OTHER], [⇧], **MORE**, [⇧], **MORE**, [⇧], **MORE** and [OTHER]. Press **MORE** until MODULE DEBUG appears in the softkey menu.
4. Press **MODULE DEBUG** and select MODULE to PDH MODULE on the Module Debug Display.
5. Set the VCO CONTROL MODE to FIXED on the PDH Module Debug Display.
6. Set the MODULE to JITTER MODULE on the Module Debug Display.
7. Set the TX CALIBRATION to OFF on the Jitter Module Debug Display.
8. Set the RX CALIBRATION to OFF on the Jitter Module Debug Display.

CAUTION The above sequence must be performed each time power is cycled on the HP 37717C, as all MODULE DEBUG parameters will adopt DEFAULT values when power is cycled.

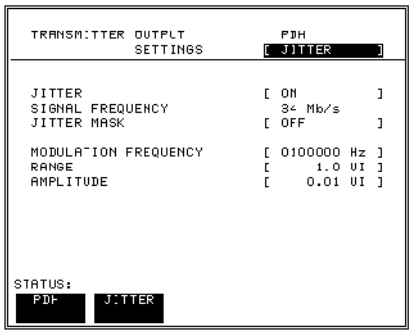
Procedure

34 MHz VCO Duty Cycle

1. Press [TRANSMIT] and set up the display as shown below.



2 Press TRANSMIT and set up the display as shown below.

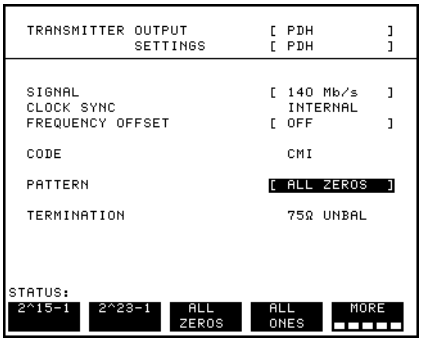


3 Connect the HP 37717C Unbalanced PDH 75Ω SIGNAL OUT port to the Oscilloscope INPUT 1 via the 75/50Ω Matching Pad - set the Oscilloscope termination to 50Ω

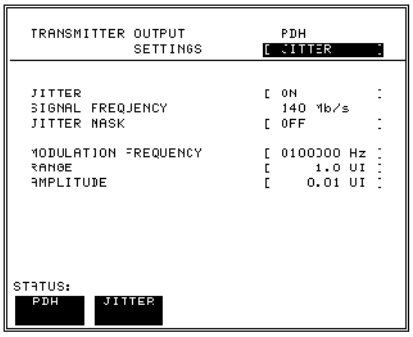
4 Adjust A12R136 to obtain a positive pulse width of 14.56 ns as measured on the Oscilloscope.

140 MHz VCO Duty Cycle.

1 Press TRANSMIT and set up the display as shown below.



2 Press TRANSMIT and set up the display as shown below.



3 Connect the HP 37717C Unbalanced PDH 75Ω SIGNAL OUT port to the Oscilloscope INPUT 1 via the 75/50Ω Matching Pad - set the Oscilloscope termination to 50Ω

4 Adjust A12R135 to obtain a DUTY CYCLE of 50% as measured on the Oscilloscope.

Control Loop DC Offset

CAUTION The following adjustment requires data to be written directly to the Jitter Tx hardware. **Take great care to select the correct address before writing data.**

1 Make the following key sequence on the HP 37717C to obtain the special DEBUG FUNCTION display.
Press [OTHER], [⇧], MORE, [⇧], MORE, [⇧], MORE and [OTHER].
Press MORE until DEBUG FUNCTION appears in the softkey menu.

2 Press DEBUG FUNCTION and select WRITE TO H/W on the Display or if firmware revision is 3448 and above, select MODULE DEBUG then MODULE GENERAL then WRITE TO H/W.

3 Set the ADDRESS to SINGLE WRITE then move the cursor to the address field and select the address as follows:

Jitter Transmitter Module Position in the Mainframe	Address Code
Slot 2 (If SDH Option NOT fitted)	D20012
Slot 4 (If SDH Option fitted)	D40012

CAUTION Take great care to select the correct address before writing data. Refer to diagrams in the Dismantling and Re-assembly part of this Manual if in doubt about the position of the Jitter Tx module.

4 Move the cursor to the DATA field and set the data to 0000000000000001.

5 Move the cursor to the TOGGLE TO WRITE TO H/W field and set to WRITE H/W. The jitter transmitter modulation will now be switched off.

6 Connect a Digital Voltmeter, set to DC Volts to A12TP10 and TP Ground.

7 Adjust A12R2 to obtain a reading of 0 mV on the Digital Voltmeter.

8 Connect the Digital Voltmeter set to DC Volts to A12TP11 and TP Ground

9 Adjust A12R3 to obtain a reading of 0 mV on the Digital Voltmeter.

10 Move the cursor to the TOGGLE TO WRITE TO H/W field and set to OFF. The jitter transmitter modulation will now be under instrument control again.

Control Loop Residual Amplitude

CAUTION The following adjustment requires data to be written directly to the Jitter Tx hardware. **Take great care to select the correct address before writing data.**

1 Connect the Spectrum Analyzer RF INPUT to A12 TP7 and TP ground via 1:1 probe.

2 Set the Spectrum Analyzer as follows:

Centre Frequency	100 kHz	Frequency Span	20 kHz
Reference Level	0 dBm	Sweep Time	1.0 seconds
Video Bandwidth	1 kHz	Resolution Bandwidth	100 Hz

3 Make the following key sequence on the HP 37717C to obtain the special DEBUG FUNCTION display. Press OTHER, ⇦, MORE, ⇦, MORE, ⇦, MORE and OTHER. Press MORE until DEBUG FUNCTION appears in the softkey menu.

4 Press DEBUG FUNCTION and select WRITE TO H/W on the Display or if firmware revision is 3448 and above, select MODULE DEBUG then MODULE GENERAL then WRITE TO H/W.

5 Set the ADDRESS to SINGLE WRITE then move the cursor to the address field and select the address as follows:

Jitter Transmitter Module Position in the Mainframe	Address Code
Slot 2 (If SDH Option NOT fitted)	D20004
Slot 4 (If SDH Option fitted)	D40004

CAUTION Take great care to select the correct address before writing data. Refer to diagrams in Dismantling and Re-assembly part of this Section if in doubt about the position of the Jitter Tx module.

6 Move the cursor to the DATA field and set the data to 0000000000000000.

7 Move the cursor to the TOGGLE TO WRITE TO H/W field and set to WRITE H/W. This sets the DAC value to zero.

8 Adjust A12R5 until the 100 kHz spectral line displayed on the Spectrum Analyzer is at a minimum.

9 Move the cursor to the DATA field and set the data to 0000000001000000.

10 Move the cursor to the TOGGLE TO WRITE TO H/W field and set to WRITE H/W. This sets the DAC output to a high value.

11 Check that there is a spectral line displayed on the Spectrum Analyzer.

12 Move the cursor to the DATA field and set the data to 0000000000000000.

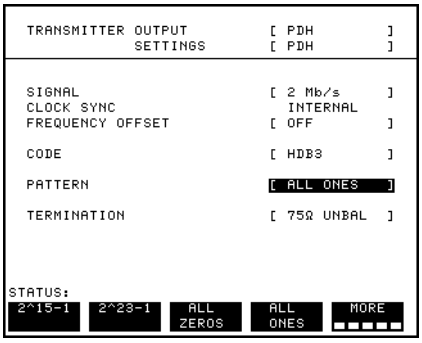
13 Move the cursor to the TOGGLE TO WRITE TO H/W field and set to WRITE H/W. This sets the DAC value back to zero.

14 Check that the spectral line displayed on the Spectrum Analyzer is at the previous minimum value again - if not, repeat the adjustment procedure above.

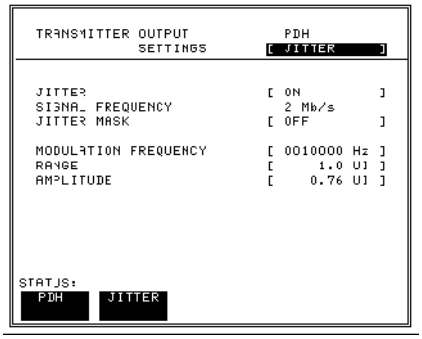
15 Move the cursor to TOGGLE TO WRITE TO H/W field and set to OFF. The jitter transmitter modulation will now be under instrument control again.

Control Loop Gain

1 Press TRANSMIT on the HP 37717C and set up the display as shown below.



2 Press TRANSMIT and set up the display as shown below.



3 Connect the HP 37717C Unbalanced PDH 75Ω SIGNAL OUT to the Spectrum Analyzer RF INPUT via the 75/50Ω Matching Pad - set the Spectrum Analyzer termination to 50Ω

4 Set the Spectrum Analyzer as follows;

Centre Frequency	**2048 kHz**
Reference Level	**0 dBm**
Video Bandwidth	**1 kHz**
Frequency Span	**100 kHz**
Sweep Time	**1.0 seconds**
Resolution Bandwidth	**100 Hz**

5 A Bessel Null spectrum similar to that given on page 3-38 should be displayed on the Spectrum Analyzer.

6 Adjust A12R1 until the central spectrum line displayed on the Spectrum Analyzer is at a minimum.

7 Change the Jitter Range to 10 UI and set the jitter amplitude to 9.7 UI.

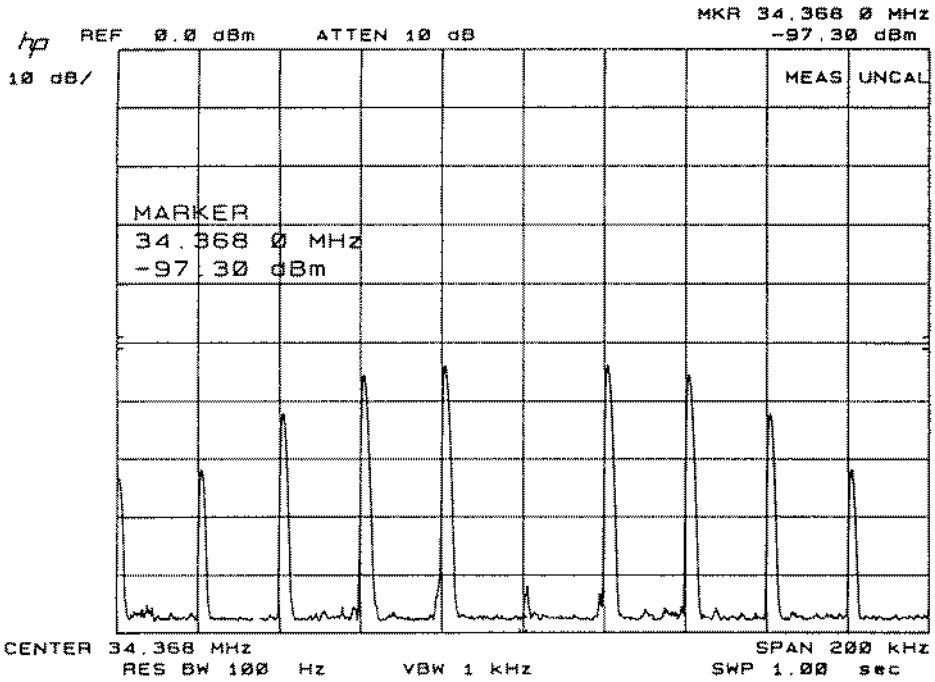


Figure 3-17 Bessel Null Example

8 Adjust A12R1 until the central spectrum line displayed on the Analyzer is at a minimum. Only a small adjustment should be required.

Jitter Tx Modulation Depth

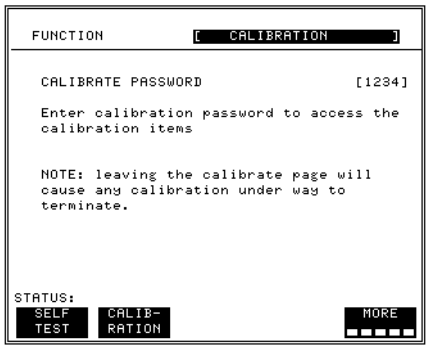
1 Connect the HP 37717C Unbalanced 75Ω SIGNAL OUT port to the Spectrum Analyzer RF INPUT via the 75/50Ω Matching Pad - set the Spectrum Analyzer termination to 50Ω

2 Set the Spectrum Analyzer as follows:

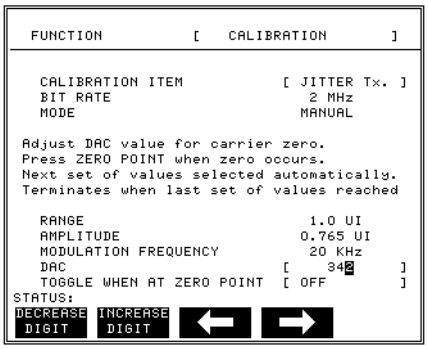
Centre Frequency	**2048 kHz**
Reference Level	**0 dBm**
Video Bandwidth	**1 kHz**
Frequency Span	**100 kHz**
Sweep Time	**1.0 seconds**
Resolution Bandwidth	**100 Hz**

3 Setup the HP 37717C [OTHER] display as shown below.

4 Set the CALIBRATE PASSWORD to 1243.



5 Select CALIBRATION ITEM to JITTER TX.



6 Press [RUN/STOP] to start calibration. A spectrum similar to that given on page 3-38 should be displayed on the Spectrum Analyzer.

7 Move the cursor to DAC and adjust the DAC value (using only the Least Significant Bit) until the carrier level displayed on the Spectrum Analyzer is at a minimum. (Bessel Null).

8 When the Bessel Null is obtained, move the cursor to TOGGLE WHEN AT ZERO POINT and press ZERO POINT. This stores the value for the modulation frequency and the routine automatically moves on to the next calibration value.

9 Repeat steps 7 and 8 for each new calibration value. At each change of BIT RATE, set the Spectrum Analyzer center frequency to the new bit rate frequency and re-adjust the span to optimize the spectrum around the carrier.

10 When finished, the HP 37717C display should indicate CALIBRATION PROCESS COMPLETE.

11 Press [OTHER] to return to normal operation then disconnect all test equipment.

12 Switch the HP 37717C off then on again to return the Debug Page parameter to default settings.

Jitter Generator (Options A3K, 140)

This section describes the setup procedure for part of the following options:

A3K, 140

In order to setup the jitter generator card, the test chassis must be fitted with known good PDH Rx and Tx cards (37717-60004 and 37717-60005) and an A1T module, 37714-60100.

Pre-Adjustment Setup

The following must be set on the front panel before any adjustments can be attempted on this card:

1 Set PDH Transmitter and Receiver settings to coupled by selecting:
OTHER, SETTINGS CONTROL, COUPLED.

2 The MODULE DEBUG page must be used to control the following settings, it can be found by using the following key sequence:
OTHER, ⇧, MORE, ⇧, MORE, ⇧, MORE, OTHER, MORE, MORE and MODULE DEBUG.

3 Set the PDH VCO control to fixed by selecting:
PDH MODULE.

VCO CONTROL MODE, FIXED.

4 Set Jitter Tx and Rx calibration off by selecting:
JITTER MODULE.

TX CALIBRATION, OFF.

RX CALIBRATION, OFF.

WARNING **All the debug functions set above will be reset if the instrument is power cycled, so this preparation procedure will have to be repeated every time the instrument has to be powered down, (e.g. if a card is moved on or off the extender card).**

NOTE Duty Cycle and Pulse width adjustments are critical to the jitter operation of the instrument, a great deal of care must be taken over these adjustments.

Procedure

2 MHz VCO Duty Cycle

1 Set the PDH data to 2 Mb/s All Ones pattern by selecting:
TRANSMIT:

SETTINGS, PDH

SIGNAL, 2 Mb/s

PATTERN, **ALL ONES**

Set the Tx jitter to 100,000 Hz modulation at 0.01 UI by selecting:

TRANSMIT

SETTINGS, **JITTER**

JITTER, **ON**

MODULATION FREQUENCY, **100000 Hz**

AMPLITUDE, **0.01 UI**

2 Set the Oscilloscope to 200 nsec/div and 500 mv/div., 50Ω input.

3 Connect PDH OUT to Oscilloscope via a 75Ω to 50Ω Converter, adjust the positive pulse width of the displayed waveform to 249 ns ±5 ns using A12R69 on the Jitter Tx card. Ensure that A12R69 can be vary the waveform by ±3 nsec without causing the waveform to go unstable.

NOTE The pulse width has been changed from 244 ns ±10 ns to 249 ns ±5 ns to ensure that the pulse width is not set up narrower than the nominal value of 244 ns.

8 MHz VCO Duty Cycle

1 Set the PDH data to 8 Mb/s, All Ones pattern by selecting:

TRANSMIT

SETTINGS, **PDH**

SIGNAL, **8 Mb/s**

PATTERN, **ALL ONES**

2 Set the Tx jitter to 100,000 Hz modulation at 0.01 UI as before:

3 Connect PDH OUT to Oscilloscope via a 75Ω to 50Ω Converter, adjust the positive pulse width of the displayed waveform to 59.2 ns ±4 ns using R47 on the Jitter Tx card.

34 MHz VCO Duty Cycle

1 Set the PDH data to 34 Mb/s, All Ones pattern by selecting:

TRANSMIT

SETTINGS, **PDH**

SIGNAL, **34 Mb/s**

PATTERN, **ALL ONES**

2 Set the Tx Jitter to 100,000 Hz modulation at 0.01 UI as before.

3 Connect PDH OUT to the Oscilloscope via a 75Ω to 50Ω Converter, adjust the positive pulse width of the displayed waveform to 14.56 ns ±1 ns using R40 on the Jitter Tx card.

140 MHz VCO Duty Cycle

1. With the Jitter Tx setting as above, set the PDH data to 140 Mb/s, All Zeroes pattern.
2. Connect PDH OUT to Oscilloscope via a 75Ω to 50Ω Converter, adjust the duty cycle of the displayed waveform to 50% ±1% using R56 on the Jitter Tx card.

Control Loop DC Offset Adjustment

1. This procedure requires access to the DEBUG pages as detailed in the preparation section, instead of selecting MODULE DEBUG, select GENERAL.
2. This debug page is used to read and write directly to the hardware, use this page to turn the jitter modulation off by selecting:

WRITE TO H/W

ADDRESS - SINGLE WRITE, D40012**

DATA - 0000000000000001

TOGGLE TO WRITE TO H/W- WRITE H/W

NOTE The "WRITE TO H/W" appears only momentarily, long enough to write the "DATA' then returns to "OFF".

NOTE ** The addresses of the system start at D10000 for the first mother board slot next to the front panel (front panel controller board is D00000) and increments toward the power supply end of the mother board. Identify the slot that the jitter Tx card is plugged into to get its slot address (in the above case D40000). The total address is obtained by adding the slot address to the appropriate offset address (in this case 0012H).

3. Using a Digital Voltmeter on Volts DC monitor TP8 with respect to ground (TP2).
4. Adjust R53 (top centre) until the Digital Voltmeter reading is 0 mV ±0.5 mV.
5. Monitor TP5 with respect to ground and adjust R39, until the Digital Voltmeter reading is 0 mV ±0.5 mV.
6. Set the jitter modulation back on by selecting:

DEBUG FUNCTION

WRITE TO H/W

ADDRESS- SINGLE WRITE, D40012**

DATA - 0000000000000000

TOGGLE TO WRITE TO H/W - WRITE H/W

7. Disconnect the Digital Voltmeter.

Loop Gain Setup

1. With the VCXO's still set to fixed and the Jitter cals still set to 'Off', set the PDH data to 2 Mb/s, All Ones pattern.
2. Set the jitter Tx to ON, 10,000 Hz modulation frequency, Range 1.0 UI.
3. Set the Jitter amplitude to 0.1 UI

4 Connect a Spectrum Analyzer via a 1 MΩ Oscilloscope probe (HP 10435A) to E6.

5 Find the 2.048 MHz spectral line by setting the centre frequency to 2.048 MHz, and span to 50 kHz to zoom in on the central spectral line.

6 Increase the jitter amplitude from 0.1 to 0.3 UI, noting that the central spectral component is the one that is decreasing in amplitude.

7 Adjust R21 until the central spectral line is at a maximum. This is only an approximate setting.

8 Increase the jitter amplitude to 0.76 UI.

9 Adjust R21 until the central line is at a minimum.

10 Decrease the modulation amplitude from 0.76 UI to 0.01 UI, in steps of 0.1 UI, and check that no other nulls appear on the central line. The above procedure will ensure that we always set the first null to a minimum.

2 MHz Reference Input - Minimum Jitter Adjust.

1 On a reference 37717C, do a recall panel zero.

2 Set the reference unit as follows:

TRANSMIT

SIGNAL, 2 Mb/s

LINE CODE, AMI

PATTERN, 2^15-1

3 Connect the SPDH TX on the Reference unit to the 2M BNC input of the A3K 37717C (J1).

4 Set the A3K test instrument as follows:

TRANSMIT

SIGNAL, 2 Mb/s

INTERFACE, CODED - (If UH3 is fitted).

CLOCK SYNC, EXT JITTER, DATA, 75 Ω

TERMINATION, 75 Ω UNBAL

LINE CODE, HDB3 HDB3

PAYLOAD TYPE, UNFRAMED

5 Connect an HP 54520A Oscilloscope to TP3 via a 10 kΩ pod and adjust L2 for minimum jitter. Secure the adjusting screw using Loctite 42540 (HP Part no. 0470-2089).

Jitter Receiver (Option UHN)

Jitter Receiver Assembly

Adjustment Reference

Measurement Loop Offset	**R2 and R4**
Jitter Hits Threshold Level	**R1**
Demod Jitter Output Level	**R68**
Wander Ref rec. clk	**L21**

NOTE The following adjustments require the instrument to be fitted with working PDH Transmit and Receive Module(s) and Jitter Generation module.

Description

Measurement Loop Offset - R4 is adjusted so that the narrow pulse displayed on an Oscilloscope connected to TP12 is at minimum amplitude; R2 is then adjusted so that this pulse has zero volts DC offset.

Jitter Hits threshold - R1 is adjusted to set the jitter hits alarm LED off with the jitter hits threshold set to 1.01 UI and the transmit jitter level set to 1.00 UI on the HP 37717C.

The Demodulated Jitter Output is connected to the 50Ω input of the Oscilloscope and R68 is adjusted until the amplitude of the displayed waveform is correct.

Equipment Required

Oscilloscope	**HP 54520A**
10 kΩ Oscilloscope Pod	**HP 54001A**
Module board Extender Card	**HP 37714-60099**

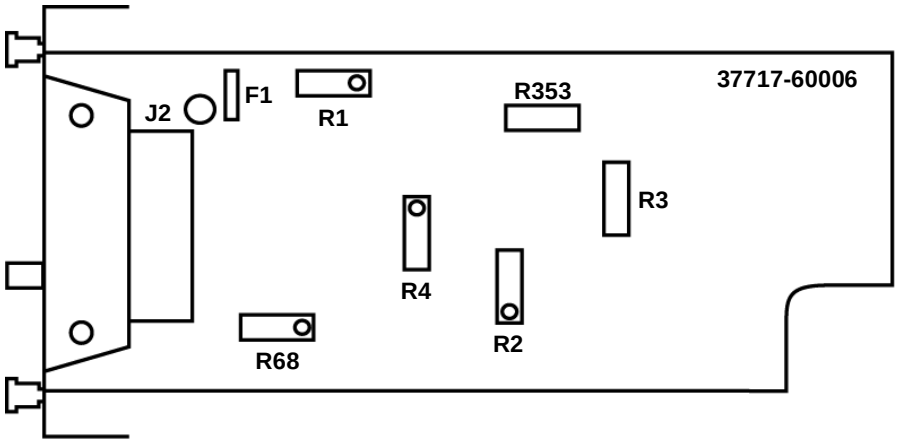


Figure 3-18 A6 Jitter Rx Module Adjustable Components

Pre-Adjustment Setup

Before carrying out any adjustment to the HP 37717C Jitter Receiver Module, perform the following pre-adjustment setup.

CAUTION This procedure uses the special MODULE DEBUG display on the HP 37717C. When using the MODULE DEBUG display, ONLY modify parameters shown. Altering other parameters can damage instrument firmware - exit the Debug Display after setup to prevent accidental damage.

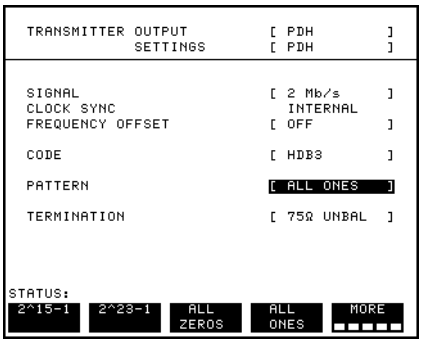
1. Remove the Jitter Receiver Module from the instrument and fit the 37717-60006 assembly on the extender card.
2. Press the [OTHER] key then **SETTINGS CONTROL** softkey.
3. Select Transmitter and Receiver COUPLED
4. Make the following key sequence on the HP 37717C to obtain the special MODULE DEBUG display. Press [OTHER], [⇧], **MORE**, [⇧], **MORE**, [⇧], **MORE** and [OTHER]. Press **MORE** until **MODULE DEBUG** appears in the softkey menu.
5. Press **MODULE DEBUG** and select MODULE PDH MODULE on the MODULE DEBUG display.
6. Set the VCO CONTROL MODE to FIXED on the PDH MODULE Debug Display.
7. Set the MODULE to JITTER MODULE on the MODULE DEBUG Display.
8. Set the TX CALIBRATION to ON on the Jitter MODULE DEBUG Display.
9. Set the RX CALIBRATION to OFF on the Jitter MODULE DEBUG Display.

CAUTION The above sequence must be performed each time power is cycled on the HP 37717C, as all MODULE DEBUG parameters will adopt DEFAULT values when power is cycled.

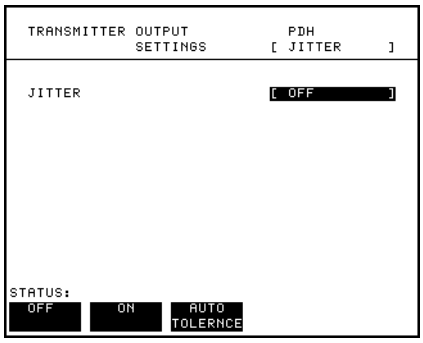
Procedure

Measurement Loop Offset

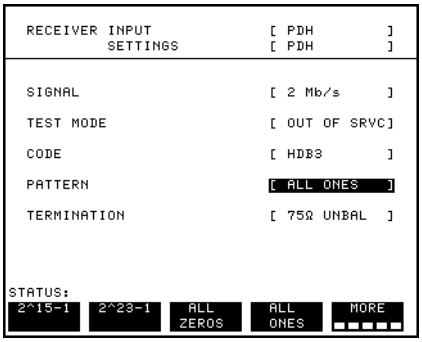
1 Press TRANSMIT and set up the display as shown below.



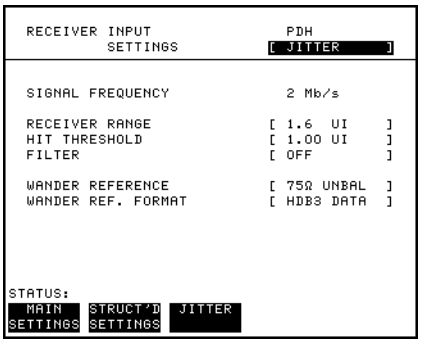
2 Press TRANSMIT and set up the display as shown below.



3 Press RECEIVE and set up the display as shown below.



4 Press RECEIVE and set up the display as shown below



5 Connect the HP 37717C Unbalanced 75Ω SIGNAL OUT port to the HP 37717C Unbalanced 75Ω SIGNAL IN port.

6 Connect a probe from the Oscilloscope 10kΩ pod to TP20.

7 Set the Oscilloscope to 20 usec/Div Timebase and 500 mV/Div sensitivity.

8 Adjust R4 until the waveform displayed on the Oscilloscope is at minimum amplitude.

9 Connect a probe from the Oscilloscope 10 kΩ pod to TP12.

10 Set the Oscilloscope to 1 usec/Div Timebase and 500 mV/Div sensitivity.

11 Re-adjust R4 until the narrow pulse displayed on the Oscilloscope is at minimum amplitude - only a small adjustment should be required.

12 Set the Oscilloscope to 1 usec/Div Timebase and 100 mV/Div sensitivity with 0 V DC offset.

13 Adjust R2 until the narrow pulse displayed on the Oscilloscope has 0 volts DC offset.

Automatic Rx Calibration

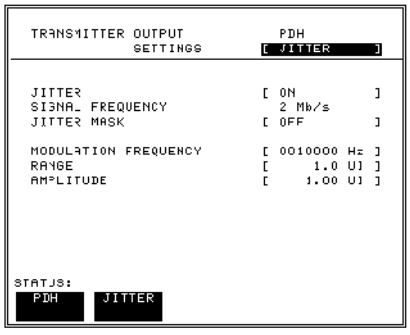
1 Set the CALIBRATION ITEM to JITTER RX.

2 Press RUN/STOP to start calibration. Calibration is automatic and takes about 30 minutes. When complete, the display will indicate CALIBRATION PROCESS COMPLETE.

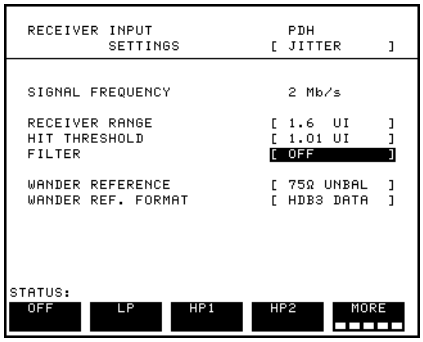
3 Press any key to return to normal operation.

Jitter Hits Threshold

1 Press TRANSMIT and set up the display as shown below.



2 Press RECEIVE and set up the display as shown below.



3 Adjust R1 until the Jitter Hits LED on the HP 37717C Front Panel is just extinguished.

4 Set the HIT THRESHOLD on the Jitter Receive display to 1.00 UI and ensure that the Jitter Hits LED on the HP 37717C Front Panel is lit.

Demodulated Jitter Output Amplitude

1 Connect the HP 37717C Demodulated Jitter Output to the 50Ω input on the Oscilloscope.

2 Adjust R68 until the amplitude of the displayed waveform is 353 mV RMS as measured on the Oscilloscope.

Wander Reference Recovered Clock

CAUTION The following adjustment requires data to be written directly to the Jitter Tx hardware. **Take great care to select the correct address before writing data.**

1 Make the following key sequence on the HP 37717C to obtain the special DEBUG FUNCTION display. Press OTHER, ⇦⇧, MORE, ⇦⇧, MORE ⇦⇧, MORE and OTHER. Press MORE until DEBUG FUNCTION appears in the softkey menu.

2 Press DEBUG FUNCTION and select WRITE TO H/W on the Display or if firmware revision is 3448 and above, select MODULE DEBUG then MODULE GENERAL then WRITE TO H/W.

3 Set the ADDRESS to SINGLE WRITE then move the cursor to the address field and select the address as follows:

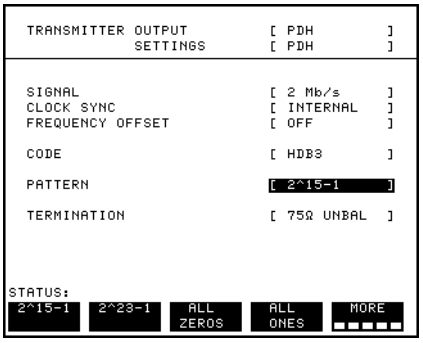
CAUTION Take great care to select the correct address before writing data.

Jitter Transmitter Module Position in the Mainframe	Address Code
Slot 2 (If SDH Option NOT fitted)	D20012
Slot 4 (If SDH Option fitted)	D40012

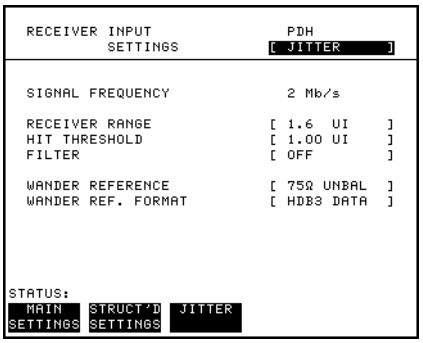
4 Move the cursor to the DATA field and set the data to 0000000000000001

5 Move the cursor to the TOGGLE TO WRITE TO H/W field and set to WRITE H/W. The jitter transmitter modulation will now be switched off.

6 Press TRANSMIT and set up the display as shown below



7 Press RECEIVE and set up the display as shown below



8 Connect the HP 37717C Unbalanced 75Ω SIGNAL OUT port to the Unbalanced 75Ω SIGNAL IN port and the Unbalanced 75Ω TIMING REF INPUT simultaneously using a T-piece.

9 Connect a probe from the Oscilloscope 10kΩ pod to TP10.

10 Adjust L21 until the waveform displayed on the Oscilloscope has minimum jitter.

11 Switch the HP 37717C off then on again to return the Debug Page parameter to default settings.

STM Line Jitter Receiver (Options A3L and A3M)

Adjustment Reference

Recover Clock	**A18R159**
Wander Reference Recovered Clock	**A18L9**

NOTE The following adjustments require the instrument to be fitted with known good PDH Rx and Tx, Jitter Generation Card, SDH Module and Line Jitter Receiver.

Description

Recover Clock - R159 is adjusted to produce a Flat Trace at Demo Jitter O/P when connected to an Oscilloscope.

Wander Reference Recovered Clock L9 is adjusted for minimum jitter seen on TP8 signal using an Oscilloscope.

Equipment Required

Oscilloscope	**HP 54520A**
10kΩ Oscilloscope Pod	**HP 54001A**
50Ω Oscilloscope Pod	**HP 54002A**
75/50Ω matching Pad	**HP 11852B**
Module board Extender Card (2)	**HP 37714-60099**

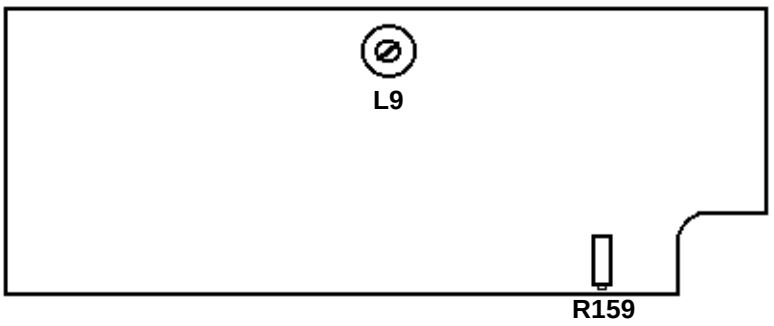


Figure 3-19 A18 Jitter Receiver Assembly

Pre-Adjustment Setup

Before carrying out any adjustment to the HP 37717C Jitter Receiver Module, perform the following pre-adjustment setup.

CAUTION This procedure uses the special MODULE DEBUG display on the HP 37717C. When using the MODULE DEBUG display, ONLY modify parameters shown. Altering other parameters can damage instrument firmware - exit the Debug Display after setup to prevent accidental damage.

1. Press the [OTHER] key then the **SETTINGS CONTROL** softkey.
2. Set the Transmitter and Receiver to COUPLED.
3. Make the following key sequence on the HP 37717C to obtain the special MODULE DEBUG display. Press [OTHER], [⇦], **MORE**, [⇦], **MORE**, [⇦], **MORE**, [OTHER]. Press **MORE** until **MODULE DEBUG** appears in the softkey menu.
4. Press **MODULE DEBUG** then select MODULE PDH MODULE .
5. Set the VCO CONTROL MODE to FIXED on the PDH MODULE DEBUG Display.
6. Set the MODULE to JITTER MODULE on the MODULE DEBUG Display.
7. Set the TX CALIBRATION to OFF on the Jitter MODULE DEBUG Display.
8. Set the RX CALIBRATION to OFF on the Jitter MODULE DEBUG Display.

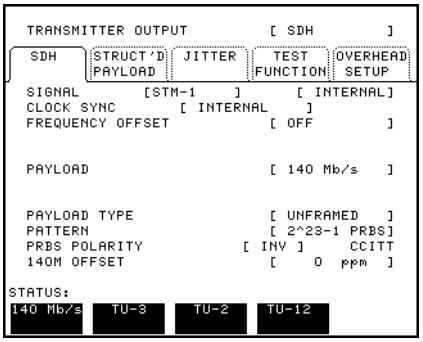
CAUTION The above sequence must be performed each time power is cycled on the HP 37717C, as all **MODULE DEBUG** parameters will adopt DEFAULT values when power is cycled.

Procedure

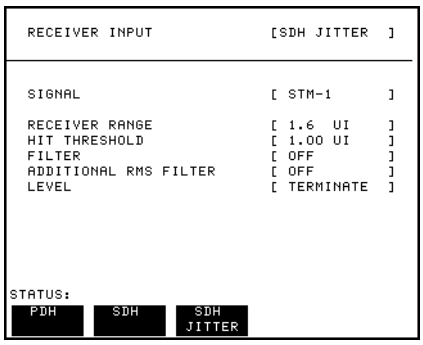
Recovered Clock

1. Press [TRANSMIT] and set up the display as shown below.

.



2 Set the and Receiver to SDH Jitter as shown below.



3 Connect the SDH Tx O/P to the STM-Ie I/P.

4 Connect the Demo Jitter O/P to the 75Ω Oscilloscope I/P.

5 Adjust R159 until the Demo Jitter O/P is a flat trace.

Wander Reference Recovered Clock

CAUTION The following adjustment requires data to be written directly to the Jitter Tx hardware. **Take great care to select the correct address before writing data.**

1 Make the following key sequence on the HP 37717C to obtain the special DEBUG FUNCTION display. Press OTHER, ⇧, MORE, ⇧, MORE, ⇧, MORE and OTHER. Press MORE until DEBUG FUNCTION appears in the softkey menu.

2 Press DEBUG FUNCTION and select WRITE TO H/W on the Display or if firmware revision is 3448 and above, select MODULE DEBUG then MODULE GENERAL then WRITE TO H/W.

3 Select ADDRESS [SINGLE WRITE] then move the cursor to the address field and select the address as follows:

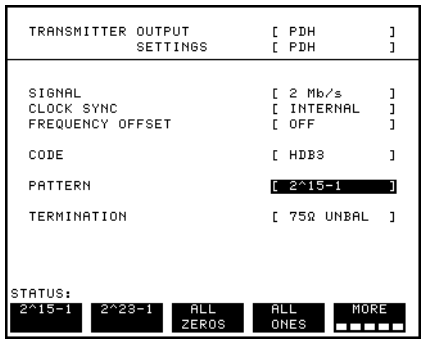
CAUTION Take great care to select the correct address before writing data.

Jitter Transmitter Module Position in the Mainframe	Address Code
Slot 4	D40012

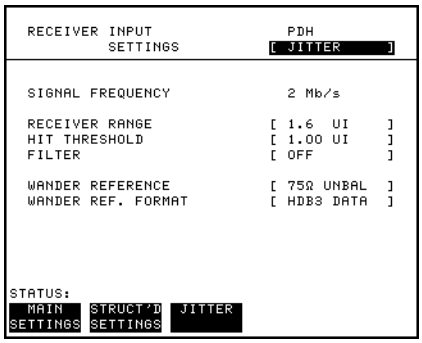
4 Move the cursor to the DATA field and set the data to 0000000000000001

5 Move the cursor to the TOGGLE TO WRITE TO H/W field and set to WRITE H/W. The jitter transmitter modulation will now be switched off.

6 Press TRANSMIT and set up the display as shown below.



7 Press RECEIVE and set up the display as shown below.



8 Connect the HP 37717C Unbalanced 75Ω SIGNAL OUT port to the Unbalanced 75Ω SIGNAL IN port and the Unbalanced 75Ω TIMING REF INPUT simultaneously using a T-piece.

9 Connect a probe from the Oscilloscope 10kΩ pod to A15TP8.

10 Adjust A15L9 until the waveform displayed on the Oscilloscope has minimum jitter.

11 Switch the HP 37717C off then on again to return the Debug Page parameter to default settings.

STM Line Jitter Receiver (Options AIM, AIN and AIP)

Adjustment Reference

False Lock Set	**R40**
Jitter Hits Level	**R31**
Demo Jitter Output	**R3**

NOTE The following adjustments require the instrument to be fitted with known good PDH Rx and Tx, Jitter Generation Card, SDH Module and Line Jitter Receiver.

Description

False Lock Set - R40 is adjusted to give 2.00 V DC ±0.01 at TP13.

Jitter Hits Level - R31 is adjusted until the jitter hits LED is just off.

Demo Jitter Output - R3 is adjusted until the 10 kHz signal is at an amplitude of 353 mV ±5 mV.

Equipment Required

Oscilloscope	**HP 54520A**
10kΩ Oscilloscope Pod	**HP 54001A**
75/50Ω Matching Pad	**HP 11852B**
Module board Extender Card (2)	**HP 37714-60099**

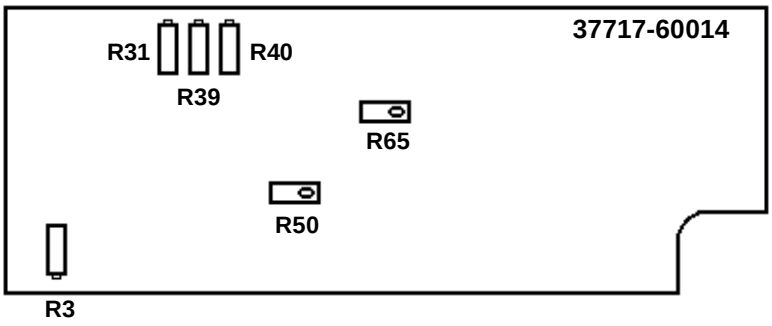


Figure 3-20 A14 STM Jitter Receiver Assembly

Pre-Adjustment Setup

Before carrying out any adjustment to the HP 37717C Jitter Receiver Module, perform the following pre-adjustment setup.

CAUTION This procedure uses the special MODULE DEBUG display on the HP 37717C. When using the MODULE DEBUG display, ONLY modify parameters shown. Altering other parameters can damage instrument firmware - exit the Debug Display after setup to prevent accidental damage.

1. Press the [OTHER] key then the **SETTINGS CONTROL** softkey.
2. Set the Transmitter and Receiver to COUPLED.
3. Make the following key sequence on the HP 37717C to obtain the special MODULE DEBUG display. Press [OTHER], [⇧], **MORE**, [⇧], **MORE**, [⇧], **MORE** and [OTHER]. Press **MORE** until **MODULE DEBUG** appears in the softkey menu.
4. Press **MODULE DEBUG** and then set MODULE to PDH MODULE.
5. Select VCO CONTROL MODE [FIXED] on the PDH MODULE DEBUG Display.
6. Select MODULE [JITTER MODULE] on the MODULE DEBUG Display.
7. Select TX CALIBRATION [OFF] on the Jitter MODULE DEBUG Display.
8. Select RX CALIBRATION [OFF] on the Jitter MODULE DEBUG Display.

CAUTION The above sequence must be performed each time power is cycled on the HP 37717C, as all MODULE DEBUG parameters will adopt DEFAULT values when power is cycled.

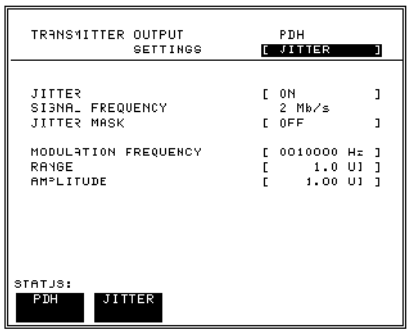
Procedure

False Lock Set

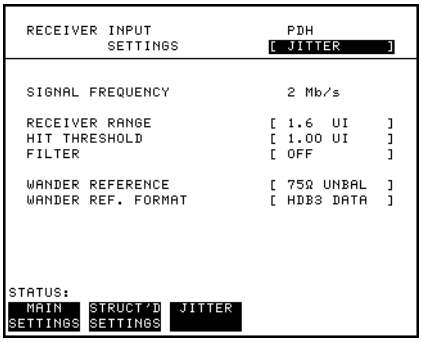
1. Monitor TP13 on Oscilloscope and adjust R40 to give 2.00 V ±0.01 V DC.

Jitter Hits Level

1. Connect PDH 75Ω to IN ports using a 75Ω coaxial cable.
2. Set [TRANSMIT] as shown below.



3 Set [RECEIVE] as shown below.



4 Adjust R31 until the Jitter Hits LED on the HP 37717C Front Panel is just extinguished.

5 Set the HIT THRESHOLD on the Jitter Receiver display to 1.00 UI and ensure that the Jitter Hits LED on the HP 37717C Front Panel is lit.

Demodulation Jitter Output Amplitude

1 Keep the settings the same as for the previous set up, and connect the Demod Output to the Oscilloscope via a 50Ω Oscilloscope pod.

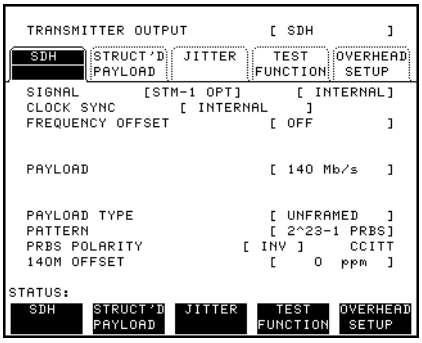
2 Adjust R3 until the 10 kHz signal seen has an RMS amplitude of 353 mV ±5 mV.

STM 1o Clock Recovery (Options A1N and A1P)

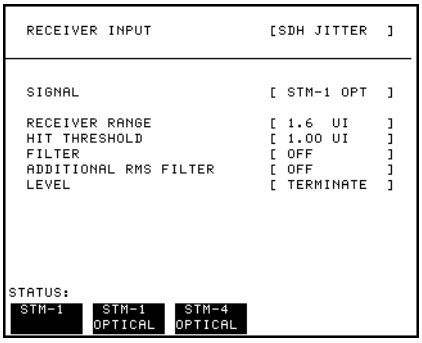
NOTE Do not connect any cables to the Optical Input of the Line Jitter Module.

Procedure

1 Press TRANSMIT and set the display as shown below.



2 Press RECEIVE and set to SDH Jitter as shown below.



3 Press OTHER, MORE, MORE then select CALIBRATION.

4 Enter the password 1243 and select STM10 J1 REC CLK.

5 Press RUN.

6 Increment/Decrement the DAC value shown until a value of 155.52 MHz is read on the Front Panel.

WARNING **Failure to do this could result in damage to the instrument.**

7 Connect the HP 37717C Optical Output on the STM1/4 Optical Module to the Optical Input on the STM1/4 Jitter Receiver Module.

8 Connect the Demod Jitter 75Ω Output to the Spectrum Analyzer via the 75/50Ω Matching Pad.

9 Set the Spectrum Analyzer as follows:

Start Point : 10 KHz	Stop Point : 3.0 MHz
Reference Level 0dBm	Sweep Time 1.0 seconds
Video Bandwidth 1kHz	Resolution Bandwidth 100 Hz

10 Move the cursor to DAC value (**use only the last two digits**) until the Noise Floor (neglecting spikes) displayed on the Spectrum Analyzer is at a minimum.

11 Ensure the Jitter Unlock led is **not** lit.

12 Press RUN/STOP key to stop gating **- this is necessary to store the new DAC value**.

13 Press RESULTS key, select [JITTER] and [CUMULATIVE].

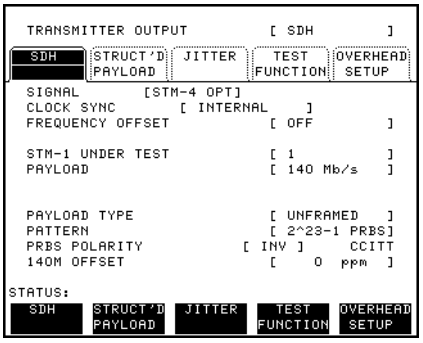
14 Select [MANUAL] gating mode then press RUN/STOP to start a measurement of intrinsic Jitter. Ensure the measured intrinsic Jitter is less than or equal to 0.04 UI after 30 seconds. Repeat steps 3 to 12 if the intrinsic reading is too high.

STM 4o Clock Recovery (Option AIP)

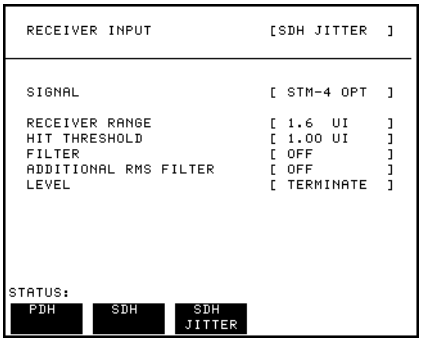
NOTE Do not connect any cables to the Optical Input of the Line Jitter Module.

Procedure

1 Press TRANSMIT and set the display as shown below. :



2 Press RECEIVE and set to SDH Jitter as shown below.



3 Press OTHER, MORE, MORE, and then CALIBRATION.

4 Enter the password 1243 and select STM4o J1 REC CLK.

5 Press RUN.

6 Increment/Decrement the DAC value shown until a value of 622.08 MHz is read on the Front Panel.

CAUTION If option URU is fitted, the Optical Output must be attenuated by 10 dB before connecting to the Optical Input on the Jitter Receiver Module. Failure to do this could result in calibration failure.

CAUTION Failure to do this could result in damage to the instrument.

7 Connect the HP 37717C Optical Output on the STM1/4 Optical Module to the Optical Input on the STM1/4 Jitter Receiver Module.

8 Connect the Demod Jitter 75Ω Output to the Spectrum Analyzer via the 75/50Ω Matching Pad.

9 Set the Spectrum Analyzer as follows:

Start Point : 10 KHz	Stop Point : 3.0 MHz
Reference Level 0dBm	Sweep Time 1.0 seconds
Video Bandwidth 1kHz	Resolution Bandwidth 100 Hz

10 Move the cursor to DAC value (**use only the last two digits**) until the Noise Floor (neglecting spikes) displayed on the Spectrum Analyzer is at a minimum.

11 Ensure the Jitter Unlock led is **not** lit.

12 Press RUN/STOP key to stop gating **- this is necessary to store the new DAC value**.

13 Press RESULTS key, select [JITTER] and [CUMULATIVE].

14 Select [MANUAL] gating mode then press RUN/STOP to start a measurement of intrinsic Jitter. Ensure the measured intrinsic Jitter is less than or equal to 0.04 UI after 30 seconds. Repeat steps 3 to 12 if the intrinsic reading is too high.

Jitter Receiver (Options A3L, A3M, A3N, A3P, A3V and A3W)

This chapter describes the setup procedure for part of the following modules:

1 A3L - 37717-60110

2 A3M - 37717-60111

3 A3N - 37717-60112

4 A3P - 37717-60113

5 A3V - 37717-60134

6 A3W - 37717-60135

In order to setup the jitter receiver card the test chassis must be fitted with known good PDH Rx and Tx cards, Jitter Generator card, SDH module and STM1e Clock Recovery card.

i.e. 37714-60006 (or 37717-60004), 37714-60007 (or 37717-60005), 37717-60008, 37714-60039, 37714-60101 and 37717-60015/16/17

Pre-Adjustment Setup

The following must be set on the front panel before any adjustments can be attempted on this card.

1 Place the 37717-60122 card under test on extender card.

2 Set PDH Transmitter and Receiver settings to coupled by selecting:

OTHER

SETTINGS CONTROL

COUPLED

3 The MODULE DEBUG page must be used to control the following settings, it can be found by using the following key sequence:

OTHER, ⇧, MORE, ⇧, MORE, ⇧, MORE, OTHER, MORE, MORE,

MODULE DEBUG.

4 Set the PDH VCO control to fixed by selecting:

MODULE, PDH MODULE

VCO CONTROL MODE, FIXED

5 Set the Jitter Tx and Rx calibration off by selecting:

MODULE, JITTER MODULE

TX CALIBRATION, OFF

RX CALIBRATION, OFF

WARNING **All the debug functions set above will be reset if the instrument is power cycled, so this preparation procedure will have to be repeated every time the instrument has to be powered down, (e.g. if a card is moved on or off the extender card).**

Procedure

Measurement Loop Offset

1 Connect the PDH 75Ω OUT and 75Ω IN ports using a 75Ω coaxial cable.

2 Set the PDH 2 Mb/s data to ALL ONES pattern by selecting:

TRANSMIT

SETTINGS, PDH

SIGNAL, 2 Mb/s

PATTERN, ALL ONES

3 Set the Jitter Transmit Off by selecting:

TRANSMIT

SETTINGS, JITTER

JITTER, OFF

4 Set the Jitter Receiver to 1.6 UI, Filters Off by selecting:

RECEIVE

SETTINGS, JITTER

RECEIVER RANGE, 1.6 UI

FILTER, OFF

5 Monitor TP13 on an HP 54520A Oscilloscope using 10kΩ pod (54001A).

6 Set the Oscilloscope to 20 usec/div timebase and 500 mV/div sensitivity.

7 A sawtooth waveform should be observed, adjust R157 until this waveform is at a minimum.

NOTE Adjusting past the minimum will cause the slope of the sawtooth to change.

8 Monitor TP11, set Oscilloscope to 1usec/div, re-adjust R157 until the displayed narrow pulse amplitude is at a minimum (ideally 0 mV but less than 100 mV in any polarity).

NOTE This should only require a small adjustment to R157.

9 Set the Oscilloscope to 100 mV/div sensitivity and 0 V offset.

10 Adjust R120 until the displayed waveform has 0 V D.C. offset.

Narrowband Detector Leakage

1 Apply a jitter level of 0.6 UI at 140 Mb/s data rate with 4 MHz modulation as follows:-

TRANSMIT

SETTINGS, PDH

SIGNAL, **140 Mb/s**

PATTERN, **PRBS23**

SETTINGS, **JITTER**

JITTER, **ON**

MODULATION FREQUENCY, **4 MHz**

RANGE, **1.0 UI**

AMPLITUDE, **0.6 UI**

2 Set up DDS frequency as follows:
MODULE DEBUG, **JITTER MODULE**, **TYPE**, **TRANSFER**, **FREQ DEBUG**, **ON**, **FREQ**, **3 MHz**.

3 Monitor TP6 on the Spectrum Analyzer using a 1:1 probe, HP 10438A. Set as follows:
CENTRE FREQ: **4 MHz**

SPAN: **8 MHz**

VIDEO BANDWIDTH: **300 Hz**

4 Adjust R73 and R54 until the 3M and 4M signals are at minimum amplitude.

Jitter Hits Threshold

1 Apply a jitter level of 1.0 UI at 2 Mb/s data rate with 10 kHz modulation by selecting:
TRANSMIT

SETTINGS, **JITTER**

JITTER, **ON**

MODULATION FREQUENCY, **10000 Hz**

RANGE, **1.0 UI**

AMPLITUDE, **1.0 UI**

2 Set the the hits threshold on the Jitter Rx to 1.01 UI by selecting:
RECEIVE

SETTINGS, **JITTER**

HIT THRESHOLD, **1.01 UI**

3 Monitor the Jitter Hits LED on the front panel and adjust R76 until the Jitter Hits LED just goes out.

4 Set the receive jitter hits threshold to 1.00 UI and check that the Jitter Hits LED lights.

Demod Jitter Output

1 Keep the settings the same as for the previous setup. Connect J1 to Digital Voltmeter using BNC cable and a BNC to Banana adaptor.

2 Adjust R2 until the 10 kHz signal seen has an RMS amplitude of 353 mV ± 5 mV (1 V pk-pk).

Main Lock Detect

1 Measure the voltage on TP14 using a Digital Voltmeter.

2 Adjust R79 for 4.2 Vdc.

Jitter Amplitude Check

1 Turn the RMS filter off by selecting:

RECEIVE

ADDITIONAL RMS FILTER | OFF

2 display the jitter amplitude by selecting:

RESULTS

RESULTS, JITTER

ERROR SOURCE, AMPLITUDE

3 Press the RUN/STOP key and check that the positive and negative peaks are 0.5 UI ±0.1 UI.

4 Check that the RMS value is 0.353 UI ±0.10 UI.

5 Press the RUN/STOP key to stop the measurement, and check against the same limits for the 8, 34 and 140 Mb/s rates by selecting:

TRANSMIT

SETTINGS, PDH

SIGNAL, 8 Mb/s, | 34 Mb/s or | 140 Mb/s

140M Jitter Intrinsics Check

1 Turn the Jitter Transmitter off by selecting:

TRANSMIT JITTER OFF

2 Display the Jitter Amplitude by selecting:

RESULTS

RESULTS, JITTER

ERROR SOURCE, AMPLITUDE

Gate for 10 seconds and check that the pk-pk amplitude is less than 0.08 UI.

Jitter Hits Verification

1 Apply a jitter level of 1.0 UI at 2 Mb/s data rate with 10 kHz modulation by selecting:

TRANSMIT

SETTINGS, JITTER

JITTER, ON

MODULATION FREQUENCY, 10000 Hz

RANGE, 1.0 UI

AMPLITUDE, 1.00 UI

2 Adjust the receive jitter hits level to 0.75 UI by selecting:

RECEIVE

SETTINGS, JITTER

HIT THRESHOLD, 0.75 UI I

3 Display the jitter hits count by selecting:

RESULTS

RESULTS, JITTER

ERROR SOURCE, HITS

4 Set the results gating time to one second by selecting:

RESULTS

TEST TIMING, SINGLE

Enter the field which says 1 HOUR, and adjust to USER PROGRAM.

Set to 1 SECS.

5 Press the RUN/STOP key and check that the displayed Hit Count is 20000 $\pm$ 1000.

6 Repeat steps 1 to 6 for 8, 34 and 140 Mb/s data rates.

STM-1 Jitter Measurement Check

1 Reset the Unit Under Test Transmitter and Receiver by selecting:

OTHER STORED SETTINGS ACTION RECALL

2 Set the SDH Transmitter as follows:

TRANSMIT

SDH

SETTINGS, JITTER

JITTER, ON

MODULATION FREQUENCY, 10000 Hz

RANGE, 1.0 UI

AMPLITUDE, 1.00 UI

3 Set the Receiver to SDH Jitter as follows:

RECEIVE

SDH JITTER

4 Connect the SDH Transmitter output to the STM1e input (J2) on the 37717-60016 board.

5 On the RESULTS page, select JITTER and SHORT TERM, 1 SEC. Start the instrument gating, the displayed jitter should be 0.5 UI ± 0.1 UI for both positive and negative peaks.

STM-1 Jitter Intrinsics Check

1 Reset the Unit Under Test Transmitter and Receiver by selecting:

OTHER, STORED SETTINGS, ACTION RECALL

2 Set the SDH Transmitter as follows:

TRANSMIT

SDH

SETTINGS, JITTER

JITTER, OFF

3 Set the Receiver to SDH Jitter as follows:

RECEIVE

SDH JITTER

4 Connect the SDH Transmitter output to the STM1e input (J2) on the HP 37717-60016 board.

5 On the RESULTS page, select JITTER and Cumulative, and gate for 10 Seconds. The displayed jitter should be < 0.1 UI.

Structured PDH Transmitter (Options UKJ, USA)

A17 SPDH Transmitter Assembly.

Adjustment Reference

CMI Tx Pulse Amplitude	**A17R39**
CMI Tx Mark:Space Ratio	**A17R47 and A17 R55**
Ternary Pulse Amplitude (positive)	**A17R46**
Ternary Pulse Amplitude (negative)	**A17R54**

Description

A frequency counter is used to measure the recovered clock frequency at all rates. The recovered clock frequency rates are then adjusted to be within specification.

Equipment Required

Oscilloscope	**HP 54520A**
75/50Ω Matching Pad	**HP 11852B**
Extender Card Assembly	**HP 37714-60099**
Frequency Counter	**HP 5335A Option 010**
75 Ohm Termination	**HP 1522-80010**
T Connector	**HP 1250-0781**

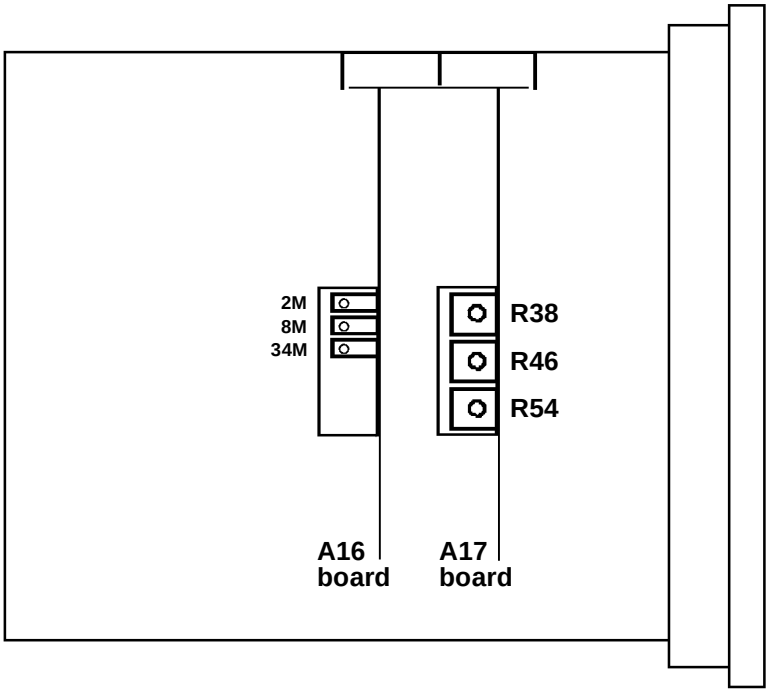


Figure 3-21 SPDH Tx Module (topside) Adjustable Components

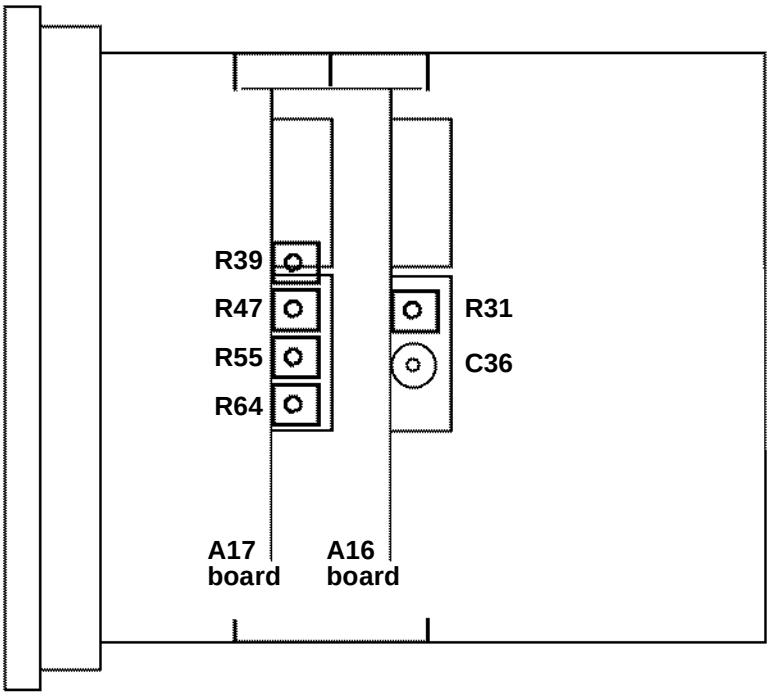


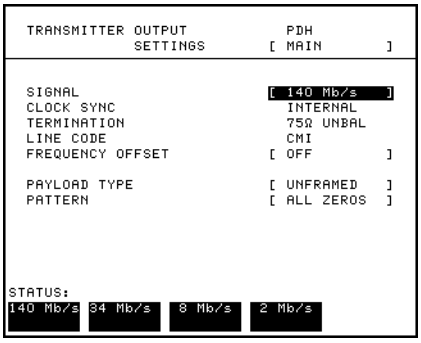
Figure 3-22 PDH Tx Module (underside) Adjustable Components

Procedure

CMI Pulse Amplitude

1 Recall the HP 37717C Default settings as shown on page 3-7.

2 Press TRANSMIT and setup the display as shown below.



3 Connect the HP 37717C Unbalanced 75Ω SIGNAL OUT port to the Oscilloscope INPUT 1 via the 75/50Ω Matching Pad - set the Oscilloscope termination to 50Ω

4 Set the Oscilloscope Channel 1 Probe Attenuation factor to X 2.40 (equivalent to 7.6 dB) to compensate for the Matching Pad attenuation.

5 Press AUTOSCALE on the Oscilloscope and adjust the timebase and Delay to display a CMI pulse as shown;

6 Using the Oscilloscope, measure the amplitude of this pulse at it's peak.

7 Adjust A17R39 to obtain a maximum pulse amplitude of 1 Volt pk-pk.

CMI Pulse Mark:Space Ratio

8 Using the Oscilloscope, measure the pulse Mark to Space Ratio.

9 Adjust A17R55 to obtain a Mark to Space Ratio of 1:1.

10 Set the Transmitter to PATTERN to ALL ONES on the HP 37717C.

11 Set the Oscilloscope Timebase to 2 nS/Division.

12 Using the Oscilloscope, measure the pulse Mark to Space Ratio.

13 Adjust A17R47 to obtain a Mark to Space Ratio of 1:1.

14 Return the HP 37717C to PATTERN [ALL ZEROS] and the Oscilloscope timebase to 1 ns/Division.

15 Re-adjust A17R55 to bring the Mark to Space Ratio back to 1:1.

16 Repeat steps 10 to 15 until no further adjustment of A17R55 and A17R47 is required.

Ternary Pulse Amplitude

17 Set the BIT RATE to 2 Mb/s and PATTERN to ALL ONES on the HP 37717C.

18 Press AUTOSCALE on the Oscilloscope and adjust the Timebase and Delay to position the positive ternary pulse in the centre of the screen.

19 Using the Oscilloscope, measure the amplitude of this pulse at it's peak.

20 Adjust A17R46 to obtain a maximum positive pulse amplitude of 2.46 Volts.

21 Adjust the Oscilloscope Timebase and Delay to position the negative ternary pulse in the centre of the screen.

22 Using the Oscilloscope, measure the amplitude of this pulse at it's peak.

23 Adjust A17R54 to obtain a maximum negative pulse amplitude of 2.46 Volts.

Structured PDH Receiver (Options UKJ, USA)

A16 SPDH Receiver Assembly.

Adjustment Reference

2048 kHz Recovered Clock frequency	**A16R30**
8448 kHz Recovered Clock frequency	**A16R38**
34368 kHz Recovered Clock frequency	**A16R46**
139,264 kHz Recovered Clock frequency	**C154**

Description

These adjustments are performed using a special HP 37717C Calibration Item. This item measures and displays the free-run Recovered Clock frequency at each bit rate, allowing adjustment to be made within specified limits.

NOTE This Calibration Item is only valid if the 10 MHz Reference Clock Frequency and VCXO Calibration procedure has been performed.

Equipment Required

Extender Card Assembly	**HP 37714-60099**

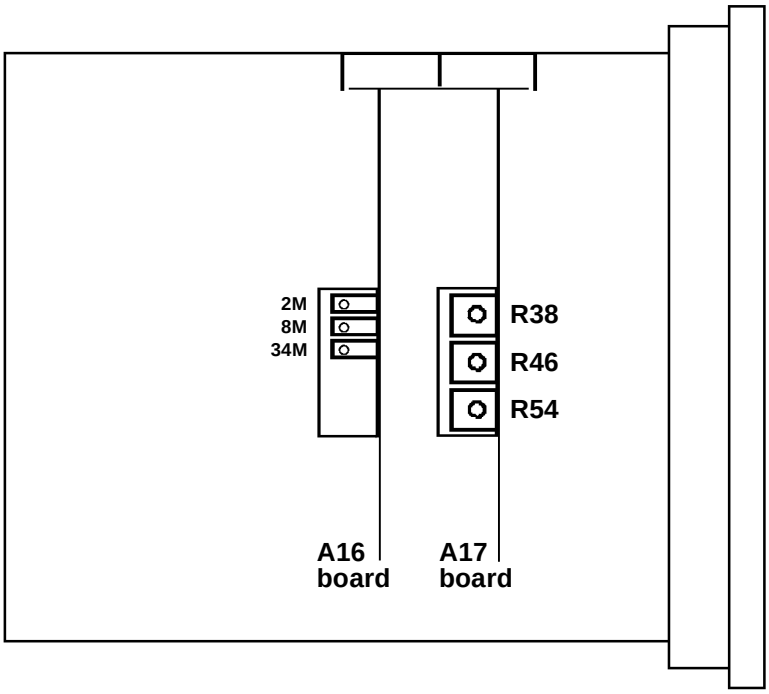


Figure 3-23 SPDH Rx Module (topside) Adjustable Components

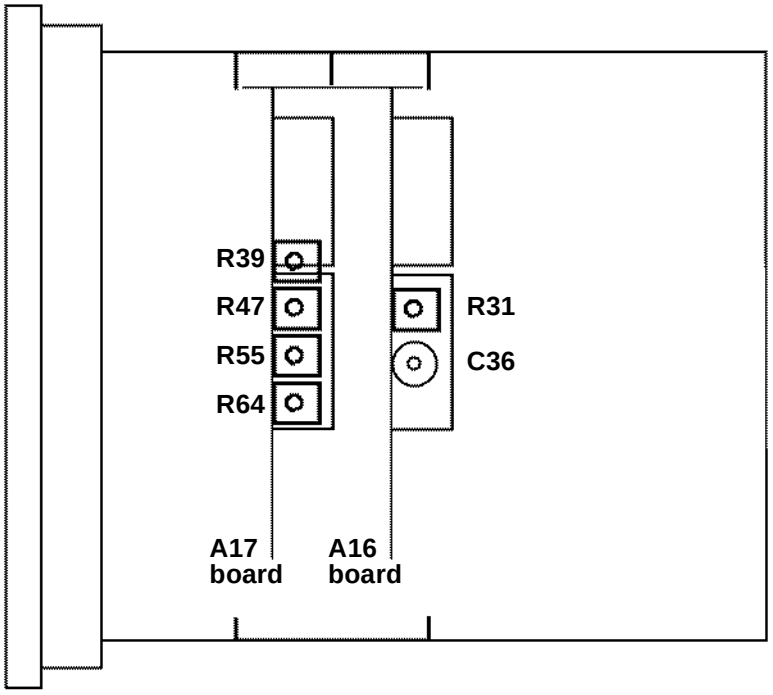


Figure 3-24 SPDH Rx Module (underside) Adjustable Components

Procedure

34 Mb/s Recovered Clock frequency

1 Select the Calibration Subtest No. function on the OTHER display.

2 Select CALIBRATE PASSWORD and using the DECREASE DIGIT and INCREASE DIGIT softkeys, set the password to 1243.

3 Set the CALIBRATION ITEM to CLOCK EXTRACT and SELECTED RATE to 34 Mb/s.

4 Press the RUN/STOP key.

5 Adjust A16R46 (34M) to obtain a displayed TARGET FREQUENCY between 34361200 Hz and 34374800 Hz.

6 Once set, press the RUN/STOP key.

140 Mb/s Recovered Clock frequency

7 Set the CALIBRATION ITEM to CLOCK EXTRACT and SELECTED RATE to 140 Mb/s.

8 Press the RUN/STOP key.

9 Adjust A16C36 (139M) to obtain a displayed TARGET FREQUENCY between 139236147 Hz and 139291853 Hz.

10 Once set, press the RUN/STOP key.

NOTE The remaining Clock Recovery adjustments can only be performed with the PDH Module fitted on a special extender card.

NOTE When removing the Module to use the Extender Card, you MUST follow the procedure in G15 Dismantling and Re-assembly Procedures.

2 Mb/s Recovered Clock frequency

11 Set the CALIBRATION ITEM to CLOCK EXTRACT and SELECTED RATE to 2 Mb/s.

12 Press the RUN/STOP key.

13 Adjust A16R30 (2M) to obtain a displayed TARGET FREQUENCY between 2047590 Hz and 2048410 Hz.

14 Once set, press the RUN/STOP key.

8 Mb/s Recovered Clock frequency

15 Set the CALIBRATION ITEM to CLOCK EXTRACT and SELECTED RATE to 8 Mb/s.

16 Press the RUN/STOP key.

17 Adjust A16R38 (8M) to obtain a displayed TARGET FREQUENCY between 8446310 Hz and 8449690 Hz.

18 Once set, press the RUN/STOP key.

Multiple Outputs (Option UHC)

A14 Multiple Outputs Assembly and A7 with an Unstructured PDH Module fitted or A17 with a Structured PDH Module fitted.

Adjustment Reference

VCO Duty Cycle (Unstructured PDH Module fitted)	**A7R189**
VCO Duty Cycle (Structured PDH Module fitted)	**A17R38**
CMI Tx Pulse Amplitude (Output 2)	**A14R8**
CMI Tx Pulse Amplitude (Output 3)	**A14R10**
CMI Tx Pulse Amplitude (Output 4)	**A14R12**
Ternary Amplitude (Output 1)	**A14R2, R3**
Ternary Amplitude (Output 2)	**A14R4, R5**
Ternary Amplitude (Output 3)	**A14R6, R7**

Description

An Oscilloscope is connected to Output 1 on the Multiple Output Module via 75/50Ω Matching Pad and the waveform is adjusted for 50% Duty Cycle using A7R189 (Unstructured PDH) or A17R38 (Structured PDH).

Each of the 3 additional outputs on the Multiple Output Module is adjusted for correct 140 Mb/s CMI amplitude using R8, R10 and R12.

Equipment Required

Oscilloscope	**HP 54520A**
75/50Ω Matching Pad	**HP 11852B**
Extender Card Assembly	**HP 37714-60099**

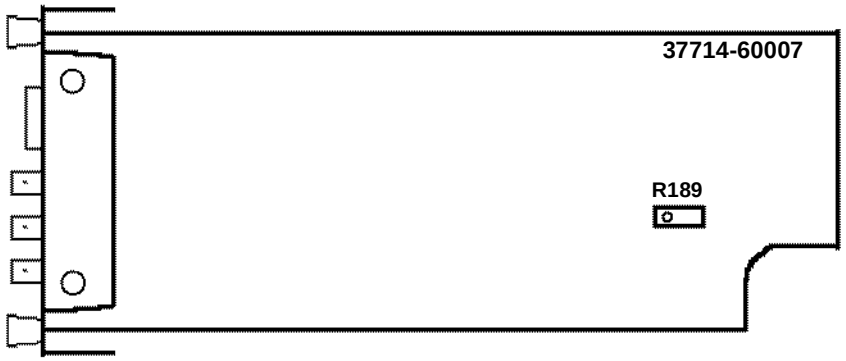


Figure 3-25 Unstructured PDH Assembly Adjustable Components

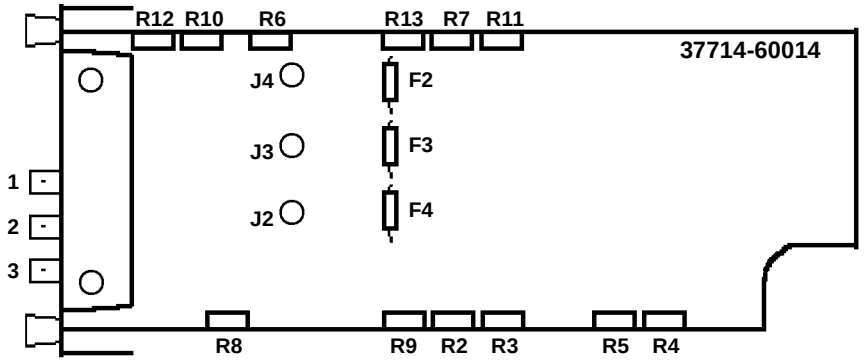


Figure 3-26 Multiple Outputs Assembly Adjustable Components

Procedure

VCO Duty Cycle

1 Fit the PDH Transmitter board (A7 or A17) on the extender card.

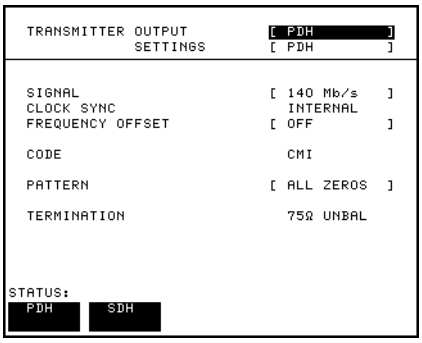
NOTE If PDH Unstructured Transmitter is fitted, it will be necessary to separate the A6 and A7 board Assemblies to gain access to A7R189.

2 Connect the Oscilloscope to A14 J2 via the 75/50Ω Matching Pad - set the Oscilloscope termination to 50Ω and Probe Attenuation factor to X 2.40 (equivalent to 7.6 dB) to compensate for the Matching Pad attenuation.

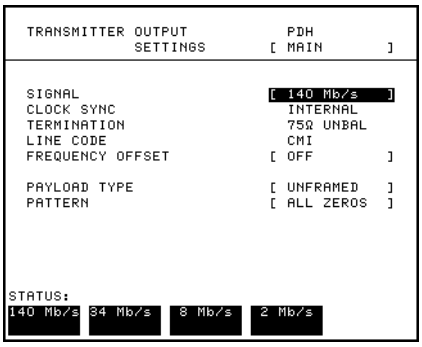
3 Recall the HP 37717C Default settings as shown on page 3-7.

4 Press TRANSMIT and set up the display as shown.

Unstructured PDH fitted



Structured PDH fitted



5 Press AUTOSCALE on the Oscilloscope and adjust the timebase and Delay to display a CMI pulse.

6 Adjust A7R189 (Unstructured PDH Module fitted) or A17 R38 (Structured PDH Module fitted) to obtain a clean waveform with 50% Duty Cycle.

CMI Pulse Amplitude 1

7 Replace the PDH Module in the instrument and fit the A14 Multiple Outputs board on the extender card.

8 Using the Oscilloscope, measure the amplitude of the A14 Output1 pulse at its peak.

9 Adjust A14R8 to obtain a maximum pulse amplitude of 1 Volt pk-pk.

10 Connect the Oscilloscope to A14 Output 2 via the 75/50Ω Matching Pad.

11 Adjust A14R10 to obtain a maximum pulse amplitude of 1 Volt pk-pk.

12 Connect the Oscilloscope to A14 Output 3 via the 75/50Ω Matching Pad.

13 Adjust A14R12 to obtain a maximum pulse amplitude of 1 Volt pk-pk.

Ternary Pulse Amplitude

14 Select BIT RATE (704 kb/s) and PATTERN (ALL ONES) on the HP 37714A / HP 37717C.

15 Press AUTOSCALE on the Oscilloscope and adjust the Timebase and Delay to position the positive ternary pulse in the centre of the screen.

16 Using the Oscilloscope, measure the peak amplitude of this pulse.

17 Adjust A14R6 to obtain a maximum positive pulse amplitude of 2.37 Volts.

18 Adjust the Oscilloscope Timebase and Delay to position the negative ternary pulse in the centre of the screen.

19 Using the Oscilloscope, measure the peak amplitude of this pulse.

20 Adjust A14R7 to obtain a maximum negative pulse amplitude of 2.37 Volts.

21 Repeat Steps 14 to 20 for A14 Outputs 1 and 2. Adjust A14R2 and R3 (Output 1) and R4 and R5 (Output 2) as required.

ATM Cell Layer Transmitter (Option UKZ)

This section describes the setup procedure for the following modules:

37717-60019 (Option UKZ Transmit)

NOTE A 37717-60081 Option UKZ Receive module MUST be fitted in the slot directly to the right of the board under test. An A1T module MUST be fitted to the left of the UKZ Transmitter.

Procedure For Ternary Pulse Amplitude

34 Mb/s (unbalanced)

1. Connect signal from J4 (Tx unbal) to an HP 54520A Oscilloscope using a 75Ω to 50Ω Converter on a 50Ω Oscilloscope pod.
2. On the Unit Under Test Transmit page select 34 Mb/s and observe the unbalanced output on an Oscilloscope and the 75Ω to 50Ω Converter.
3. Oscilloscope settings are as follows:

CH1	CH2	Timebase	Trigger	VMarkers
490 mV/div Offs +1 V/-1 V (for +ve & -ve pk adjust)	Off	50 ns/div	CH1, 0 V, +ve slope, edge	± 2.46 V

NOTE When a 75Ω to 50Ω Converter is used the signal will be attenuated as indicated on the Converter. The Oscilloscope must therefore be set to the appropriate probe attenuation, for example: Greenpar: 3.16; Suhner: 2.45

4. Press Autoscale on the Oscilloscope.
5. Adjust the positive pulse amplitude to 1.00 V ±0.01 V using R44.
6. Adjust the negative pulse amplitude to -1.00 V ±0.01 V using R50. See Page 3-78 Figure 3-26, “Ternary Pulse Amplitude,” for expected result.
7. The pulse amplitude should be 1 V ±0.02 V with a good pulse shape i.e. 2 V pk-pk as illustrated in Fig 3-27.

Specification - 34 Mb/s unbalanced

Vmark = 0.9 -> 1.1 V (1.0 V nom)

Vpp = 1.8 -> 2.2 V (2.0 Vnom)

2 Mb/s unbalanced

1. Select 2 Mb/s, unbalanced signal using the soft keys on the Transmit set-up page.
2. Feed the unbalanced output, J4 (Tx unbal) to an HP 54520A Oscilloscope pod via a 75Ω to 50Ω Converter.
3. The pulse amplitude should be 2.37 V ±0.2 V with a good pulse shape i.e. 4.74 V pk-pk.

Specification- 2 Mb/s unbalanced

Vmark = 2.133 -> 2.607 V (2.37 V nom)

Vpp = 4.267 -> 5.214 V (4.74 Vnom)

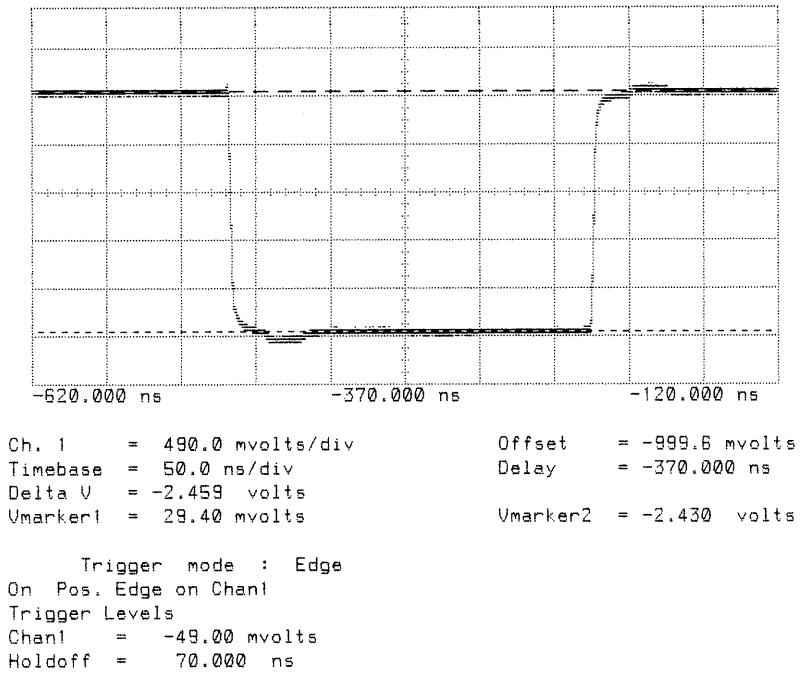


Figure 3-27 Ternary Pulse Amplitude

DS3 - Hi (unbalanced)

1. On the Unit Under Test Transmit page select DS3-HI and observe the unbalanced output on an Oscilloscope and the 75Ω to 50Ω Converter.
2. Press Autoscale on the Oscilloscope.
3. The pulse amplitude should be 0.91 V ±0.02 V with a good pulse shape i.e 1.82 V pk-pk.

Specification- DS3 (unbalanced)

Vmark = 0.91 V nominal

Vpp = 1.82 V nominal

DSX-3 (unbalanced)

1. On the Unit Under Test Transmit page select DSX-3 and observe the unbalanced output on an Oscilloscope and the 75Ω to 50Ω Converter.
2. Press Autoscale on Oscilloscope.
3. The pulse amplitude should be 0.56 V ±0.02 V with a good pulse shape i.e 1.12 V pk-pk.

Specification- DSX-3 (unbalanced)

Vmark = 0.457 -> 0.753 V (0.56 V nominal)

Vpp = 0.914 -> 1.506 V (1.12 Vpp nominal)

DS3-900 (unbalanced)

1. On the Unit Under Test Transmit page select DS3-900' and observe the unbalanced output on an Oscilloscope and the 75Ω to 50Ω Converter.
2. Press Autoscale on the Oscilloscope.
3. The pulse amplitude should be 0.33 V ±0.02 V with a good pulse shape i.e 0.66 V pk-pk.

Specification- DS3-900' (unbalanced)

Vmark = 0.33 V nominal

Vpp = 0.66 Vpp (nominal)

Procedure For Balanced Output

2M Amplitude check

1. On the Unit Under Test select 2 Mb/s, 120 Ω mode and feed the output signal from the 120Ω Bantam connector (J5) via an HP 15508B bal/unbal Converter and 75Ω to 50Ω Converter to the Oscilloscope.
2. Oscilloscope settings are as follows:

CH1	CH2	Timebase	Trigger	VMarkers
490 mV/div Offs +1 V/-1 V (for +ve & -ve pk adjust)	Off	50 ns/div	CH1, 0 V, +ve slope, edge	± 2.48 V

3. Check that the positive and negative pulses are 2.48 V ±0.01 V.
4. See Page 3-80 Figure 3-28, "Balanced Ternary Pulse Amplitude," for expected result.

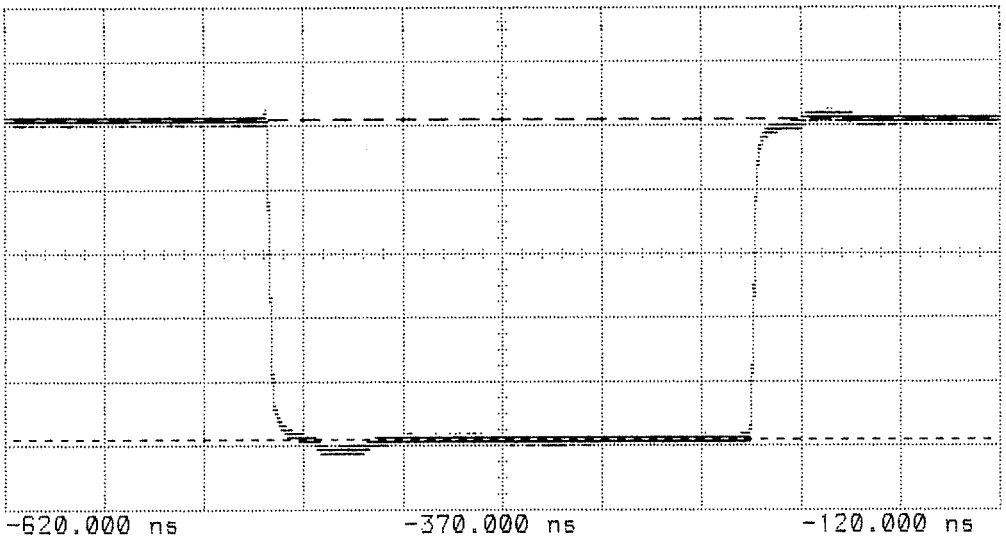


Figure 3-28 Balanced Ternary Pulse Amplitude

Specification- 2M balanced

Vmark = 2.229 -> 2.725 V (2.48 V nom) [NOTE: 110/75 ohm conv]

Vpp = 4.458 -> 5.45 V (4.95 Vnom)

DSX-1 Amplitude Check

1. On the Unit Under Test select DSX-1 mode and feed the output signal from the 100Ω Bantam connector (J5) via 15508B bal/unbal Converter and 75Ω to 50Ω Converter to the Oscilloscope.
2. Oscilloscope settings are as follows:

CH1	CH2	Timebase	Trigger	VMarkers
490 mV/div Offs +1 V/-1 V (for +ve & -ve pk adjust)	Off	50 ns/div	CH1, 0 V, +ve slope, edge	± 2.46 V

3 Check that the positive and negative pulses are 2.46 V ±0.1 V.

Specification- DS1 (balanced)

Vmark = 2.229 -> 2.725 V (2.48 V nom)

Vpp = 4.458 -> 5.45 V (4.95 Vnom)

DS1-LO Amplitude Check

1 On the Unit Under Test Transmit page select DS1-LO.
2 Press Autoscale on Oscilloscope.
3 The pulse amplitude should be 2.12 V ±0.02 V with a good pulse shape i.e 4.24 V pk-pk.

Specification- DS1-LO (balanced)

Vmark = 2.12 V nominal

Vpp = 4.24 Vpp (nominal)

Procedure For Clock Output

1 On the Unit Under Test Transmit page select DS3-HI.
2 Connect the Clock Output J6, to an Oscilloscope and the 75Ω to 50Ω Converter.
3 Press Autoscale on Oscilloscope.
4 The pulse amplitude should be 2.7 V ±0.1 V.

Specification- Clock Output

Vamp = 2.7 V nominal

Procedure For Insert Port Tests

1 Connect the HP 3771C Reference Instrument to the Unit Under Test as follows:

Reference Instrument unbal Tx to Unit Under Test UKZ unbal Mux port, J3.

Reference Instrument unbal Rx to Unit Under Test UKZ unbal Tx, J4.

2 Configure the Test instrument as follows:

OTHER

SETTINGS CONTROL
COUPLED

TRANSMIT

SIGNAL | 2 Mb/s

PAYLOAD TYPE, UNFRAMED

PATTERN, **1000**

3 Configure the Unit Under Test as follows:

OTHER

STORED SETTINGS, **RECALL 0**

TRANSMIT

SIGNAL, **E1 2Mb/s**

OTHER

MODULE DEBUG

MODULE, **ATM MODULE**

ATM MODULE, **TEST FUNCTION**

INSERT TEST, **ON**

4 Check that the Unit Under Test gains pattern sync with no errors or alarms.

WARNING **After using the INSERT TEST debug feature the Unit Under Test must be power cycled before continuing.**

Procedure For Module Interaction Tests

A1T Interaction

1 Connect the SDH Tx port to the SDH Rx port.

2 Configure the instrument as follows.

OTHER

STORED SETTINGS

STORED SETTING, **0**

ACTION, **RECALL**

SETTINGS CONTROL, **COUPLED**

TRANSMIT

SIGNAL, **STM-1**

3 Check that the instrument gains pattern sync and that there are no errors or alarms present.

ATM Cell Layer Receiver (Option UKZ)

This section describes the setup procedure for the following modules:

1 37717-60143 (Option UKZ Receive)

A 37717-60080 Option UKZ Transmit module MUST be fitted in the slot directly to the left of the board under test. An A1T module MUST be fitted to the left of that.

Procedure

Recovered Clock Adjustments

NOTE Firmware calibration is only valid if the 10 MHz internal clock calibration has been performed and the unit has been powered up for a minimum of 15 minutes, if this is not the case then monitor frequency at test point E1. Use FREQ. COUNTER at ALL times to check Frequency.

1 Select [OTHER] on the front panel then using the softkeys, select CALIBRATION. Using the cursor and softkeys, set CALIBRATION ITEM to CLK EXTRACT.

2 Using the softkeys, set the SELECTED CLOCK to DS1 (1.544 MHz). Depress the [RUN/STOP] key and adjust R43 to the target frequency ±200 ppm (±308 Hz for manual adjust) using the FREQ. COUNTER. Once set, depress [RUN/STOP] key on the front panel.

3 Using the softkeys, set the SELECTED CLOCK to 2 MHz (2.048 MHz). Depress the [RUN/STOP] key and adjust R52 to the target frequency ±200 ppm (±410 Hz for manual adjust). Once set, depress [RUN/STOP] key on the front panel.

4 Using the softkeys, set the SELECTED CLOCK to 34 MHz (34.368 MHz). Depress the [RUN/STOP] key and adjust R53 to the target frequency ±200 ppm (±6.8 kHz for manual adjust). Once set, depress [RUN/STOP] key on the front panel.

5 Using the softkeys, set the SELECTED CLOCK to DS3 (44.736 MHz). Depress the [RUN/STOP] key and adjust R8 to the target frequency ±200 ppm (±8.9 kHz for manual adjust). Once set, depress [RUN/STOP] key on the front panel.

Balanced Receiver Check

1 Connect SPDH balanced OUT J5, to IN J3, using 120Ω 3 pin Siemens cable.

2 Recall instrument Stored Settings Panel 0.

3 Set the Unit Under Test Tx and Rx settings coupled.

4 Set the Unit Under Test Tx signal to 2 Mb/s 120Ω Balanced.

5 Gate for 30 seconds and check for error free operation.

Ternary Waveforms at 34 MHz

1 Select an HDB3 unbalanced signal at 34 MHz using the softkeys on the setup page. With "SIG OUT",J4, connected to "SIG IN",J2, on the front panel using either 75Ω BNC or Siemens depending on options, connect CH1 of the Oscilloscope to E5 and CH2 to E6.

Table 3-2 Oscilloscope settings

CH1	CH2	Timebase	Trigger	Split Display
400 mV/div 0 V offset	400 mV/div 0 V offset	20 nS/div	CH1, 0 V, +ve slope, edge	On

2 Verify the waveform shapes are as in Figure 3-29, "Re-timed data at 34 MHz".

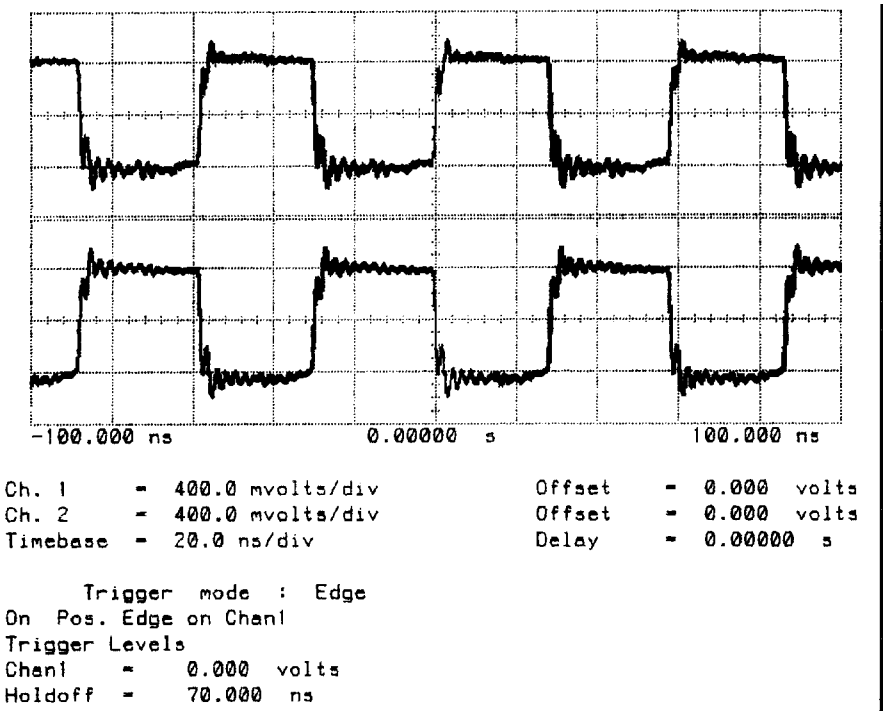


Figure 3-29 Re-timed data at 34MHz

Ternary Back-to back

1 Connect SPDH balanced OUT J5, to IN J3, using 120Ω 3 pin Siemens cable.

2 Select PRBS2^15 -1.

3 Check for ALL LED's Off on the instrument front panel.

4 Repeat for frequencies of 2 MHz, DS1 and DS3.

Recovered Clock At 34 MHz

1 Select an HDB3 unbalanced signal at 34 MHz using the softkeys on the setup page. With **SIG OUT** still connected to **SIG IN** on the front panel, connect CH1 of an Oscilloscope to E1.

Table 3-3 Oscilloscope settings

CH1	CH2	Timebase	Trigger	Split Display
200 mV/div 0 V offset	Off	20 ns/div	CH1, 0 V, +ve slope,edge	Off

2 Verify the waveform shape as shown in Figure 3-30, "Recovered 34 MHz Clock".

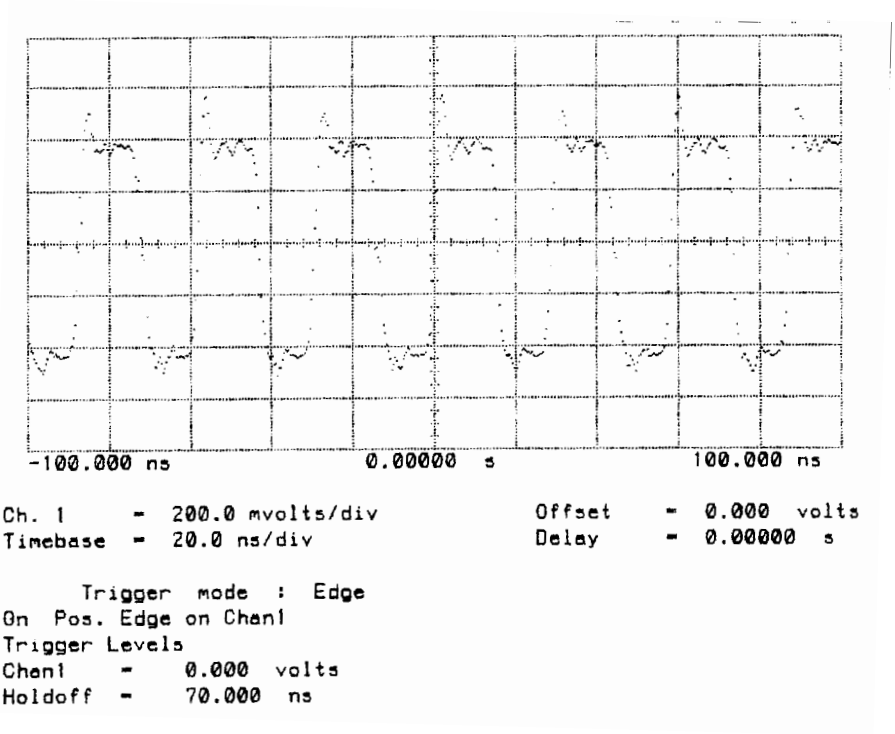


Figure 3-30 Recovered 34 MHz Clock

Data Re-timing Margin Check

1 On the Unit Under Test recall stored settings 0.

2 Connect the Unit Under Test unbal Tx port to the Unit Under Test unbal Rx port.

3 Set the Unit Under Test to COUPLED.

4 Set the Unit Under Test Signal to DS3.

5 Using an HP 54520A Oscilloscope (or equivalent) connect channel 1 to UKZ Rx test point E1, CLOCK, and channel 2 to E3, DATA.

6 Configure the Oscilloscope as follows:

CH1: 200 mV/div; OFFSET = 0 V

CH2: 200 mV/div; OFFSET = 300 mV

Trigger: channel 2; 0 V; rising edge

Timebase: 2 ns/div; DELAY = 0 s

Display: PERSISTENCE infinite

7 Using the Oscilloscopes time markers measure the time interval between the rising edge of the clock, E1, in the centre of the display and the falling edge of the data pulse, E3. The time interval should be in the range 2.5 to 5 ns.

8 If the time interval is < 2.5 ns then move the 0 ohm resistor in position R7 to position R6 and repeat the above test.

9 If the time interval > 5 ns then move the 0 ohm resistor in position R7 to position R4 and repeat the above test.

Drop Port tests

1 Connect the Reference HP 37717C to the Unit Under Test as follows:
Reference HP 37717C SPDH Tx (unbal) to Unit Under Test UKZ Rx (unbal), J2
Reference HP 37717C SPDH Rx (unbal) to Unit Under Test UKZ Drop port (unbal), J5.

2 Configure the Reference HP 37717C as follows:

OTHER

SETTINGS CONTROL, INDEPENDENT

TRANSMIT

SIGNAL, 34 Mb/s

PAYLOAD TYPE STRUCTURED

2M PAYLOAD, UNFRAMED

TEST SIGNAL, 2 Mb/s

PATTERN, 1000

RECEIVE

SIGNAL, 2 Mb/s

PAYLOAD TYPE, UNFRAMED

PATTERN, 1000

3 Configure the Unit Under Test as follows:

RECEIVE

SIGNAL, E3 34 Mb/s

4 Configure the Unit Under Test to drop a signal as follows:

OTHER

MODULE DEBUG

MODULE, **ATM MODULE**

ATM MODULE, **TEST FUNCTION**

DROP TEST, **ON**

5 Check that the Reference HP 37717C gains pattern sync with no errors or alarms.

WARNING **After using the DROP TEST debug feature the Unit Under Test must be power cycled before continuing.**

Module Interaction Tests - A1T Interaction

Connect the SDH Tx port to the SDH Rx port.

6 Configure the instrument as follows:

OTHER

STORED SETTINGS

STORED SETTING, **0**

ACTION, **RECALL**

SETTINGS CONTROL, **COUPLED**

TRANSMIT

SIGNAL, **STM-1**

7 Check that the instrument gains pattern sync and that there are no errors or alarms present.

Binary Interface (Option UH3)

This section describes the setup procedure for the Binary Interface PCA. This PCA is used in the following modules:

1 37717-60104 Option UH3 BNC Connectors.

2 37717-60107 Option US7 Small Siemens Connectors.

This PCA must be tested with Option Option UKK (unstructured PDH) or Option UKJ (structured PDH) loaded in the HP 37717C.

Procedure For -5.2 V Supply Adjustment

NOTE BEFORE power-on, R3 should be turned FULLY ANTI-CLOCKWISE to ensure that the -5.2 V power requirements for ECL circuitry does not exceed the allowable negative power rail voltage level and cause possible damage to the logic device.

1 Place the 37717-60082 PCA on an extender card to the right of the UPDH Module / SPDH Rx.

2 Connect a Digital Multimeter to TP1 (GND) and TP2 (N5V).

3 Switch on the Unit Under Test.

4 Adjust potentiometer R3 for a voltage of -5.2 V ± 0.05 V.

5 Using the Digital Multimeter monitor the test points shown in the table below. Switch off the Unit Under Test if the required voltages are not present.

Location	Output Voltage
TP6 (+5 V)	+5 V ± 0.25 V
TP4 (+5 VE)	+5 V ± 0.25 V
L11	+12 V ± 0.6 V
L12	-12 V ± 0.6 V

Procedure For Clock & Data Out

NOTE When tested with UKJ (Structured PDH) the binary interface rates are 2, 8, 34 and 140 Mb/s. When tested with UKK (Unstructured PDH) the binary interface rates are 0.7, 2, 8, 34 and 140 Mb/s.

ECL Threshold

6 Set the Unit Under Test to its default settings.

7 On the TRANSMITTER OUTPUT screen, change the INTERFACE to BINARY.

8 Probe F3 on the Oscilloscope and check the CLOCK signal is at ECL levels using an HP 54003A Pod and an HP 10345A 10:1 probe.

9 Change the PATTERN to 1010.

10 Probe F4 on the Oscilloscope and check the DATA signal is at ECL levels.

11 Connect the CLOCK OUT port to the Oscilloscope via a blocking capacitor and 75Ω to 50Ω Converter.

12 Select each rate (0.7, 2, 8, 34 and 140 Mb/s) in turn and check that the waveform parameters meet the limits shown in Table 3-4.

Table 3-4 ECL Limits

Rise Time	Duty Cycle
< 1 ns	60/40 to 40/60

13 Connect the DATA OUT port to the Oscilloscope via a blocking capacitor and 75Ω to 50Ω Converter.

14 Select each signal rate in turn and check that the waveform parameters meet the limits shown in Table 3-4. Ensure that the PATTERN is set to 1010 for each rate.

TTL Threshold

1 Change the SIGNAL to 34 Mb/s.

2 On the TRANSMITTER OUTPUT screen select BINARY.

3 Change the CLOCK and DATA THRESHOLD to TTL.

4 Probe F3 on the Oscilloscope and check the CLOCK signal is at TTL levels, using HP 54003A Pod and 10345A 10:1 probe.

5 Change the PATTERN to 1010.

6 Probe F4 on the Oscilloscope and check the DATA signal is at TTL levels.

7 Connect the CLOCK OUT port to the Oscilloscope via a 75Ω to 50Ω Converter.

8 Select each rate in turn and check that the waveform parameters for the CLOCK meet the limits shown in Table 3-5.

NOTE The Clock and Data Outputs are only specified up to 50 MHz when the TTL threshold is selected. Therefore it is only necessary to test the 34 Mb/s rate and below

Table 3-5 TTL Limits

Rise Time	Amplitude	Duty Cycle
< 8 ns	>2.4 V	60/40 to 40/60

9 Connect the DATA OUT port to the Oscilloscope via a 75Ω to 50Ω Converter.

10 Select each signal rate in turn and check that the waveform parameters for the DATA meet the limits in Table 3-5. Ensure that the PATTERN is set to 1010 for each rate.

Procedure For External Clock Input

Testing With UPDH Module

1 Set the Test Chassis Transmitter as follows:

SIGNAL **2 Mb/s**

INTERFACE **BINARY**

CLOCK SYNC **EXTERNAL**

THRESHOLDS

:CLOCK OUT **ECL**

DATA OUT **ECL**

EXT CLOCK **AUTO**

POLARITY:

CLOCK OUT **NORMAL**

DATA OUT **NORMAL**

EXT CLOCK **NORMAL**

2 Set the HP 8656B Signal Generator as follows:

Frequency	O/P Level	Modulation
170 MHz	-10 dBm (approx.)	OFF

3 Connect the CLOCK OUT via a blocking capacitor and 75Ω to 50Ω Converter to the Oscilloscope.

4 Connect the Signal Generator to the EXT CLOCK IN port.

5 Check that the mark:space ratio of the displayed clock waveform is between 60:40 and 40:60.

6 Connect CLOCK OUT to CLOCK IN and DATA OUT to DATA IN.

7 Check that NO alarm LED's are on.

8 Set the Signal Generator frequency to 700 kHz.

9 Connect CLOCK OUT via a blocking capacitor and 75Ω to 50Ω Converter to the Oscilloscope.

10 Check that the mark:space ratio of the displayed clock waveform is between 60:40 and 40:60.

11 Connect CLOCK OUT to CLOCK IN and DATA OUT to DATA IN.

12 Check that **NO** alarm LED's are on.

Testing with an SPDH Module

NOTE A Reference HP 37717C with Option UH3 fitted is required to fully test the External Clock Input.

1 Ensure the Tx and Rx are set to **COUPLED** on the Test Chassis.

2 Set the Unit Under Test Tx as follows:

SIGNAL, **140 Mb/s**

INTERFACE, **BINARY**

CLOCK SYNC **EXTERNAL**

THRESHOLDS:

CLOCK OUT **ECL**

DATA OUT **ECL**

EXT CLOCK **ECL**

POLARITY:

CLOCK OUT **NORMAL**

DATA OUT **NORMAL**

EXT CLOCK **NORMAL**

3 Set the Reference 37717C as follows:

SIGNAL **140 Mb/s**

INTERFACE **BINARY**

CLOCK SYNC **INTERNAL**

THRESHOLDS:

CLOCK OUT **ECL**]

DATA OUT **ECL**]

POLARITY:

CLOCK OUT **NORMAL**

DATA OUT **NORMAL**

4 Connect the CLOCK OUT via a blocking capacitor and 75Ω to 50Ω Converter to the Oscilloscope.

5 Connect the CLOCK OUT of the Reference HP 37717C to the EXT CLOCK of the Binary Interface under test.

6 Check that the mark:space ratio of the displayed clock waveform is between 60:40 and 40:60.

7 Connect the CLOCK and DATA OUT to CLOCK and DATA IN of the Binary Interface under test.

8 Check that NO alarm LED's are on.

9 Change the Signal to 2 Mb/s on the Unit Under Test and the Reference HP 37717C

10 Check that NO alarm LED's are on.

11 Connect the Reference 37717C CLOCK OUT to the Unit Under Test EXTERNAL CLOCK.

12 Check that the mark:space ratio of the displayed clock waveform is between 60:40 and 40:60.

Procedure For Back-To-Back Tests

1 Set the Unit Under Test PDH Tx as follows:

SIGNAL **34 Mb/s**

INTERFACE **BINARY**

CLOCK SYNC **INTERNAL**

FREQUENCY OFFSET **OFF**

PAYLOAD TYPE **UNFRAMED**

PATTERN **2^23-1 PRBS**

2 Set the Unit Under Test BINARY Tx as follows:

THRESHOLDS:

CLOCK OUT **ECL**]

DATA OUT **ECL**]

POLARITY:

CLOCK OUT **NORMAL**

DATA OUT **NORMAL**

3 Set the Unit Under Test BINARY Rx as follows:

THRESHOLDS:

CLOCK OUT **ECL**

DATA OUT **ECL**]

POLARITY:

CLOCK OUT **NORMAL**

DATA OUT **NORMAL**

Ensure that Tx and Rx are set to INDEPENDENT on the Unit Under Test .

4 Connect CLOCK OUT to CLOCK IN.

5 Connect DATA OUT to DATA IN.

6 Check that NO Alarm LED's are on.

7 Change the DATA OUT POLARITY to INVERTED on the HP 37717C [TRANSMIT] screen.

8 Check that the Pattern Loss LED is ON.

9 Change the DATA OUT POLARITY back to NORMAL.

10 Check that the Pattern Loss LED is OFF and that NO other Alarm LED's are on.

11 Change the DATA IN polarity to INVERTED on the [RECEIVE] screen.

12 Check that the Pattern Loss LED is ON.

13 Change the DATA IN polarity back to NORMAL.

14 Check that the Pattern Loss LED is OFF and NO other Alarm LED's are on.

15 Change the PDH Tx and Rx SIGNAL to 8 Mb/s.

16 Change the PDH Tx and Rx PATTERN to 1000.

17 Change the BINARY Tx and Rx CLOCK and DATA THRESHOLDS to TTL.

18 Check that NO Alarm LED's are on.

19 Change the DATA OUT polarity to INVERTED.

20 Check that the Pattern Loss LED is ON.

21 Change the DATA OUT polarity back to NORMAL.

22 Check that the Pattern Loss LED is OFF and NO other Alarm LED's are on.

23 Change the DATA IN polarity to INVERTED.

24 Check that the Pattern Loss LED is ON.

25 Change the DATA IN polarity back to NORMAL.

26 Check that the Pattern Loss LED is OFF and NO other Alarm LED's are on.

STM Clock (Option A3R)

This section describes the setup procedure for part of the following modules;

1 37714-60130 (Option A3R)

2 37714-60131 (Option A3S)

NOTE The Reference HP 37717C must be fitted with a test HP 37714-60076 PCA, URU or USN module, jitter transmitter (HP 37717-60008 & HP 37717-60094) and SDH jitter receiver (HP 37717-60122 and HP 37717-60015, HP 37717-60016 or HP 37717-60017).

NOTE To ensure that the Firmware in the Processor Card is A.03.17 or later.
Press OTHER, MORE, OPTIONS, ⇩, REMOTE/PRINTER to display the firmware rev.

Procedure For Receive Clock Recovery

1 Connect a known working 2 Mb/s output to the clock input at J2.

2 Set 2 Mb/s Transmit by selecting:
TRANSMIT PDH

TRANSMIT SIGNAL (2M)

75Ω Unbalanced

3 Set pattern PRBS 15 (2^15-1) on known working instrument.

4 Set unit under test clock sync to 2M clock reference (J2) by selecting
TRANSMIT SDH

CLOCK SYNC (EXTERNAL MTS)

2M DATA

5 Connect the Oscilloscope to TP10 (CKOUT) using 10kΩ pod.

6 Set up Oscilloscope as follows:

CH1	Timebase	Trigger	Delay Ref.	Display	Persistence	Split Display
1 V/div 2.4 V offset	100 nS/div	CH1 -ve slope	Centre	Normal	500 ms	Off

7 Adjust C38 to give minimum jitter on Oscilloscope trace. (see Page 3-96 Figure 3-31).

8 Check Clock Loss LED (DS1, on board) is not lit.

9 Disconnect cable going to J2.

10 Connect 3 Pin Siemens test cable from 2M Output on known working instrument to J3.
TRANSMIT PDH

TRANSMIT SIGNAL (2M)

120Ω Balanced

11 Check that the clock loss LED is still extinguished.

12 Connect the Option 110/120 G'STD DS1 TRANSMIT OUT to J4.

13 On the Reference HP 37717C set:
PDH/DSn

SIGNAL DS1

14 On the Unit Under Test set:
SDH

CLOCK EXTERNAL

BITS 1.5 Mb/s

15 Connect the Oscilloscope to TP10 (CKOUT) on the HP 37714-60075 PCA using a 10KΩ pod.

16 Set the Oscilloscope Timebase to 200 ns/div.

17 Adjust C42 to give minimum jitter on the Oscilloscope trace (Figure 3-31),"2M Clock Recovery, set for minimum jitter").

18 Check the CLOCK LOSS LED (DS1 on the HP 37714-60075 PCA) is not lit.

19 Disconnect the cable from J4.

20 Set Unit Under Test clock sync to INTERNAL by selecting:

21 TRANSMIT SDH
CLOCK SYNC (INTERNAL)

22 Connect the Oscilloscope channel 1 to E2 using 10kΩ pod.

23 Set up Oscilloscope as previous settings.

24 Check for 2.5 V D.C. ±0.5 V.

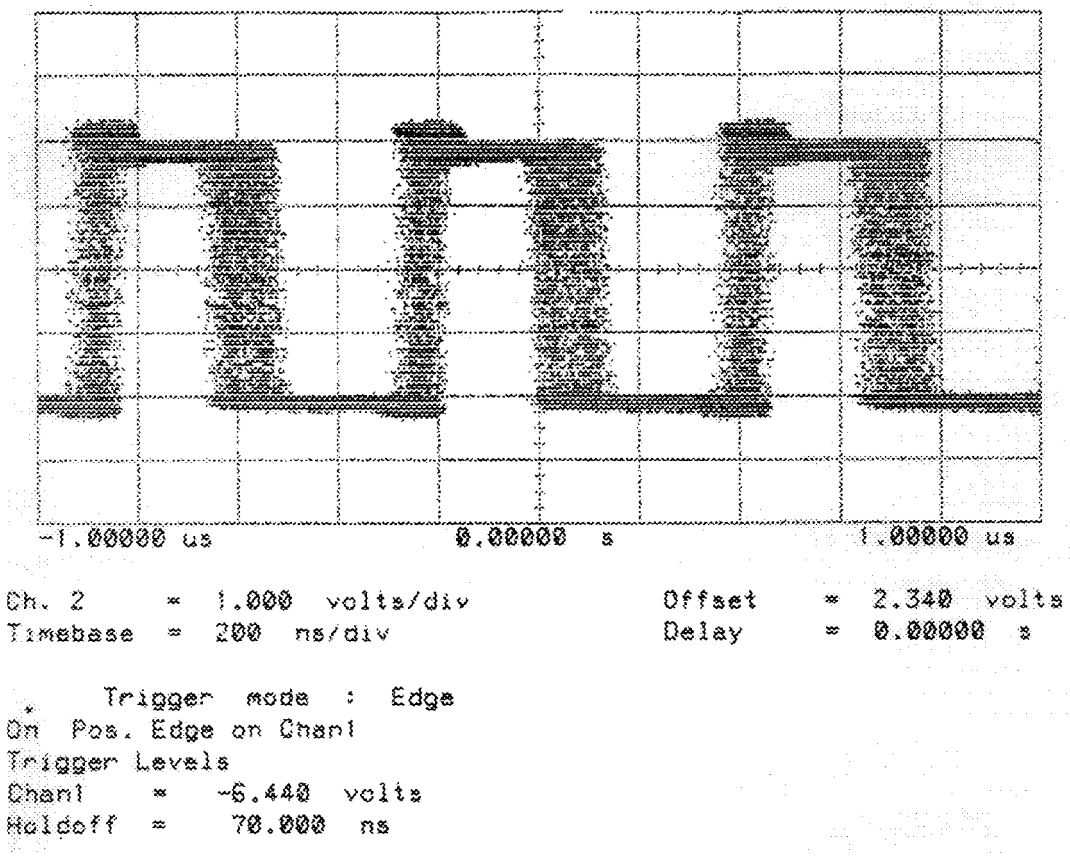


Figure 3-31 2M Clock Recovery, set for minimum jitter.

Procedure For Stm-1 Receive Clock Sync

1 Reset the Unit Under Test and the Reference Instrument by selecting:

OTHER

STORED SETTINGS

ACTION, RECALL

2 Set SDH Transmitter and Receiver settings to coupled by selecting:

OTHER

SETTINGS CONTROL, COUPLED

3 Set the Unit Under Test and the Reference Instrument to Transmit SDH.

4 Connect the Reference Instrument SDH output to J2 on the Unit Under Test (SDH IN)

5 Set the Unit Under Test to:

TRANSMIT

CLOCK SYNC

STM-1 RECEIVE

6 Ensure that the CLOCK LOSS LED is extinguished.

Procedure For Offset Clock

Pre-Adjustment Setup

Connect the SDH O/PJ4, to SDH I/PJ2, with a 75 ohm cable. The following must be set on the instrument front panel before any adjustments can be attempted on this card.

1 Reset the Unit Under Test Transmitter and Receiver by selecting:

OTHER

STORED SETTINGS

ACTION RECALL

2 Set SDH Transmitter and Receiver settings to coupled by selecting:

OTHER

SETTINGS CONTROL COUPLED

Positive Offset

3 Set the instrument to SDH and the frequency offset to +100 ppm.

TRANSMIT

SDH

FREQUENCY OFFSET, ON

+ 100 PPM

4 Ensure that the correct frequency is measured.

RESULTS

SDH RESULTS

MORE

FREQUENCY

RUN/STOP

Allow the instrument to make two measurements and then check that the measured offset is within the limits:

Offset = + 100.0 ppm $\pm$ 5.0 ppm

Negative Offset

1 Set the instrument to SDH and the frequency offset to -100 ppm:

TRANSMIT

SDH

FREQUENCY OFFSET ON

- 100 PPM

2 Ensure that the correct frequency is measured:

RESULTS

SDH RESULTS
MORE
FREQUENCY

RUN/STOP

Allow the instrument to make two measurements and then check that the measured offset is within the limits:

Offset = - 100.0 ppm ± 5.0 ppm

SDH Jitter

Preparation

Connect the SDH O/P (J4) to the Jitter Receiver STM1E I/P (J2). The following must be set on the instrument front panel before any adjustments can be attempted on this card.

1 Reset the Unit Under Test Transmitter and Receiver by selecting:

OTHER

STORED SETTINGS
ACTION | RECALL

2 Set the transmitter to SDH.

3 Set the receiver to SDH JITTER.

4 The MODULE DEBUG page must be used to control the following settings, it can be found by using the following key sequence:
OTHER; ⇧; MORE; ⇧; MORE; ⇧; MORE; OTHER. Press MORE until MODULE DEBUG appears in the softkey menu.

5 Set Jitter Tx and Rx calibration off by selecting:
MODULE, JITTER MODULE

TX CALIBRATION, OFF

RX CALIBRATION, OFF

WARNING **All the debug functions set above will be reset if the instrument is power cycled, so this preparation procedure will have to be repeated every time the instrument has to be powered down, (e.g. if a card is moved on or off the extender card).**

1 UI range jitter measurement

1 Set the instrument to generate 0.5 UI SDH jitter:

TRANSMIT

SDH

JITTER

JITTER ON

AMPLITUDE 0.5 UI

RECEIVE

SDH JITTER

2 Measure the received jitter and check that it is within limits:
RESULTS

JITTER CUMULATIVE

AMPLITUDE

RUN/STOP

Check that no alarms are lit and that the measured jitter is within the range:

Jitter pk-pk = 0.5 UI ± 0.1 UI

10 UI range jitter measurement

1 Set the instrument to generate 5 UI SDH jitter by selecting:

TRANSMIT

SDH

JITTER

JITTER ON

RANGE 10 UI

AMPLITUDE 5 UI

RECEIVE

SDH JITTER

RECEIVER RANGE 16 UI

2 Measure the received jitter and check that it is within limits:

RESULTS

JITTER

CUMULATIVE
AMPLITUDE

RUN/STOP

Check that only the jitter hits alarm is lit and that the measured jitter is within the range:

Jitter pk-pk = 5 UI ± 1 UI.

STM 1/4 optics

NOTE All PCAs must be fitted into the chassis to perform this test.

1 Reset the Unit Under Test Transmitter and Receiver by selecting:

OTHER

STORED SETTINGS

ACTION RECALL

2 Set SDH Transmitter and Receiver settings to coupled by selecting;

OTHER

SETTINGS CONTROL
COUPLED

3 Connect 1550 nm Optical OUT to IN (thru' an attenuator to limit max I/P to -8 dB).

4 Set Unit Under Test Transmit and Receive to STM-1 Optical (1550 nm).

TRANSMIT

SDH

SIGNAL, STM-1 OPT 1550

5 Ensure that all error warning LEDs are extinguished.

6 Set Unit Under Test Transmit and Receive to STM-4 Optical (1550 nm):

TRANSMIT

SDH

SIGNAL, STM-4 OPT 1550

7 Ensure that all error warning LEDs are extinguished.

SDH (Option A3R)

This section describes the setup procedure for part of the following modules:

1 37714-60130 (Option A3R)

2 37714-60131 (Option A3S Small Siemens)

If a 75Ω to 50Ω Converter is used the signal will be attenuated as indicated on the Converter. The Oscilloscope must therefore be set to the appropriate probe attenuation, for example:

Greenpar: 3.16

Suhner: 2.45

ET8175: 10

NOTE The Reference HP 37717C must be fitted with an HP 37714-60075, an SPDH Tx & Rx and a UH2 module. The HP 37714-60176 card is the REV D version of the HP 37714-60076 card.

Procedure For STM-1 CMI Transmitter

Mark - Space Adjust

1 Connect the signal from J4 to an HP 54520A Oscilloscope using a 75Ω coax cable and a 75Ω to 50Ω Converter on a 50Ω input pod. Set the Oscilloscope up as follows:

CH1	Timebase	Trigger	Offset
200 mV/div	2 nS/div	-ve edge, centre	0 V

2 Set Unit Under Test STM-1 TX pattern to all 1's by selecting: OTHER, ⇧, MORE, ⇧, MORE, ⇧, MORE and OTHER. Press MORE until MODULE DEBUG appears in the softkey menu.

3 Then Press MODULE DEBUG STM-1 ALL 1'S

4 Adjust R34 to give a 50:50 mark to space ratio.

5 Alter pattern from STM-1 ALL 1'S to STM-1 ALL 0'S.

6 Change Oscilloscope TIME BASE to 1 ns/div.

7 Adjust R39 to give a 50:50 mark to space ratio.

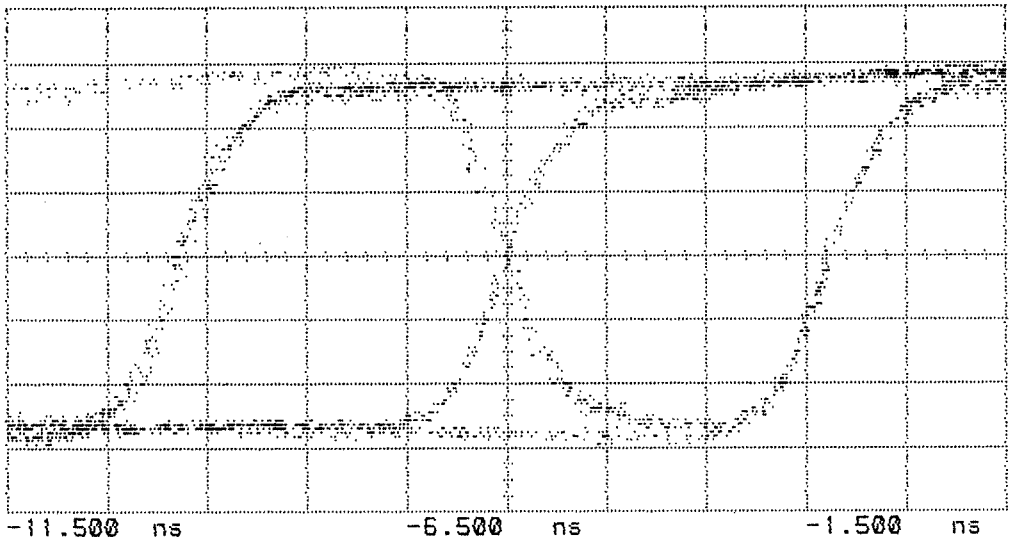
8 Repeat steps 2 to 6 as necessary.

9 Switch STM-1 test pattern OFF.

10 Set Oscilloscope TIME BASE to 1 ns/div, set DELAY to 7 ns.

11 Adjust R39 to bring data pattern back to a 50:50 mark to space ratio, as shown in fig 3-32.

Figure 3-32 STM-1 CMI TX mark space adjust



Amplitude

1 Connect the signal from J4 to the 75 Ω terminated input of an HP 54520A Oscilloscope, using a 75 Ω coax cable.

2 Set Oscilloscope as follows:

CH1	Timebase	Offset
200 mV/div	2 ns/div	0 V

3 Set Unit Under Test STM-1 TX pattern to all 1's using the same procedure as before by selecting STM-1 ALL 1'S, on the debug page.

4 Adjust amplitude via R26 to give 1 V ±50 mV pk-pk (allowing for 75Ω to 50Ω Converter attenuation).

Rise and Fall Time Measurement

1 Connect J4 to an HP 54520A Oscilloscope using 75Ω coax cable and a 75Ω to 50Ω Converter on a 50Ω Oscilloscope pod.

2 Set up the Unit Under Test STM-1 TX pattern to ALL 1's using the same procedure as before (see Mark-space Adjust), and select STM-1 Test Pattern ALL ONES.

3 Set up Oscilloscope by hitting Auto-Setup key.

4 Measure rise time by selecting the Oscilloscope Measure function, and hitting the Rise Time key. Check that the rise time is less than 1.5 ns.

5 Measure the fall time by hitting the Fall Time key. Check that the fall time is less than 1.5 ns.

Overshoot Measurement

1 Connections: as for Rise and Fall Time Measurement.

2 Set up Oscilloscope by hitting Auto-Setup key.

3 Select Oscilloscope Measure function and hit Overshoot key. Check that the overshoot is less than 30 mV (3%).

Attenuation Test

1 Recall the instrument default settings.

2 Set the OTHER page Settings Control to COUPLED.

3 Connect the SDH "SIG OUT",J4, to SDH "SIG IN",J2, via a RS2115 attenuator.

Terminate

1 Set the Unit Under Test Tx and Rx to STM-1, 2^23-1 pattern, Terminate mode.

2 Set the RS2115 attenuator to 7 dB.

3 Check that the Errors alarm LED stays off for at least 10 seconds.

Monitor

1 Set the attenuator to 24 dB and change the Unit Under Test to Monitor mode.

2 Select 26 dB GAIN.

3 Check that the Errors alarm LED stays off for at least 10 seconds.

4 Repeat with attenuator set to 28 dB.

Procedure For STM-o B3ZS Transmitter

Mark - Space Adjust

NOTE Adjusting R53 from one end stop to the other alters the M:S ratio by only 1% or 2%. Therefore set R53 to the middle of its range.

Attenuation Test STM -o (Monitor Mode)

1 Set the Unit Under Test Tx and Rx to the settings shown in the table below.

2 Select the appropriate attenuation on the attenuator for that setting, shown in the table below.

3 Set the Rx LEVEL to MONITOR.

4 For each setting check that the Errors Alarm LED remains **OFF** for at least 10 seconds.

.

Signal: STM-0		
Tx	**Rx**	**Attenuation**
X-CON	HIGH	16 dB
X-CON	HIGH	28 dB
X-CON	LOW	16 dB
X-CON	LOW	30 dB
HIGH	HIGH	16 dB
HIGH	HIGH	30 dB
LOW	LOW	16 dB
LOW	LOW	28 dB

Procedure For STM 1/4 Optics

NOTE All PCAs must be fitted into the chassis to perform this test.

1 Reset the Unit Under Test Transmitter and Receiver by selecting:

OTHER

STORED SETTINGS

ACTION | RECALL

2 Set SDH Transmitter and Receiver settings to coupled by selecting:

OTHER

SETTINGS CONTROL COUPLED

3 Connect 1310 nm Optical OUT to IN.

4 Set Unit Under Test Transmit and Receive to STM-1 Optical (1310 nm):

TRANSMIT

SDH

SIGNAL STM-1 OPT 1310

5 Ensure that all error warning LEDs are extinguished.

6 Set Unit Under Test Transmit and Receive to STM-4 Optical (1500 nm):

TRANSMIT

SDH

SIGNAL | STM-4 OPT 1310

7 Ensure that all error warning LEDs are extinguished.

Procedure For STM-1 Receive Clock Sync

1 Reset the Unit Under Test and Gold Standard by selecting:

OTHER

STORED SETTINGS

ACTION | RECALL

2 Set SDH Transmitter and Receiver settings to coupled by selecting:

OTHER

SETTINGS CONTROL COUPLED

3 Set the Unit Under Test and the Reference Instrument to Transmit SDH.

4 Connect the Reference Instrument SDH output to J2 on the Unit Under Test (SDH IN).

5 Set the Unit Under Test to:

TRANSMIT

CLOCK SYNC

STM-1 RECEIVE

6 Ensure that the CLOCK LOSS LED is extinguished.

4

Replaceable Parts

Introduction

This section contains the information required to order the replaceable parts for the HP 37717C. These replaceable parts are listed in one of the following categories:

Non-exchange Assemblies - see Table 4-1.

Exchange Module Assemblies - see Table 4-2.

Mainframe Replaceable Components - see Tables 4-3, Table 4-4 Case Assembly, Table 4-5 Disk Drive and CPU and Figure 4-1 Case Assembly.

Module Replaceable Components - see module information in Figures 4-2 to 4-20 and Tables 4-6 to 4-22.

Exchange Program

The Hewlett-Packard Exchange Assembly Program provides a fully tested and warranted restored board assembly at reduced cost. Due to the nature of the program, only selective high-cost HP 37717C assemblies are eligible. All other boards are available only as Non-exchange Assemblies.

For the cost benefit to be realized, the defective part must be returned to Hewlett-Packard.

Ordering Information

Check Table 4-2 to see if the part is available on the Exchange Program. If the part is not listed, quote the Hewlett-Packard part number from Table 4-1 or Table 4-3, and address the order to the nearest HP Sales and Service Office.

Where an assembly is listed as an Exchange Part, use the following procedure to obtain the part:

1 Order the Exchange Assembly from the nearest HP Sales and Service Office, using the Exchange Part Number given in Table 4-2. The restored assembly will be sent immediately from the Customer Service Replacement Parts Center.

NOTE Do not return the faulty assembly to Hewlett-Packard until you receive the restored Exchange Assembly.

2 Complete the Exchange Failure Report which accompanied the restored Exchange Assembly.

3 Return the faulty assembly and the exchange failure report to the Customer Service Replacement Parts Center using the same special packaging received.

Table 4-1 Non-Exchange Modules

Reference Designator	HP Part Number	Description
A0	37717-60160	Power Supply plus cables
A2	37714-60002	Front Panel Cover Assembly
A3	37717-60029	37717C Motherboard
A4	37717-60159	37717C CPU replacement
A6	37714-60006	PDH Rx
A7	37714-60007	PDH Tx
A45	2090-0346	37717C LCD Assembly
A62	37717-60562	Front Panel Control
A63	37717-60563	LED PCA
CPU	37717-60190	Disc Drive Replacement
UKX	37717-60095	Inlid Printer Assembly
	37717-60045	Chassis Assembly
	37717-60085	Sleeve Cover
	37717-60119	Original Front Panel
	37717-60248	New Front Panel

Table 4-2 Exchange Modules

Option	HP Part Number	Description
UKK	37714-69044	Unstructured PDH
UKJ/UKN	37717-69020	Structured PDH Tx
UKJ/UKN	37717-69021	Structured PDH Rx
UKZ/110	37717-69080	DS1/3 ATM Tx
UKZ/110	37717-69081	DS1/3 ATM Rx
UH3	37717-69082	Binary Interface PDH
UH0	37714-69018	STD Clock PCAB
UH0,UHA,US1	37714-69109	SDH Assy
US1,A1T	37714-69010	SDH Clock PCAB
US1,A1T	37714-69101	SDH Clock PCAB
A1T	37714-69039	SDH Assembly
A3R,120	37714-69075	Enhanced SDH Clock PCAB
A3R,120	37714-69076	Enhanced SDH Assembly
A3R,120	37714-69176	Enhanced SDH Assembly
UH1	37714-69011	STM-1 Optical Assembly
UKT	37714-69070	STM1/4 Optics
USN	37714-69071	STM1/4 Optics
130	37714-69111	STM-0/1/4 Dual Optics
131	37714-69110	STM-1/1/4
UHK	37717-69008	Jitter Tx PDH
UHN	37717-69006	Jitter Rx PDH
A1M	37717-69033	STM-1-e Jitter Module
A1Q	37717-69034	STM-1-e Jitter Module
A1N	37717-69046	STM-1e/o Jitter Module
A1R	37717-69047	STM-1e/o Jitter Module
A1P	37717-69048	STM-1/4 e/o Jitter Module
A1S	37717-69049	STM-1/4 e/o Jitter Module
A3K	37717-69105	Jitter Tx PDH/SDH
A3L	37717-69110	STM-1E PDH Jitter Rx
A3M	37717-69111	STM-1E PDH Jitter Rx
A3N	37717-69112	STM-1E/STM-1O/STM-4O PDH Jitter Rx
A3P	37717-69113	STM-1E/STM-1O/STM-4O PDH Jitter Rx
A3V	37717-69134	STM-1E/STM-1O/PDH Jitter Rx
A3W	37717-69135	STM-1E/STM-1O/PDH Jitter Rx

Table 4-3 Mainframe Replaceable Components

HP Part Number	Description	Quantity
0960-0549	Audio Buzzer 4 KHz	1
106703	RFI Gasket	10
1540-1211	Pouch	1
1990-0485	Front Panel LED Green	1
1990-0486	Front Panel LED Red	24
1990-0487	Front Panel LED Yellow	4
2110-1120	Fuse 5A, 250 V On-board PSU Assembly	1
37714-00006	Post Rear	1
37714-00013	Panel Blank Single	1
37714-00014	Panel Blank Double	1
37714-00023	Panel Blank Double Optic	1
37714-60017	Cable, 13-Way Ribbon Assembly (A3J8/A0J2)	1
37714-60018	Cable, 60-Way Ribbon Assembly (A3J1/A2J1)	1
37714-60029	Cable, 50-Way Ribbon Assembly (A1J1/A2J4)	1
37714-60032	Cable, 16-Way Ribbon Assembly (A10J1/A2J2)	1
37714-60099	Module Board Extender Card	2
37714-80001	Prom Assembly	1
37717-90414	HP 37717C Operating Manual	1
37717-90435	HP 37717C Calibration Manual	1
37717-90430	HP 37717C Remote Control Manual	1
5002-1109	Label, ISM	1
5021-5483	Latch Catch	2
5041-7235	Gasket Seal	1m
5041-8915	Front Panel Cover	1
5062-0730	Catch Drawer Assembly	2
0950-3108	Disc Drive Assembly	1
37717-60028	Input Cable for PSU Module	1
37717-60051	Sense Cable for PSU Module	1
0515-2032	Module Retaining Screws (Torx)	2 per Module

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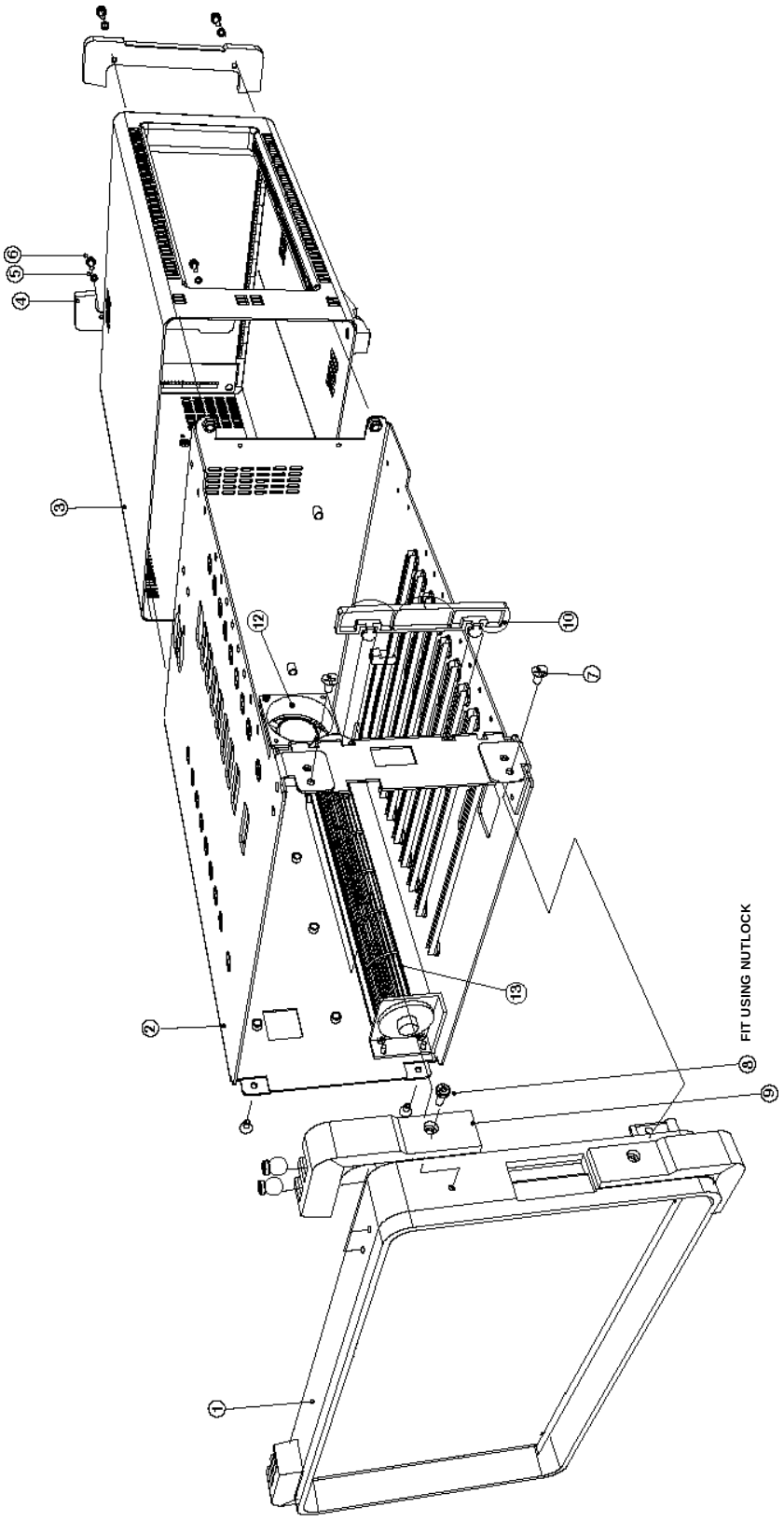

Figure 4-1 HP 37717C Case Assembly

Table 4-4 Case Assembly Replaceable Parts List

Parts List	HP Part Number	Quantity	Item In Figure 4-1
HP 37717C Chassis Assembly	37717-60045	1	2
HP 37717C Sleeve Cover Assembly	37717-60085	1	3
Rear Foot	37701-40001	2	4
M5 Lock Washer	2190-0587	4	5
M5 x 14 Panhead Pozidriv Screw	0515-0949	4	6
M4 x 8 90° c/sk Head		4	7
M3 x 8 Panhead Pozidriv Screw		12	8
Bumper Kit	5062-4806	1	9
Front End Bezel Insert	37714-40003	1	10
HP 37717C Front Panel Assembly (includes Membrane Keypad)	37717-60119	1	1
HP 37717C Barrel Fan (7-section)	37717-60040	1	12
Line Input/Switch Assembly	37717-60053	1	13
Line Filter Assembly	37717-60018	1	P/O 13
Power Fail Cable	37717-60051		
Line Fuse 5A 230V	2110-1120	1	
V Switch Cable Assembly	37717-60017		

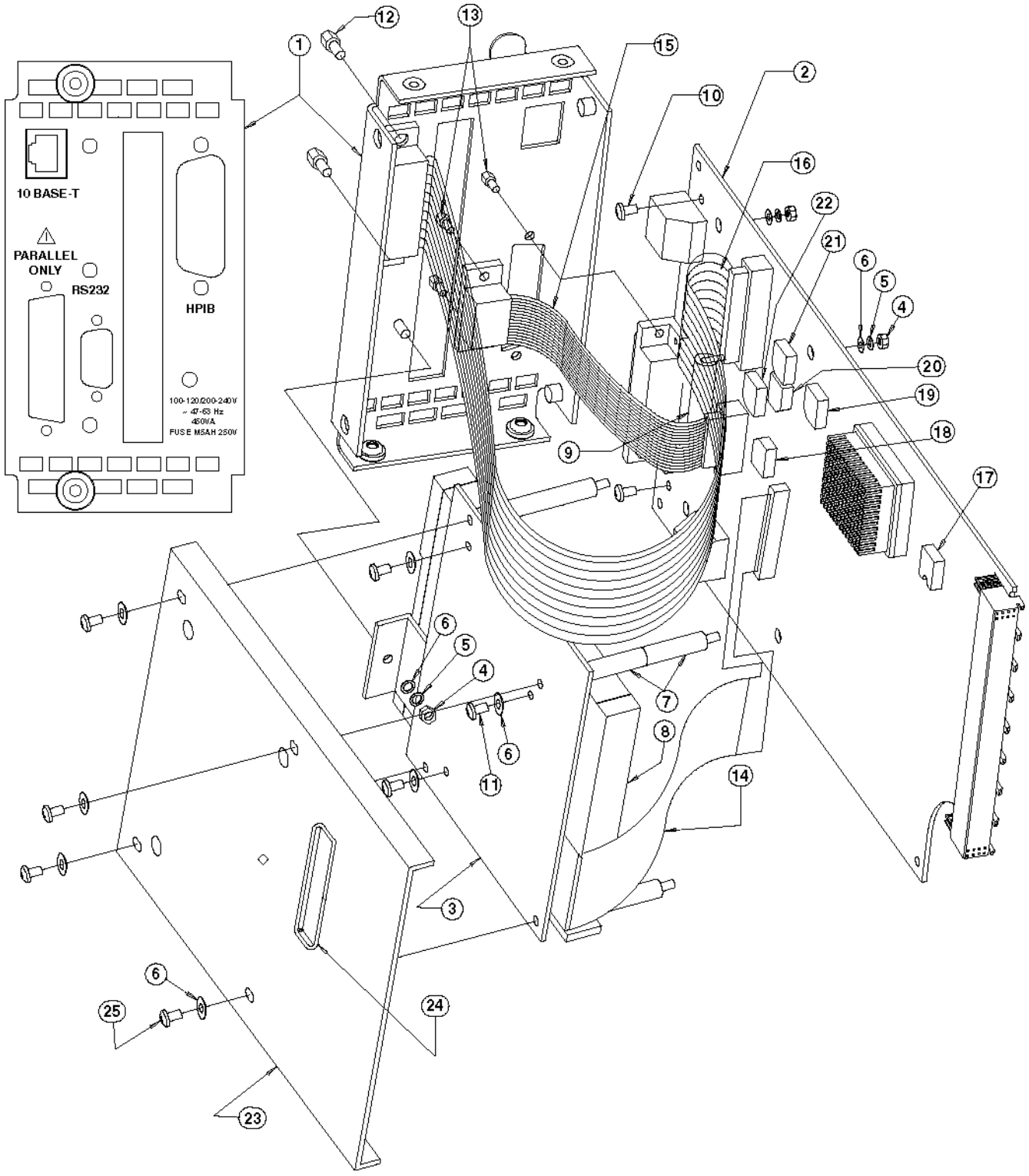

Figure 4-2 Processor - Exploded View

Table 4-5 Disk Drive CPU Replaceable Parts List

Description	HP Part No.	Qty	Item
Processor Module (non-LAN)	37717-60052	1	N/A
Module Front Panel	37714-00031	1	1
Processor Board Assembly (non-LAN)	37714-60028	1	2
Disk Drive Support Plate	37714-00030	1	3
Nut M3	0535-0025	1	4
Lock Washer M3	2190-0584	5	5
Plain Washer M3 x 0.5	3050-0891	11	6
Standoff	0380-2082	8	7
Disk Drive Assembly	0950-3108	1	8
Battery 3.6Volts Lithium	1420-0380	1	9
Screw machine M3 x 6mm	0515-0886	2	10
Screw machine M2.5 x 6mm	0515-0894	3	11
Stud 4-40 UNCH3.5	380-2072	2	12
Screw Lok Kit D	1251-5436	2	13
Cable Assembly (disk drive -CPU Board)	37717-60002	1	14
Ribbon Cable	37714-60058	1	15
Ribbon Cable	37701-60027	1	16
RFI Strip	8160-0616	N/A	17
Bootrom (eeprom) IC *	37714-80032	1	18
Disk Drive RFI Shield	37714-00050	N/A	23
Edge Protection Strip	0400-0018	N/A	24
Screw machine M3 x 8mm	0515-0897	4	25

* This eeprom contains unique information about the instrument personality. If changing this part, follow the instructions in Service note 37717C-07 - see Appendix B.

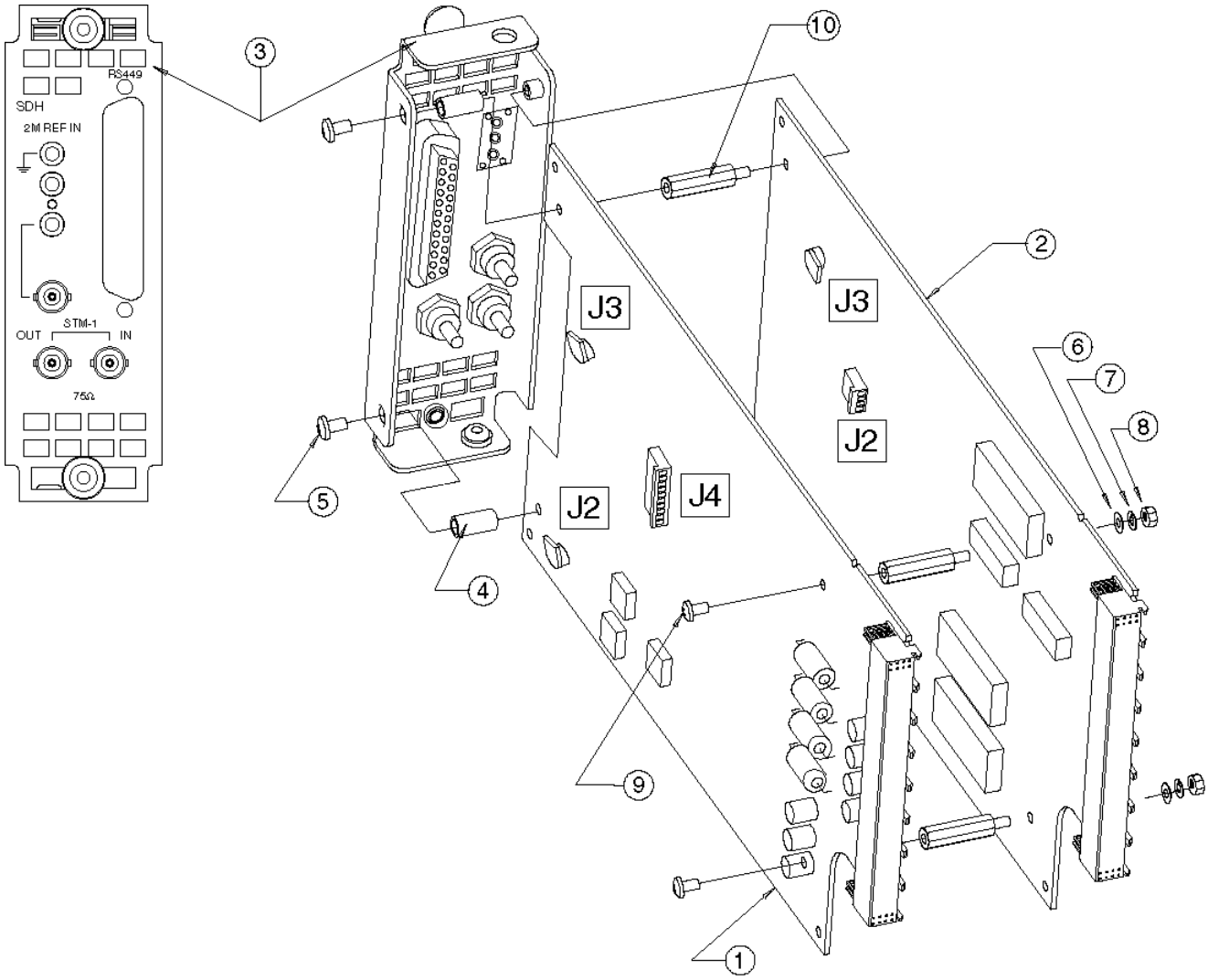

Figure 4-3 Option A1T SDH Module - Exploded View

Table 4-6 SDH Option A1T Replaceable Parts List

Description	HP Part No.	Qty	Item
Option A1T SDH Module	37714-60100	1	N/A
Option A1U SDH Module	37714-60102	1	N/A
SDH Board Assembly	37714-60039	1	1
Clock Board Assy	37714-60101	1	2
Front Panel Assembly (BNC)	37714-60093	1	3
Front Panel Assembly (small Siemens)	37714-60094	1	3
Spacer	0380-0008	2	4
Screw machine M3 x 20mm	0515-1441	2	5
Plain Washer M3 x 0.5	3050-0891	2	6
Lock Washer M3	2190-0584	2	7
Nut M3	0535-0025	2	8
Screw machine M3 x 6mm	0515-0886	2	9
Standoff	0380-2082	8	10

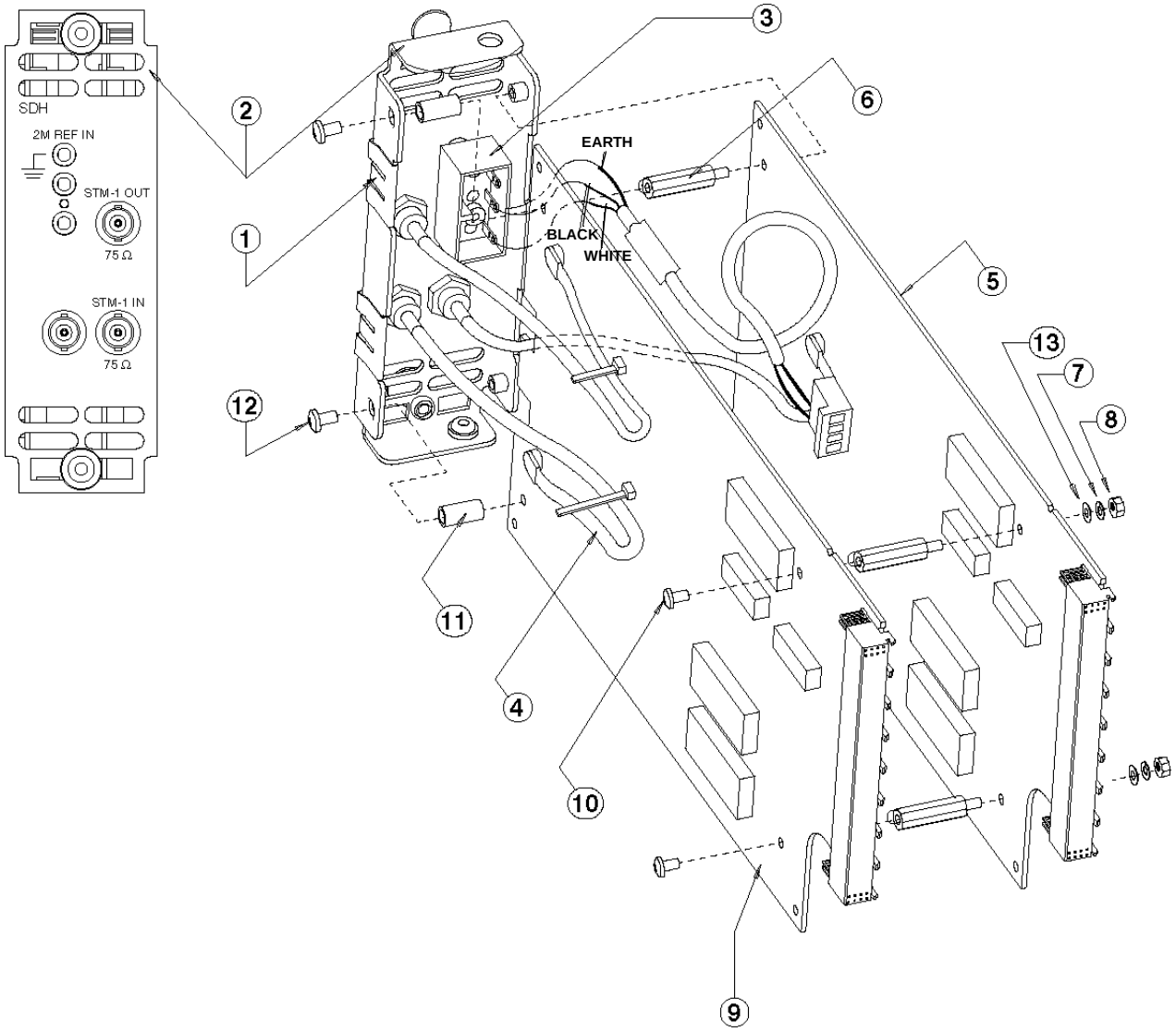

Figure 4-4 Option US1 SDH Module - Exploded View

Table 4-7 Option US1 SDH Module Parts List

Description	HP Part No.	Qty	Item
Clip Spring	5180-0409	2	1
Panel SDH	37714-00009	1	2
Panel SDH (small Siemens)	37714-00020	1	2
Cbl 3-pin Siemens	37714-60021	1	3
Cbl-Asy BNC-FL75	37721-60025	3	4
Cbl-Asy FL-75 (small Siemens)	37721-60030	1	4
Std Clock PCAB UHO	37714-60008	1	5
Std Clock PCAB UHA	37714-60010	1	5
Std Offhx M3 x 22 M/F	0380-2082	4	6
Washer LK M3	2190-0584	2	7
Nut M3	0535-0025	2	8
SDH Assy PCAB	37714-60009	1	9
SCR MC M3 x 6mm	0515-0886	2	10
Spacer	0380-0008	2	11
SCR MC M3 x 20mm	0515-1441	2	12
Flat Washer	3050-0891	2	13
Serrated Washer	2190-0016	3	14
Nut	0535-0026	1	15
Cable Tie	1400-0307	3	16
Cable Clamp	1400-1617	2	17
Screw	0515-1427	1	18
Spacer	37724-20001	1	19

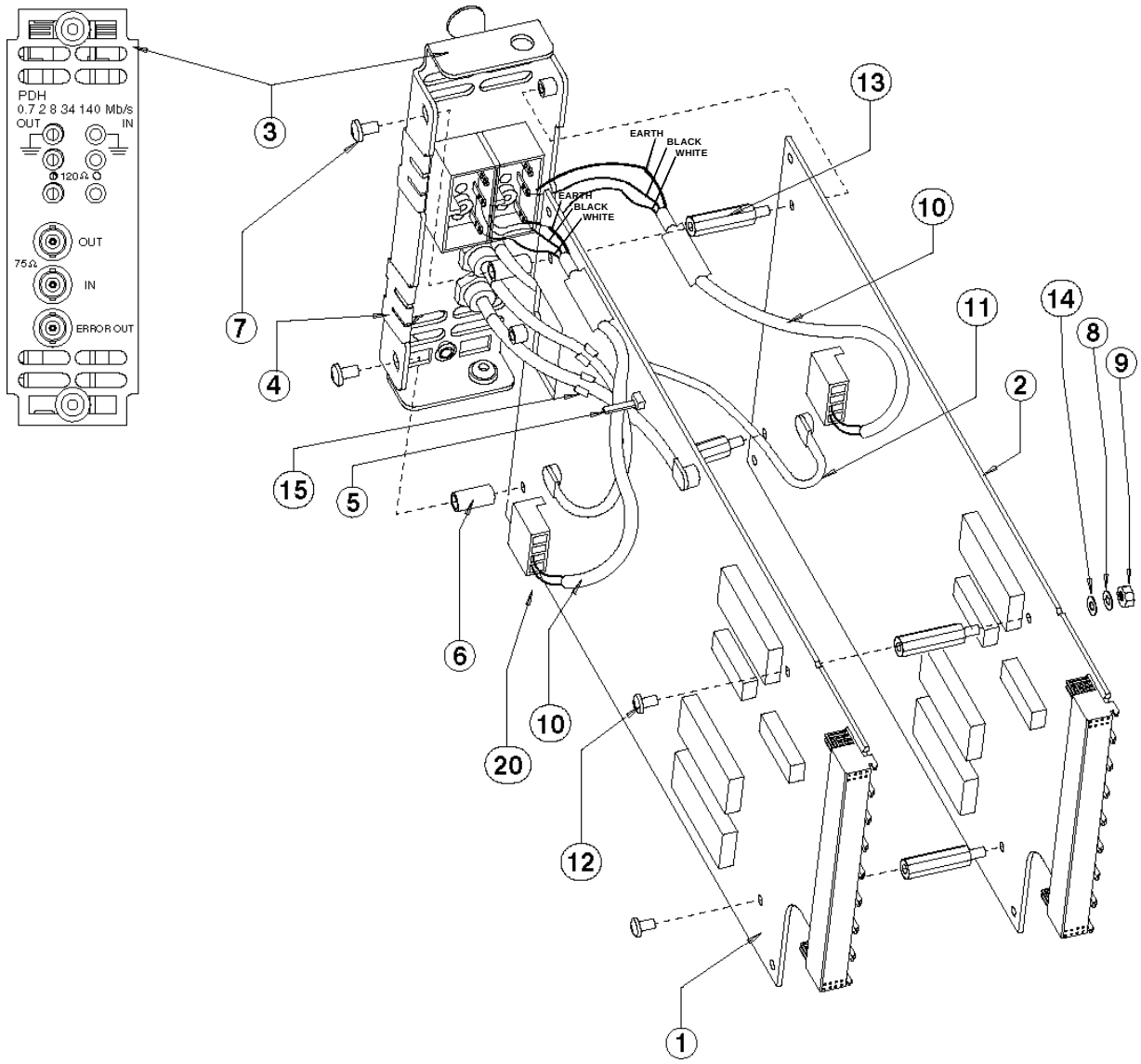

Figure 4-5 Unstructured PDH Module - Exploded View

Table 4-8 Unstructured PDH Module Parts List

Description	HP Part No.	Qty	Item
PDH Recvr PCAB	37714-60006	1	1
PDH Tx PCAB	37714-60007	1	2
Panel PDH	37714-00008	1	3
Panel PDH (small Siemens)	37714-00019	1	3
Clip Spring	5180-0409	2	4
Cable Tie	1400-0307	3	5
Spacer	0380-0008	2	6
SCR Mch M3 x 20mm	0515-1441	2	7
Washer LCK M3	2190-0584	2	8
Nut M3	0535-0025	2	9
Cbl 3-pin Siemens (includes screw-nut)	37714-60021	2	10
Cbl-Asy BNC FL-75	37721-60025	3	11
Cbl-Asy FL-75 (small Siemens)	37721-60030	1	11
SCR MC M3 x 6mm	0515-0886	2	12
Std Offhx M3 x 22 M/F	0380-2082	4	13
Flat Washer	3050-0891	2	14
Cable Clamps	1400-1617	2	15
Serrated Washer	2190-0016	3	16
Block	37724-20001	2	17
Screw	0515-1427	1	18
Nut	0535-0026	1	19
Capacitor	0160-4389	1	20
Fuse 0.125A 250V	2110-0671	3	N/S
Fuse 1.00A 125V	2110-0665	1	N/S

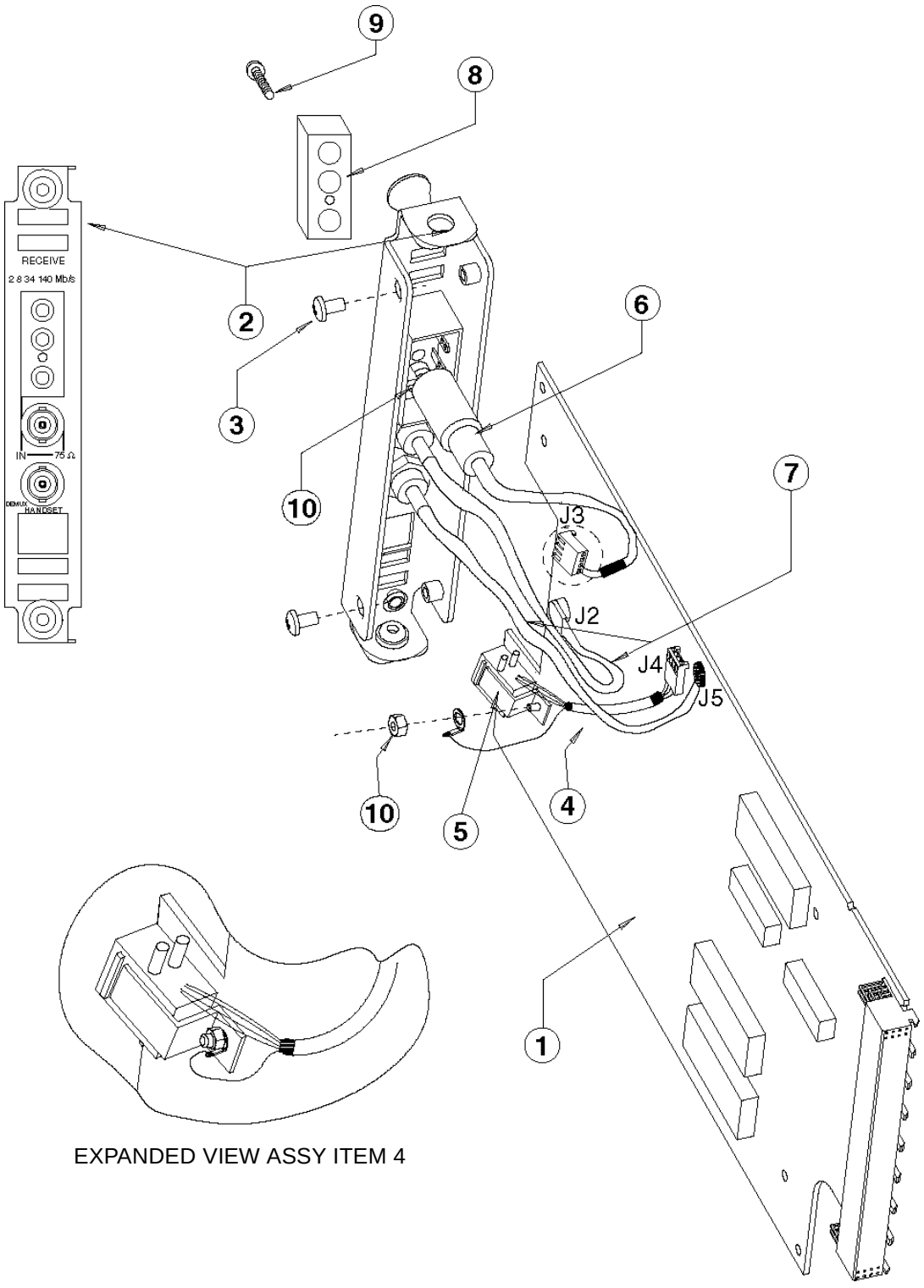

Figure 4-6 Structured PDH Receiver Module - Exploded View

Table 4-9 Structured PDH Receiver Module Parts List

Description	HP Part No.	Qty	Item
PDH Recvr PCAB	37717-60004	1	1
Panel SPDH Rx	37717-00011	1	2
Panel SPDH Rx (small Siemens)	37717-00012	1	2
SCR MC M3 x 6mm	0515-0886	2	3
Cbl Assy HDST Jak	37717-60022	1	4
Bracket	37717-00016	1	5
Cbl 3-pin Siemens	37714-60021	1	6
Cbl-Asy BNC FL-75	37721-60025	2	7
Cbl-Asy FL-75 (small Siemens)	37721-60030	1	7
Block	37724-20001	1	8
Screw	0515-1427	1	9
Nut	0535-0026	2	10
Serrated Washer	2190-0016	2	11
Fuse 0.125A 250V	2110-0671	1	N/S

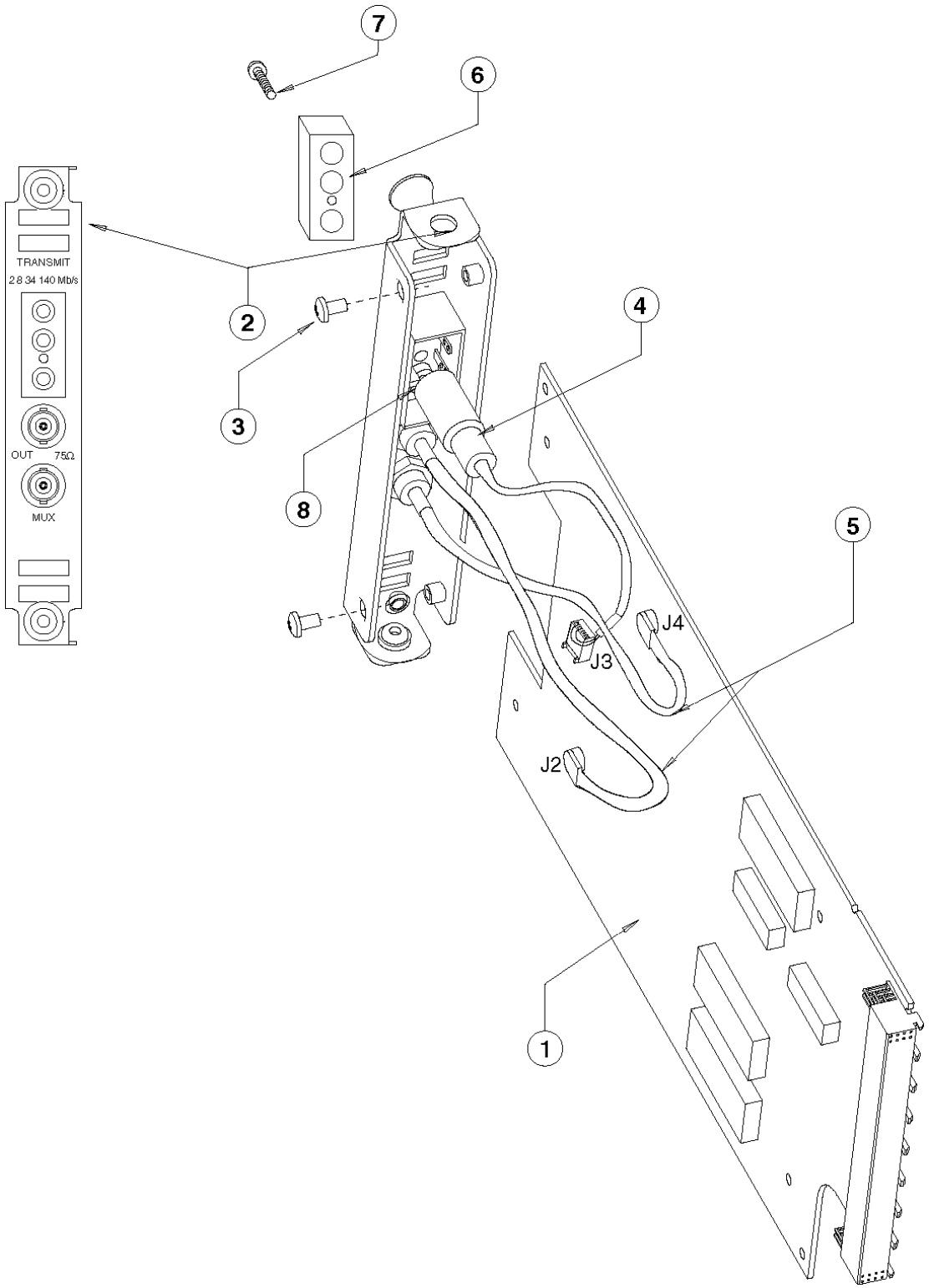

Figure 4-7 Structured PDH Transmitter Module - Exploded View

Table 4-10 Structured PDH Transmitter Module Parts List

Description	HP Part No.	Qty	Item
PDH Recvr PCAB	37717-60005	1	1
Panel SPDH/ATM Tx	37717-00009	1	2
Panel SPDH Tx (small Siemens)	37717-00010	1	2
SCR MC M3 x 6mm	0515-0886	2	3
Cbl 3-pin Siemens	37714-60021	1	4
Cbl-Asy BNC FL-75	37721-60025	2	5
Cbl-Asy FL-75 (small Siemens)	37721-60030	1	5
Block	37724-20001	1	6
Screw	0515-1427	1	7
Nut	0535-0026	1	8
Serrated Washer	2190-0016	2	9
Fuse 0.125A 250V	2110-0671	1	N/S

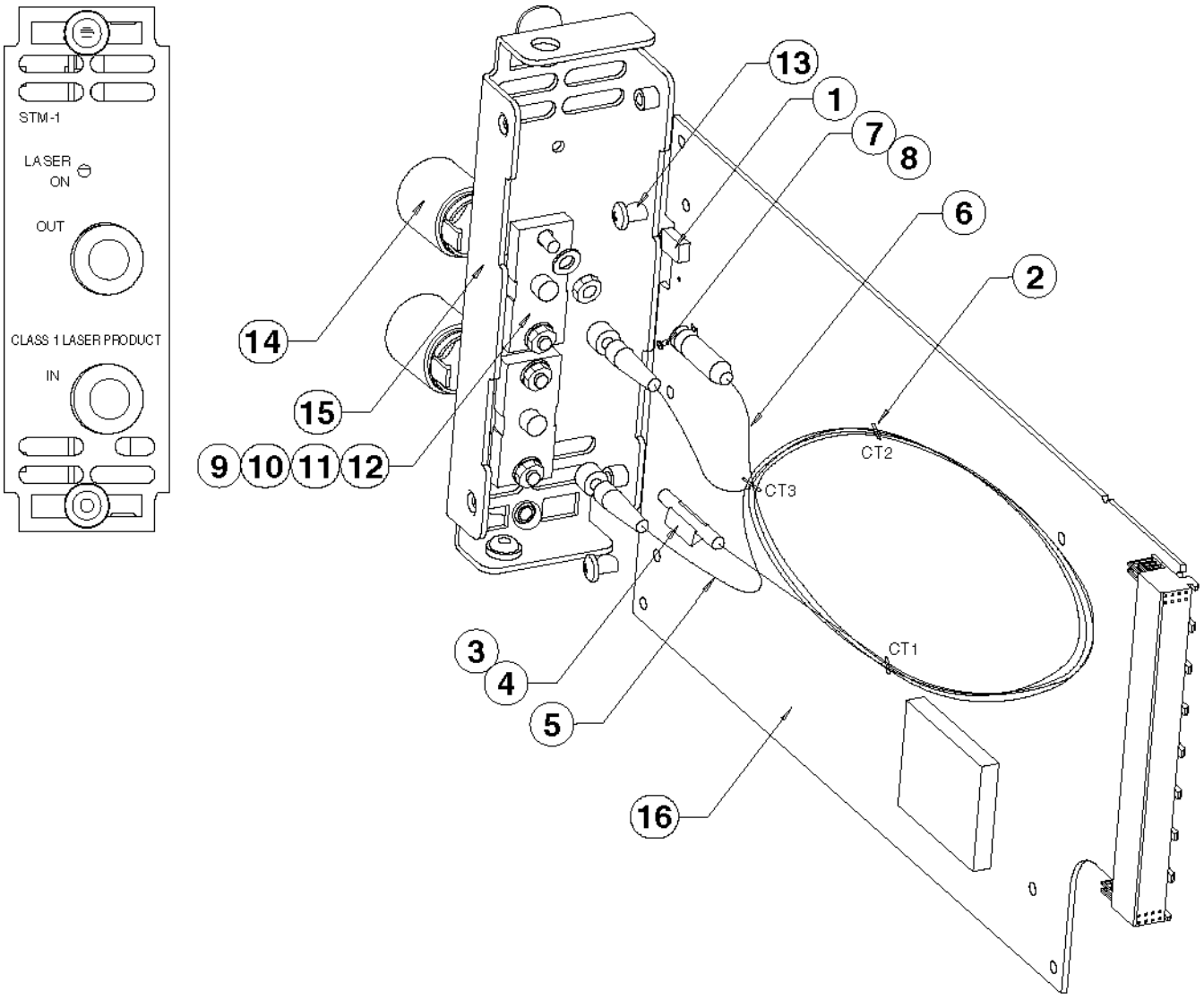

Figure 4-8 Option UH1 1310nm STM-1 Optics Module - Exploded View

Table 4-11 Option UH1 1310nm STM-1 Optics Module Parts List

Description	HP Part No.	Qty	Item
Led Yel -4584	1990-0487	1	1
Saddle Wire .27WD	1400-1567	3	2
Clip-Cmpnt	1400-0494	1	3
Loctite Output 384	0470-1911	1	4
F/O Pin-Tia	1005-0241	1	5
F/O Coax Laser	1005-0240	1	6
Screw M2 x 6.0 LG	0515-0888	2	7
Nut HX M2 STL + ZN	0535-0069	2	8
Insul FLG-BSHG	0340-0418	4	9
Bushing Optical	E1661-24102	2	10
Washer LK M3	2190-0584	4	11
Nut M3	0535-0025	4	12
SC Mach M3 16mm	0515-1111	2	13
Shutter Assy	08145-64521	2	14
Panel Optic	37714-00010	1	15
STM1 Opt	37714-60011	1	16

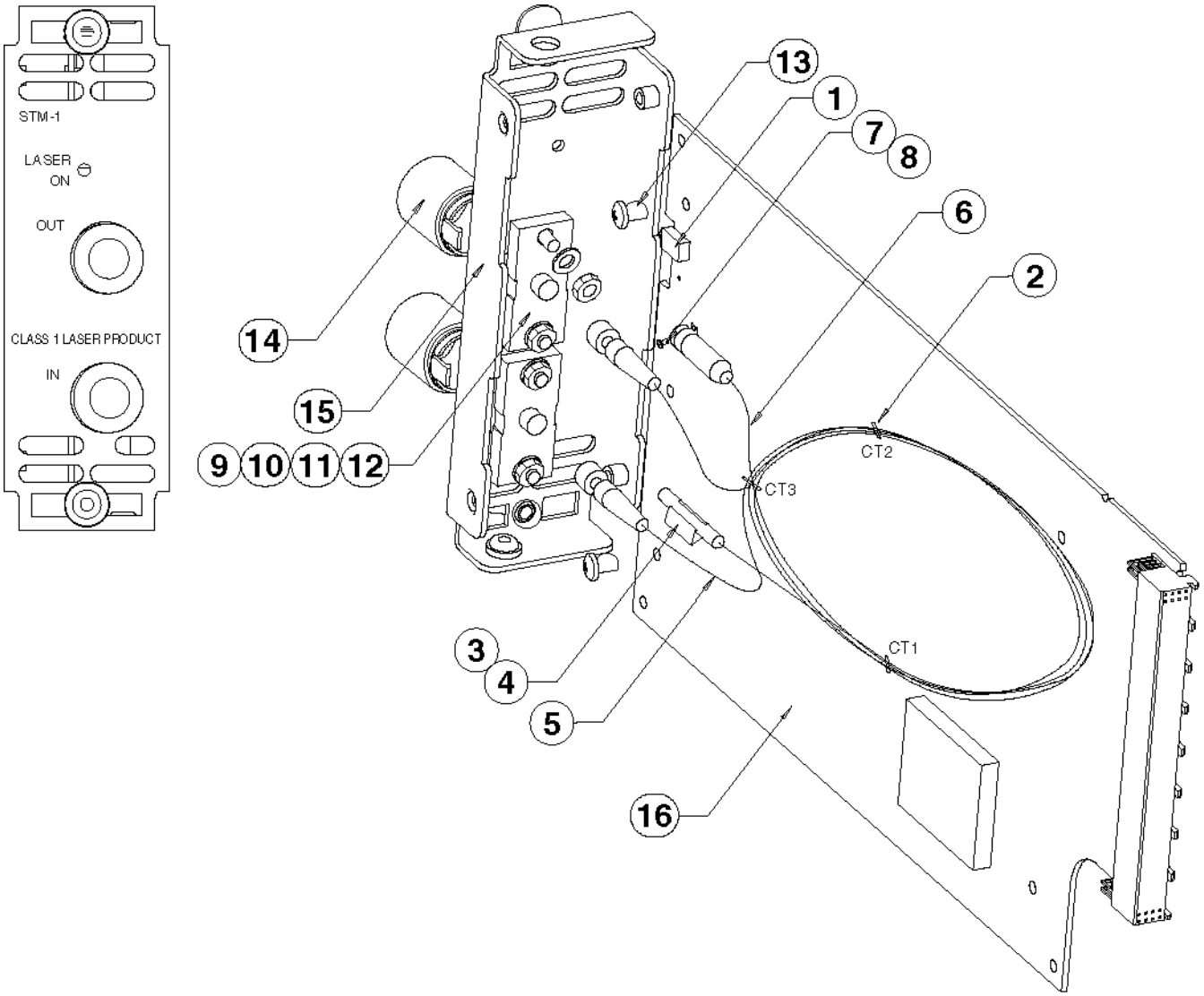

Figure 4-9 Option UH2 1310nm STM-1/4 Optics Module - Exploded View

Table 4-12 Option UH2 1310nm STM-1/4 Optics Module Parts List

Description	HP Part No.	Qty	Item
Led Yel -4584	1990-0487	1	1
Saddle Wire	1400-1617	1	2
Clip-Cmpnt	1400-0494	1	3
Screen Lid	37717-00014	1	N/S
F/O Pin-Tia	1005-0266	1	5
F/O Coax Laser	1005-0240	1	6
Screw M2 x 6.0 LG	0515-0888	2	7
Nut HX M2 STL + ZN	0535-0069	2	8
Insul FLG-BSHG	0340-0418	4	9
Bushing Optical	E1661-24102	2	10
Washer LK M3	2190-0584	4	11
Nut M3	0535-0025	4	12
SC Mach M3 16mm	0515-1111	2	13
Shutter Assy	08145-64521	2	14
Panel Optic	37714-00011	1	15
STM1/4 Opt	37714-60013	1	16
Fan Assembly	37776-60016	1	N/S

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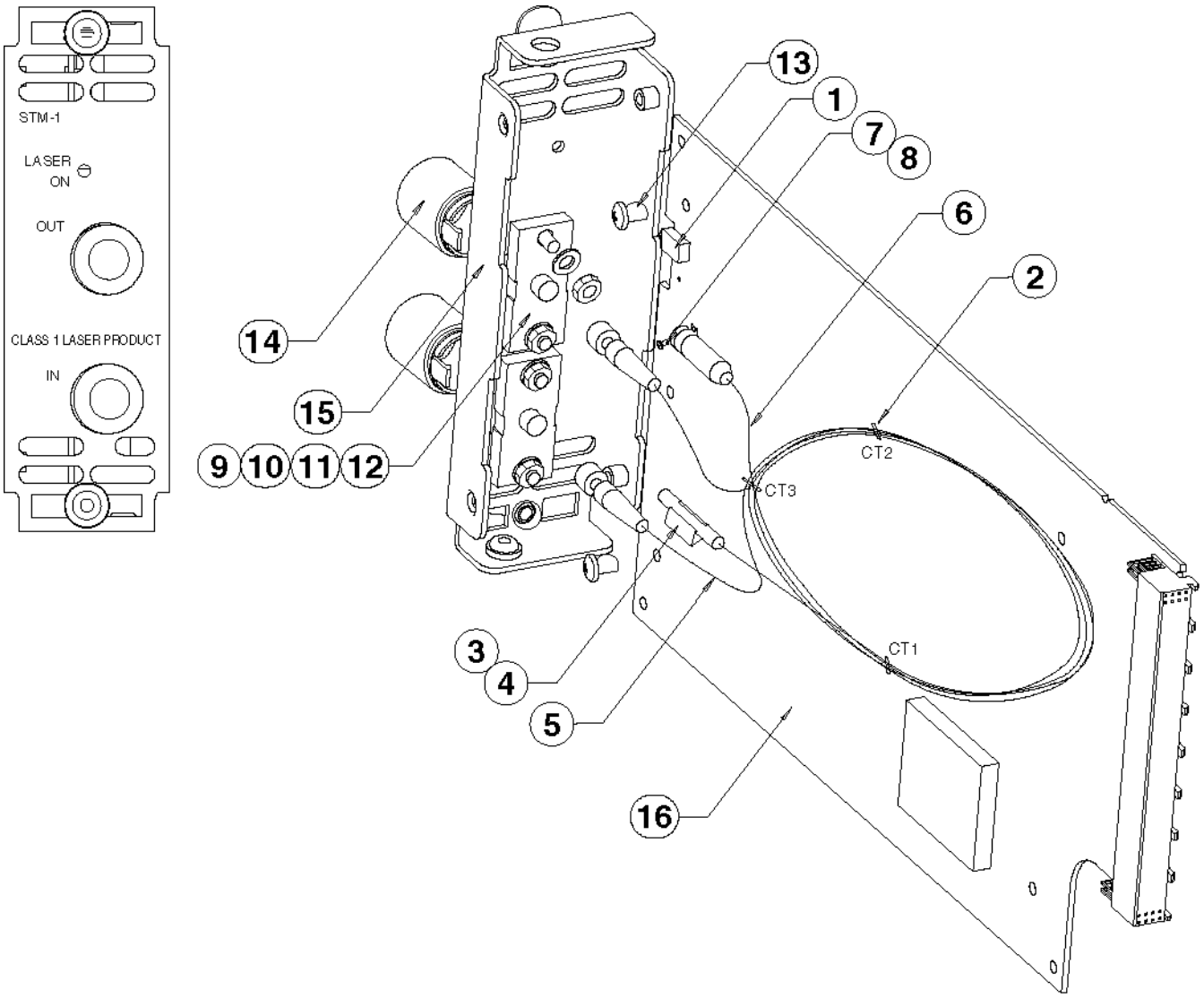


Figure 4-10 Option URU 1550nm STM-1 Optics Module - Exploded View

Table 4-13 Option URU 1550nm STM-1 Optics Module Parts List

Description	HP Part No.	Qty	Item
Led Yel -4584	1990-0487	1	1
Saddle Wire	1400-1617	1	2
Clip-Cmpnt	1400-0494	1	3
Screen Lid	37717-00014	1	N/S
F/O Pin-Tia	1005-0266	1	5
F/O Coax Laser	1005-0240	1	6
Screw M3 x 6.0 LG	0515-0890	3	N/S
Screw M3 x 22 LG	0515-1643	1	N/S
Nut HX M2 STL + ZN	0535-0069	2	8
Insul FLG-BSHG	0340-0418	4	9
Bushing Optical	E1661-24102	2	10
Washer LK M3	2190-0584	4	11
Nut M3	0535-0025	4	12
SC Mach M3 16mm	0515-1111	2	13
Shutter Assy	08145-64521	2	14
Panel Optic	37714-00026	1	15
STM1/4 Opt	37714-60012	1	16
Fan Assembly	37776-60016	1	N/S
Thermal Insulator	37776-00017	1	N/S
Cable Assy	37714-60022	1	N/S
Laser Heatsink	37714-20022	1	N/S

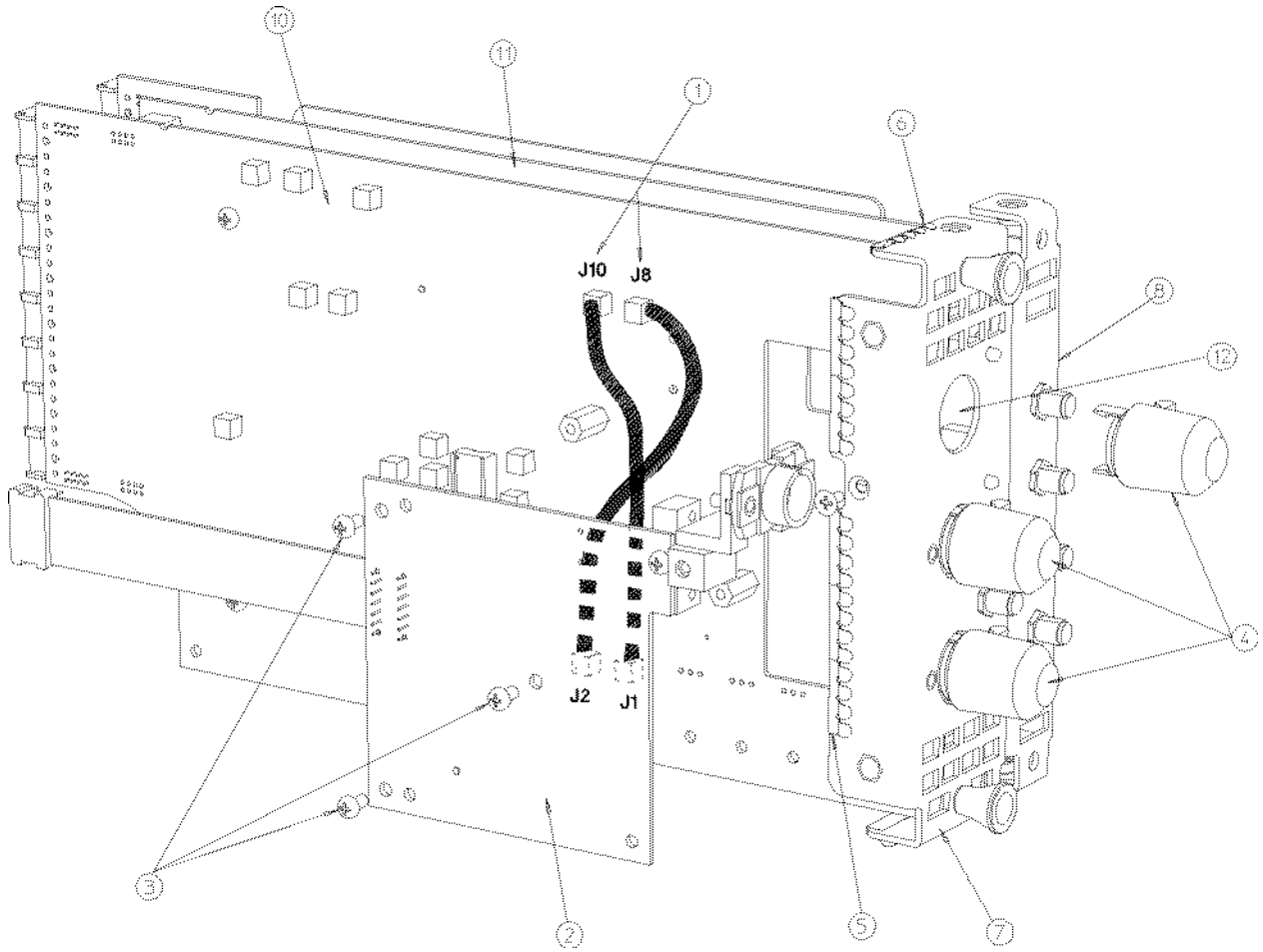


Figure 4-11 Option UKT/USN STM 1/4 Optical Module- Exploded View (Front)

Table 4-14 Option UKT/USN STM 1/4 Optical Module Parts List

Description	HP Part No.	Qty	Item
STM1/4 Optical Module	37714-60071	1	-
Coaxial Cable Assy.	70843-60078	2	1
1550nm Transmit Assy. (1)	37714-60067	1	2
Screw Machine M3x6mm	0515-0886	3	3
Optical Shutter	08145-64521	3	4
RFI Gasket	8160-0876	-	5
RFI Gasket	8160-0884	-	6
Optical Module Front Panel	37714-00039	1	7
SDH Binary Interface Module (3)	37714-60074	1	8
Screw CSK M3x6	0515-0890	1	9
Optical Assy.	37714-60063	1	10
Digital Assy.	37714-60064	1	11
Blanking Plug (2)	6960-0003	1	12
Coaxial Cable Assy. (4)	E1669-64207	1	13
Coaxial Cable Assy.(4)	E1669-64208	1	14
Coaxial Cable Assy.(4)	70843-60076	2	15
Coaxial Cable Assy.(4)	E1669-64217	1	16
Led Yellow	1990-0487	2	17

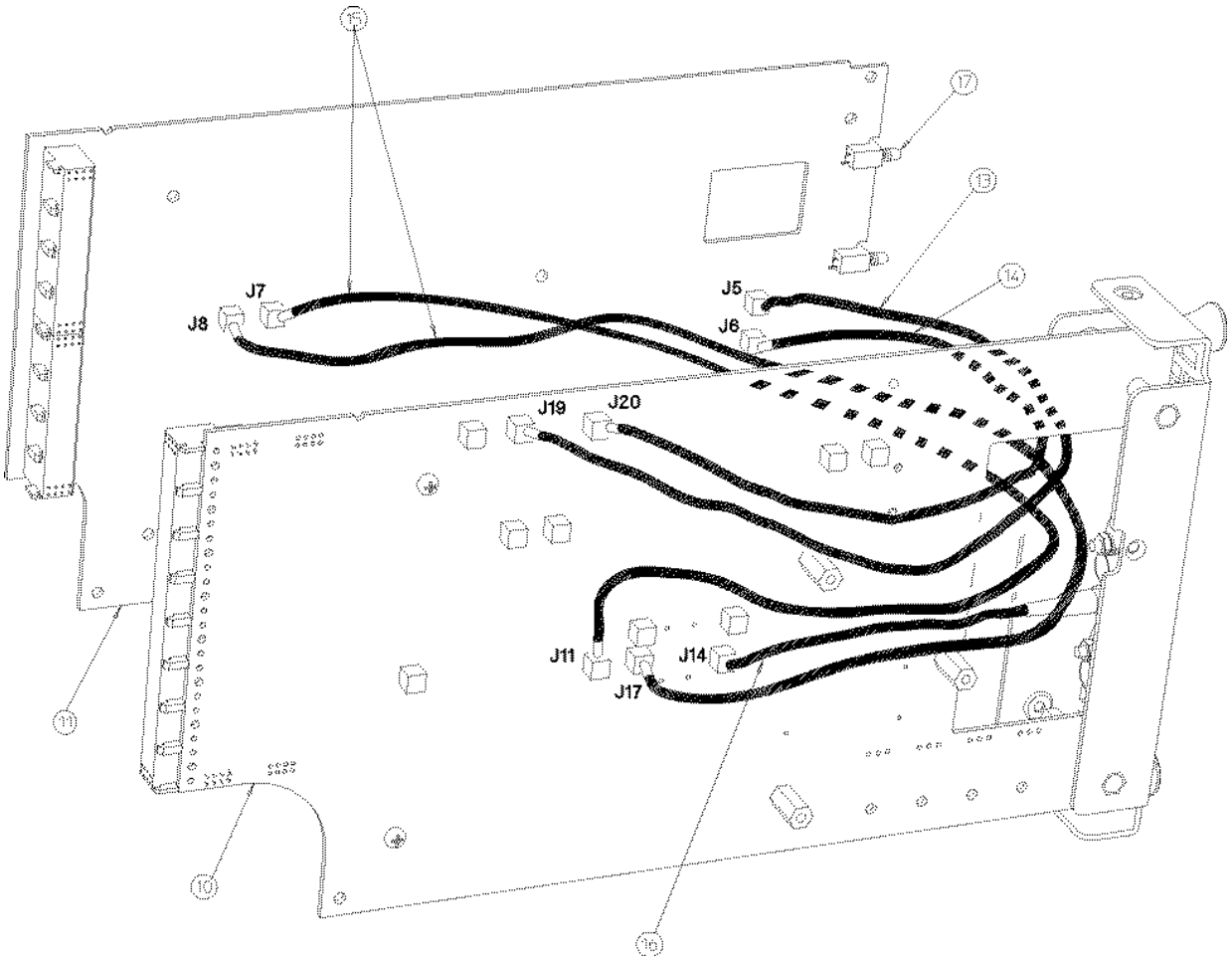


Figure 4-12 Option UKT/USN STM 1/4 Optical Module - Exploded View (Rear)

For Parts List see Table 4-14 on Page 4-27.

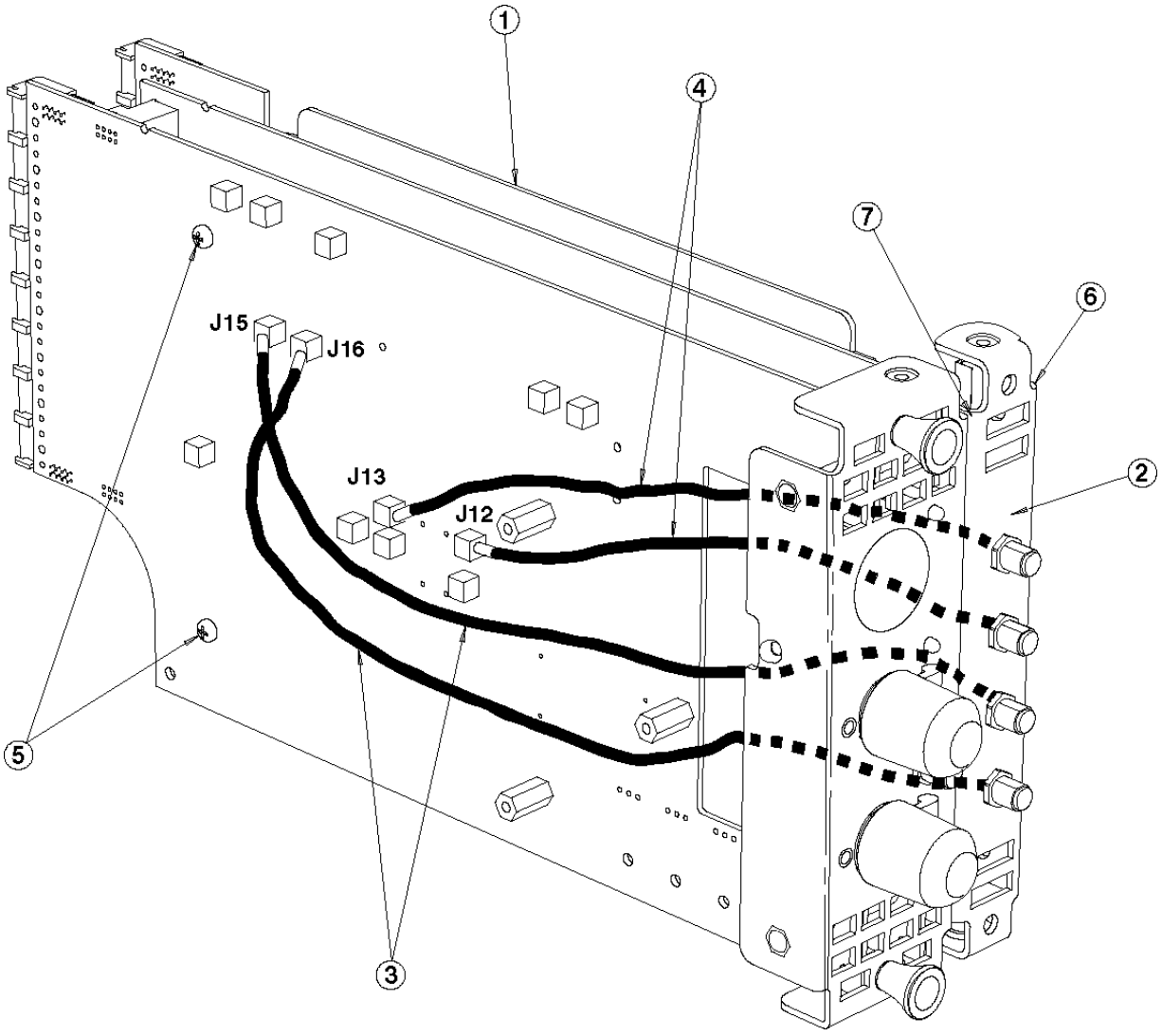


Figure 4-13 SDH Binary Interface Module - Exploded View

Table 4-15 SDH Binary Interface Module Parts List

Description	HP Part No.	Qty	Item
SDH Binary Interface Module	37714-60074	1	-
Binary Interface Assy.	37714-60066	1	1
Binary Module Front Panel	37714-00040	1	2
Coax Cable Assy	E1685-64217	2	3
Coax Cable Assy	E1669-64202	2	4
Screw Sc Machine M3x6mm	0515-0886	-6	5
RFI Gasket	8160-0876	-	6
RFI Channel Strip	8160-0616	-	7

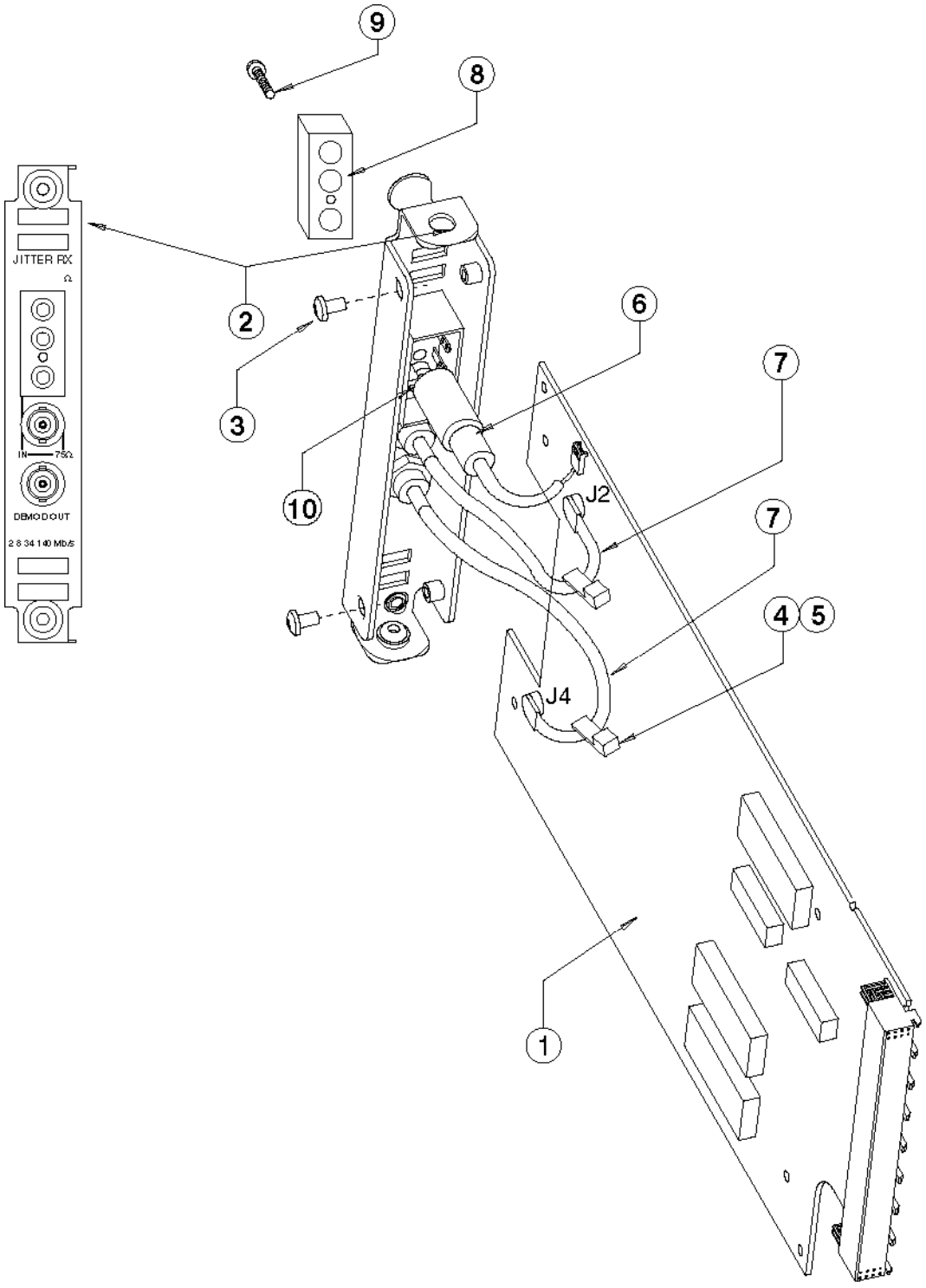


Figure 4-14 Option UHN Jitter Rx Module - Exploded View

Table 4-16 Option UHN Jitter Rx Module Parts List

Description	HP Part No.	Qty	Item
PDH Recvr PCAB	37717-60006	1	1
Panel Jitter Rx	37717-00008	1	2
Panel Jitter Rx (small Siemens)	37717-00006	1	2
SCR MC M3 x 6mm	0515-0886	2	3
Cable Clamps	1400-1617	2	4
Cable Tie	1400-0307	2	5
Cbl 3-pin Siemens	37714-60021	1	6
Cbl-Asy BNC FL-75	37721-60025	2	7
Cbl-Asy FL-75 (small Siemens)	37721-60030	1	7
Block	37724-20001	1	8
Screw	0515-1427	1	9
Nut	0535-0026	2	10
Serrated Washer	2190-0016	2	11
Fuse 0.125A 250V	2110-0671	1	N/S

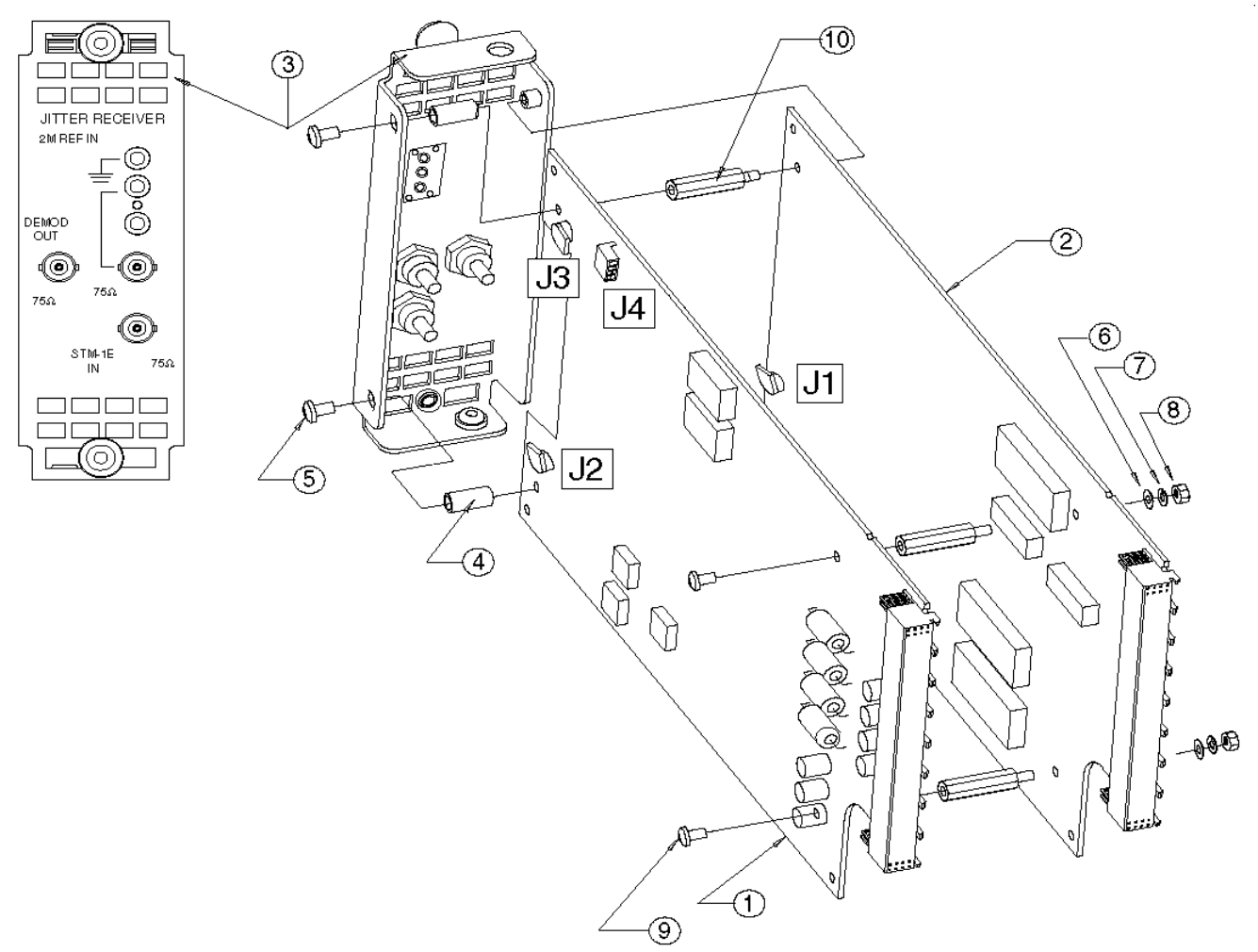


Figure 4-15 A1M STM -1e Jitter Rx Module - Exploded View

Table 4-17 Option A1M STM -1e Jitter Rx Module - Replaceable Parts List

Description	HP Part No.	Qty	Item
Option A1M STM-1E Jitter Rx Module - (see Note 1)	37717-60033	1	N/A
Option A1Q STM-1E Jitter Rx Module - (see Note 1)	37717-60034	1	N/A
STM-1E Jitter Rx Board Assy	37717-60016	1	1
Clock Board Assy (see Note 1)	37714-60014	1	2
Front Panel Assembly (BNC)	37714-60090	1	3
Front Panel Assembly (small Siemens)	37714-60091	1	3
Spacer	0380-0008	2	4
Screw machine M3 x 20mm	0515-1441	2	5
Plain Washer M3 x 0.5	3050-0891	2	6
Lock Washer M3	2190-0584	2	7
Nut M3	0535-0025	2	8
Screw machine M3 x 6mm	0515-0886	2	9
Standoff	0380-2082	8	10

NOTE

1. Modules with Build Status 2:18 and above (nominal) have modification to the Clock Board assembly (HP2 Filter now conforms to G825).

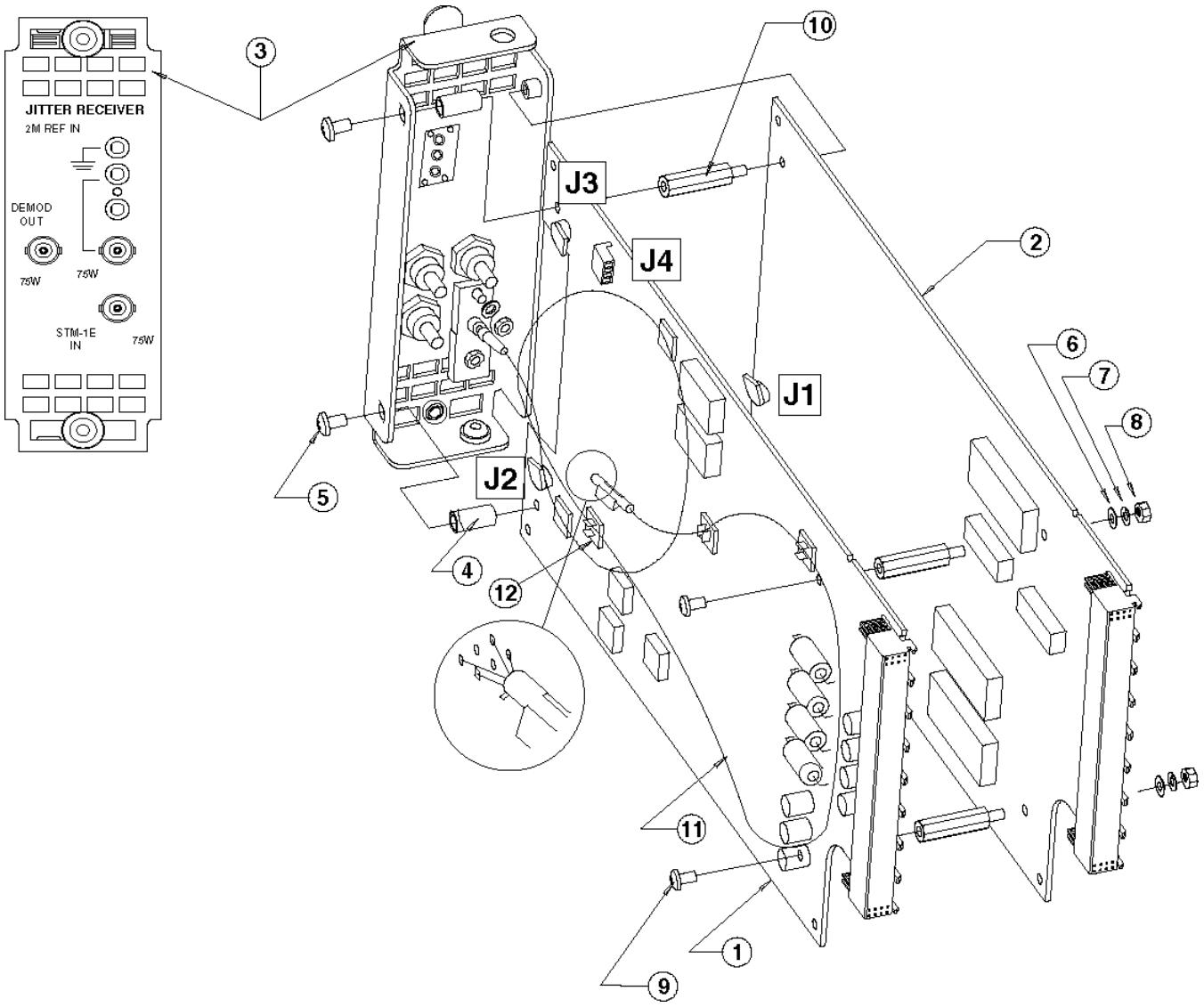


Figure 4-16 A1N/A1R STM1/4 - e/o Jitter Rx Module - Exploded View

Table 4-18 Option A1N/A1R STM1/4 e/o Jitter Rx Module Replaceable Parts List

Description	HP Part No.	Qty	Item
Option A1N STM-1E-O Jitter Rx Module - (see Note 1)	37717-60046	1	N/A
Option A1R STM-1E-O Jitter Rx Module - (see Note 1)	37717-60047	1	N/A
STM-1 Optical Jitter Rx Board Assy	37717-60017	1	1
Clock Board Assy (see Note 1)	37714-60014	1	2
Option A1N Front Panel Assembly (BNC)	37714-60089	1	3
Option A1R Front Panel Assembly (small Siemens)	37714-60092	1	3
Spacer	0380-0008	2	4
Screw machine M3 x 20mm	0515-1441	2	5
Plain Washer M3 x 0.5	3050-0891	2	6
Lock Washer M3	2190-0584	2	7
Nut M3	0535-0025	2	8
Screw machine M3 x 6mm	0515-0886	2	9
Standoff	0380-2082	8	10
Optical Receiver F/O PIN TIA 155	1005-0361	1	11
Cable Clamp	1400-1617	1	12
Coaxial Cable	37717-60065	1	
Coaxial Cable	37721-60025	3	
Optical Bushing	E1661-24102	1	
Optical Shutter Assembly	08145-64521	1	

NOTE

1. Modules with Build Status 2:18 and above (nominal) have modification to the Clock Board assembly (HP2 Filter now conforms to G825).

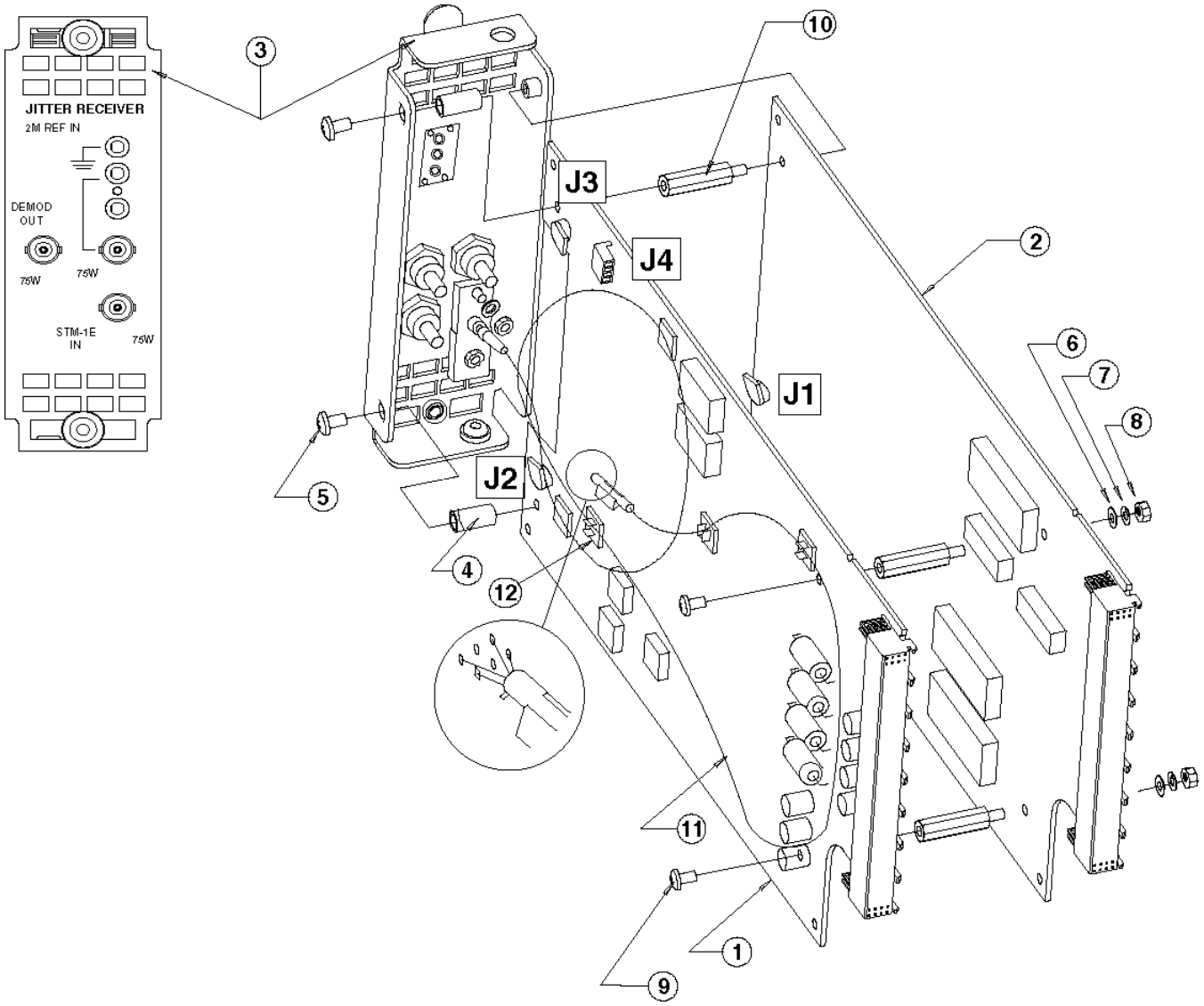


Figure 4-17 Option A1P STM1/4 - e/o Jitter Rx Module - Exploded View

Table 4-19 Option A1P STM1/4 - e/o Jitter Rx Module Replaceable Parts List

Description	HP Part No.	Qty	Item
Option A1P STM-1/4E-O Jitter Rx Module - (see Note 1)	37717-60048	1	N/A
Option A1S STM-1/4E-O Jitter Rx Module - (see Note 1)	37717-60049	1	N/A
STM-1/4 Optical Jitter Rx Board Assy	37717-60015	1	1
Clock Board Assy (see Note 1)	37714-60014	1	2
Option A1P Front Panel Assembly (BNC)	37714-60089	1	3
Option A1S Front Panel Assembly (small Siemens)	37714-60092	1	3
Spacer	0380-0008	2	4
Screw machine M3 x 20mm	0515-1441	2	5
Plain Washer M3 x 0.5	3050-0891	2	6
Lock Washer M3	2190-0584	2	7
Nut M3	0535-0025	2	8
Screw machine M3 x 6mm	0515-0886	2	9
Standoff	0380-2082	8	10
Optical Receiver F/O PIN TIA 622	1005-0361	1	11
Cable Clamp	1400-1617	1	12
Coaxial Cable	37717-60065	1	
Coaxial Cable	37721-60025	3	
Optical Bushing	E1661-24102	1	
Optical Shutter Assembly	08145-64521	1	

NOTE 1. Modules with Build Status 2:18 and above (nominal) have modification to the Clock Board assembly (HP2 Filter now conforms to G825).

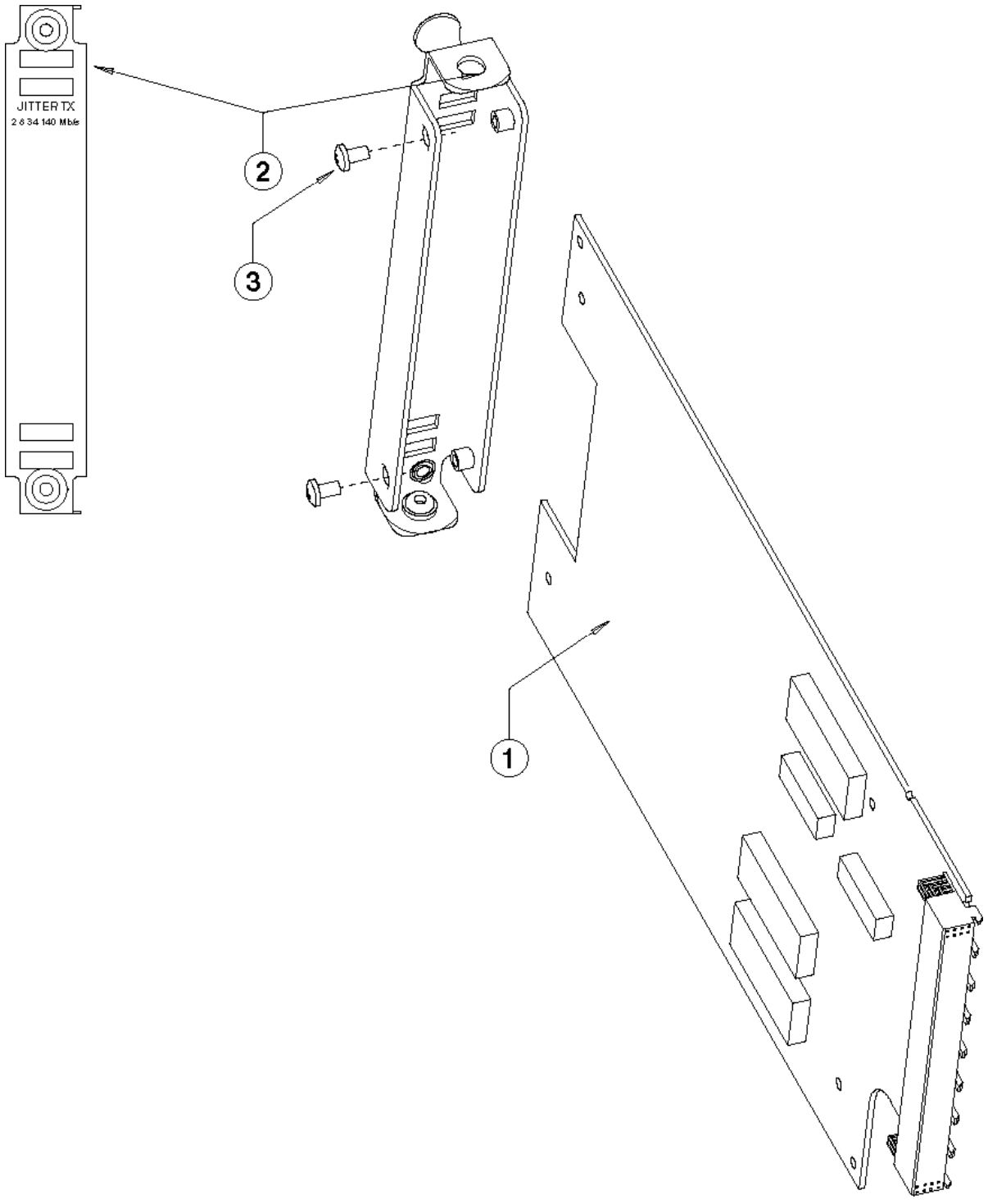


Figure 4-18 Option UHK Jitter Tx Module - Exploded View

Table 4-20 Option UHK Jitter Tx Module Parts List

Description	HP Part No.	Qty	Item
PDH Recvr PCAB	37717-60008	1	1
Panel Jitter Tx	37717-00007	1	2
SCR MC M3 x 6mm	0515-0886	2	3

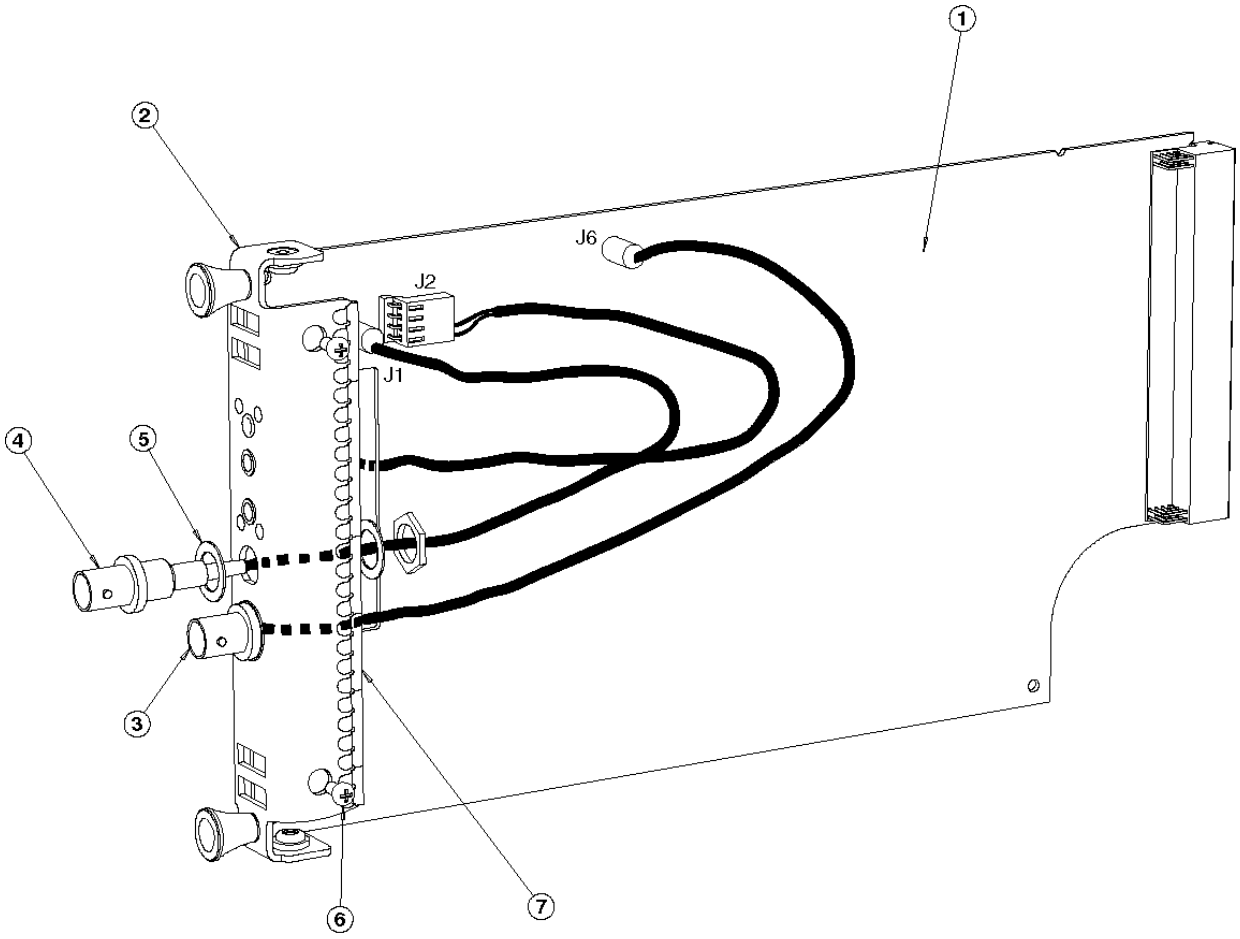


Figure 4-19 Option A3K Jitter and Wander Transmitter Module - Exploded View

Table 4-21 A3K Jitter and Wander Transmitter Module Replaceable Parts List

Description	HP Part No.	Qty	Item
A3K Jitter and Wander Transmitter Module	37717-60105	1	-
Jitter Tx Interface PLA	37717-60094	1	1
Front Panel Assy.	37717-60118	1	2
Cable Assy. (BNC)	37721-60025	1	3
Cable Assy. (BNC)	37721-60025	1	4
Lock Washer	2190-0016	2	5
Pan Head Screw M3x6mm	0515-0886	2	6
RFI Gasket	8160-0876	-	7

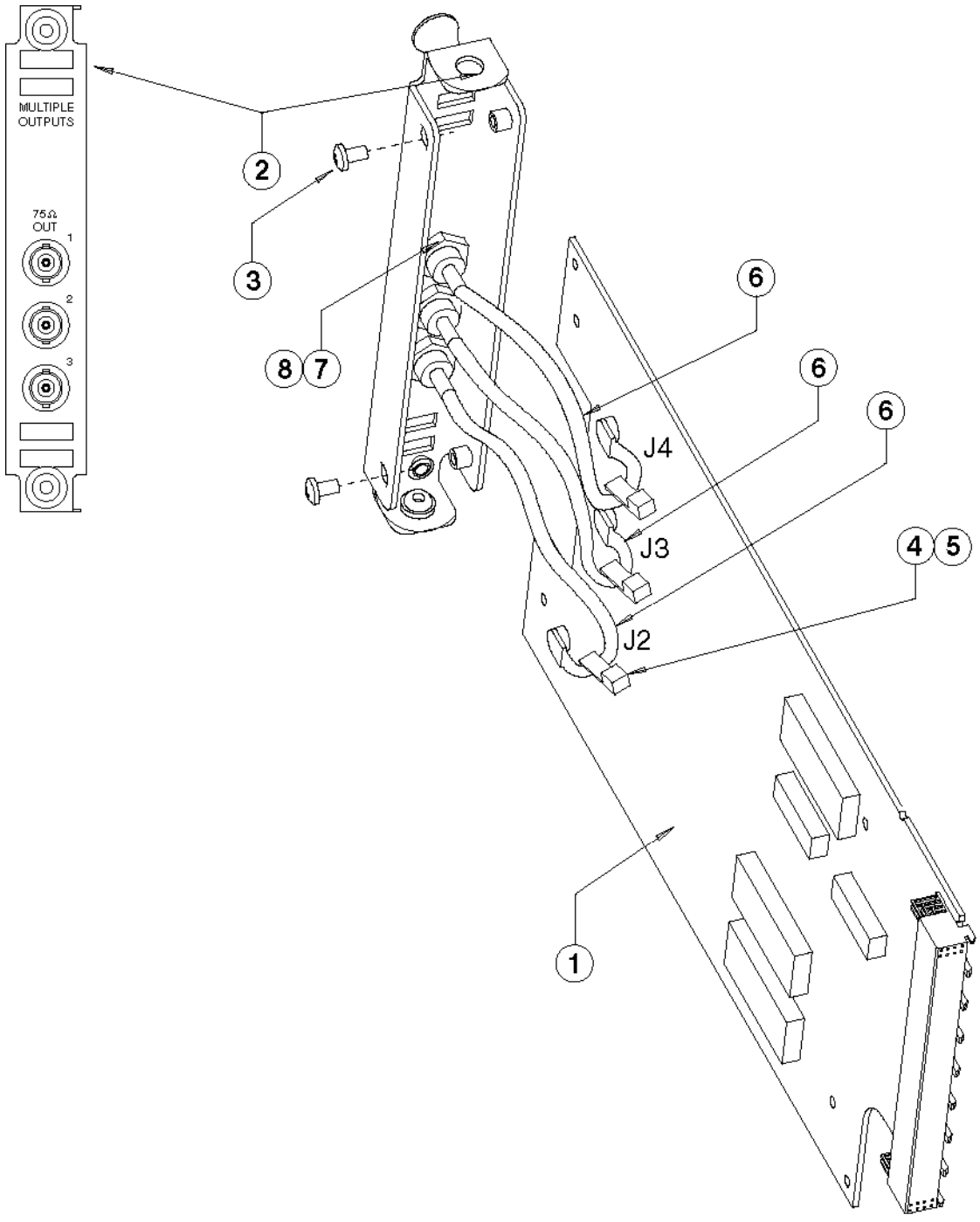


Figure 4-20 Option UHC Multiple Output Module - Exploded View

Table 4-22 Option UHC Multiple Output Module Parts List

Description	HP Part No.	Qty	Item
Mult O/P PCAB	37714-60014	1	1
Panel Mult Output (BNC)	37714-00021	1	2
Panel Mult Output (small Siemens)	37714-00022	1	2
SCR MC M3 x 6mm	0515-0886	2	3
Cable Clamps	1400-1617	3	4
Cable Tie	1400-0307	3	5
Cbl-Asy BNC FL-75	37721-60025	3	6
Cbl-Asy FL-75 (small Siemens)	37721-60030	3	6
Nut	0535-0026	3	7
Serrated Washer	2190-0016	3	8
Fuse 1.0A 125V	2110-0665	1	N/S
Fuse 0.125A 250V	2110-0671	3	N/S

5

Service

Theory of Operation

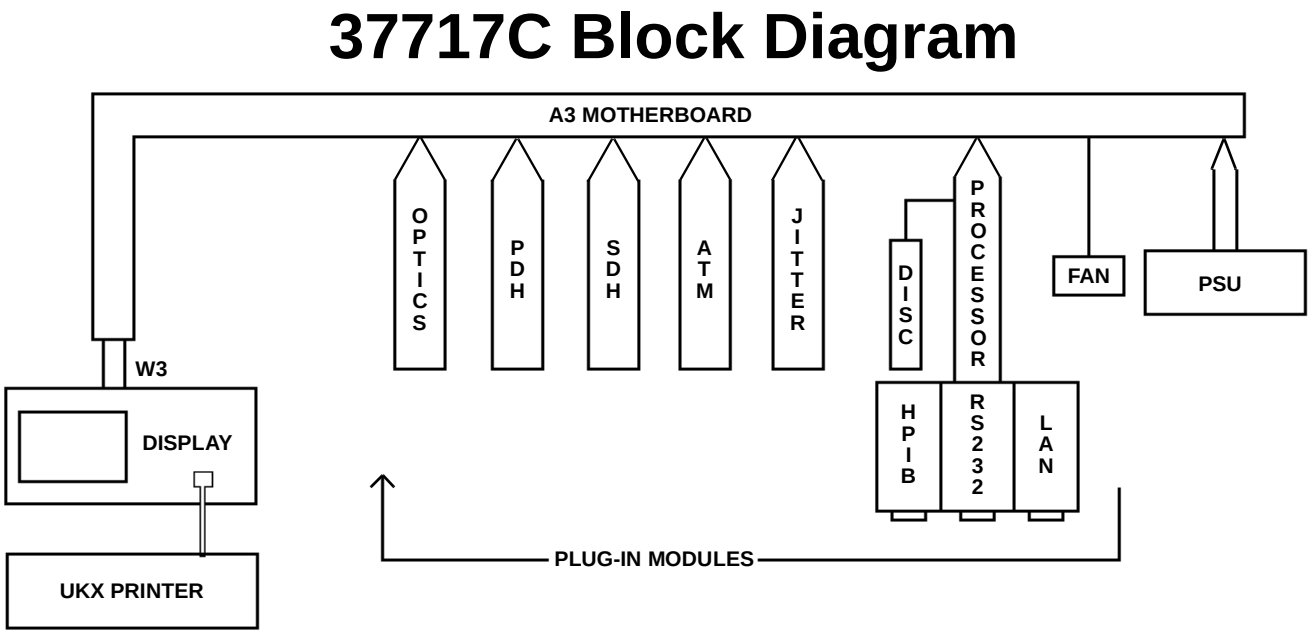


Figure 5-1 The 37717C Block Diagram

General

The HP 37717C is one of the range of Telecommunications Test products from Hewlett-Packard. It is used in testing both electrical and optical interfaces at PDH/DSn and SONET/SDH rates. It is also useful in testing ATM networks and network equipment (including generation and measurement of jitter).

The Analyzer comprises a mainframe with a large colour display, disc drive and optional 80-column Printer. Single and double width Plug-in modules are added to meet the customer's requirements for the various test functions.

Introduction

A block diagram of the HP 37717C is shown in Figure 5-1. The A3 motherboard is the main communication highway between all other modules in the HP 37717C. These are:

PSU

This is an OEM supplied Power Supply which takes 90 to 250 Vac mains line input and supplies all necessary dc power requirements to the HP 37717C.

Fan

This is a barrel fan which runs the length of the A3 motherboard and cools all the modules in the instrument. It is supplied by 12 Vdc from the PSU and is therefore a useful first indicator that the PSU is at least partially operational.

CPU

This is a double width plug-in module and is always installed immediately to the left of the PSU. It contains the main control processor for the HP 37717C together with the floppy disc drive, RS-232, HP-IB and LAN ports. It communicates directly with all the plug-ins and outputs data to the colour display and /or optional Printer via the A3 motherboard and W3 ribbon cable.

A floppy disc drive is fitted to load update firmware and store result files on floppy disc. Interfaces to RS-232, HP-IB and LAN communication ports are also available as options.

On board flash EEPROM contains calibration data for the various plug-in modules together with the Option structure peculiar to the particular HP 37717C the CPU is installed in.

Other Plug-in Modules

Plug-in modules are available for various functions as T-Carrier, PDH (structured and unstructured), SDH, SONET, ATM Jitter and LAN testing. These are explained more fully in their relevant sections. Repair is by PCA (or module) replacement.

Display/Keyboard

The colour Display and keyboard provides the main operator interface to the HP 37717C. It is connected to the main A3 motherboard via ribbon cable WX.

The display is an assembly consisting of a colour electroluminescent display, a membrane keyboard and three PCA assemblies. The complete unit is available as an exchange assembly although the lower level PCA assemblies are available if required.

In Lid Printer

This is an 80 column graphics Printer which plugs into the front panel of the HP 37717C. A flip up cover allows paper replacement and viewing of the three status LEDS. There are no serviceable parts within the unit and the Printer must be replaced as a unit if suspected to be faulty.

Self Tests

Self tests are available for each plug-in module which should give approximately 90 per cent confidence that the unit is fully functional.

General Information

Introduction

This section contains information to help troubleshoot and repair the Hewlett-Packard Model HP 37717C Communications Performance Analyzer. The information is organized into subsections as follows:

- **General Information** - Introduction, Safety Considerations, Anti-static Precautions and Repair Strategy.
- **Built-in Service Features** - Describes Self-Test and other Troubleshooting features.
- **General Service Sheets** - Contain Assembly Level troubleshooting information.
  G1 is the start-point for all troubleshooting and will lead to other General Service Sheets (G-Sheets) which isolate the faulty assembly.
- **Dismantling Procedures** - Provides procedures for removing and refitting Modules and board assemblies.

Safety Considerations

The HP 37717C is designed in accordance with international safety standards. However potentially lethal voltages are present in the Power Supply Units. Maintenance should only be carried out by qualified Service Personnel who are aware of the fire and electric shock hazards involved.

WARNING **PROCEDURES DESCRIBED IN THIS SECTION ARE PERFORMED WITH POWER SUPPLIED AND PROTECTIVE SHIELD COVERS REMOVED. REPAIRS SHOULD ONLY BE PERFORMED BY SERVICE TRAINED PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED.**

WARNING **To protect operating personnel, the instrument chassis must be grounded. Provide Line power using only approved cables, plugs and sockets.**

Anti-static Precautions

The Board assemblies used in this instrument contain components and devices which are susceptible to damage by electrostatic discharge (ESD). To minimise the risk of ESD damage, the following precautions should be observed when servicing the HP 37717C.

- Static-free Workstation: Perform servicing only at a designated static-free workstation.
- Soldering: Soldering irons must be properly earthed (grounded). Always use metallized solder removers.
- Freezer Spray: Temperature related faults should be located using only an approved ant-static freezer spray.
- Anti-Static Products: The following anti-static products are available from Hewlett-Packard.

Product	HP Part No.
Anti-static Workstation	9300-0792
Metallized Solder Remover	8690-0227
Wrist-strap and Cord	9300-0970

Repair Strategy

The HP 37717C use an Assembly-Level troubleshooting/repair strategy. Major assemblies are covered by the Hewlett-Packard Board Exchange Program to minimise cost-of-ownership.

Troubleshooting

The Troubleshooting in this section aims firstly to isolate the fault to module level and then locate the faulty board assembly within the module. The instrument's built-in Self-tests and detailed "G Sheet" procedures are used to help with this.

When the faulty board has been located, an Exchange or replacement assembly can be ordered using the information in the Replaceable Parts Section of this manual. Detailed dismantling and replacement procedures are included to help with board replacement.

Built-in Service Features

The following Service features are built-in to the HP 37717C:

- Power-on Checks
- Self-Test
- Calibration Routines
- Module Debug Page and Debug Function Page
- Test and Probe Points
- Extender Cards

Power -on Checks

These are run automatically when the unit is switched on. They perform checks on the Control Processor, Memory and Peripherals. Failure will cause a Fatal Error Code to be displayed. This can be read from the display or the Front Panel Leds. A listing of the Fatal Error codes is given in Service Sheet G5.

Self-Test

This consists of individual tests which are used during troubleshooting to verify the functionality of each section of the instrument. These are:

- CPU Tests
- PDH Tests (where this option is fitted)
- SDH Tests (where this option is fitted)
- Optical Interface Tests (where this option is fitted)
- Jitter Tests (where this option is fitted)
- ATM Tests (where this option is fitted)

When troubleshooting, General Service Sheet G1 will indicate when to run Self-test and the action to be taken on failure. External cabling and loopback connectors are required to run these tests. Service Sheet G2 provides all required self-test setup information.

Calibration Routines

These should be used when calibrating the HP 37717C. They are automatic or semi-automatic and are called up when required in the Performance Tests and Adjustment Procedures.

Module Debug Page

This page provides some selecTable setups which are called up during Performance Tests and Adjustments. The Module Debug Page cannot be accessed during normal operation and should never be used without valid procedures.

CAUTION Instrument damage can result if parameters are modified incorrectly in the Module Debug Page. Never use this page without valid procedures.

Debug Function Page

This page allows the user to read and write data directly in instrument registers. It is called up during the Adjustments procedures to switch off the Jitter Transmitter output and may also be used during troubleshooting to set up special conditions on individual modules. The Debug Function Page cannot be accessed during normal operation and should never be used without valid procedures.

CAUTION Instrument damage can result if parameters are modified incorrectly in the Debug Function Page. Never use this page without valid procedures.

Test and Probe Points

These are provided on Board Assemblies within each Module to allow for monitoring on an Oscilloscope or Counter. They are used in Adjustment and Troubleshooting procedures. Care should be taken when using Probe Points, as these do not provide for the probe to be hooked-on.

Extender Cards

- Module Board Extender Card (part number HP 37714-60099)

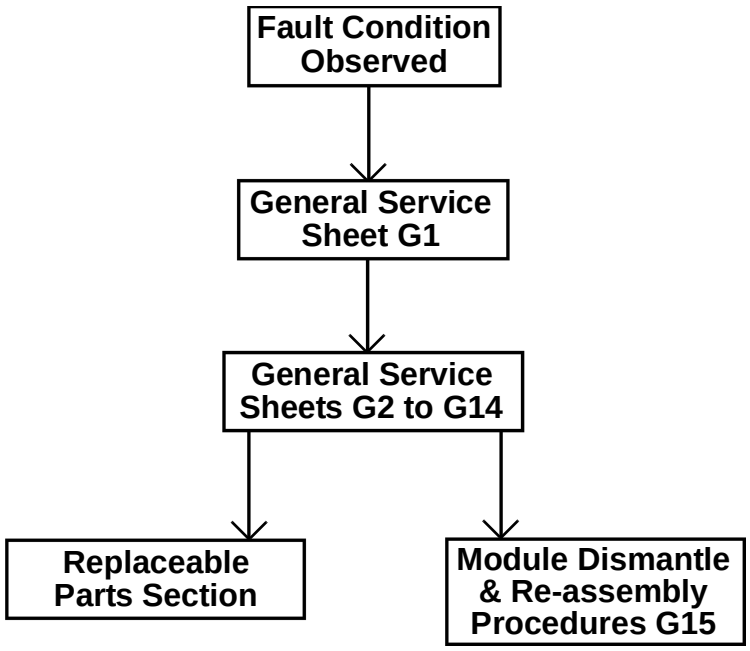
The **Module Board Extender Card** is required during Adjustment and Troubleshooting procedures to allow access to Test and Probe Points. To use this card, remove the required Module (see NOTE below), fit the Extender Card into the correct slot in the Mainframe, then plug the Assembly onto the Extender Card. If the module contains two plug-in board assemblies, another Module Board Extender card may be required to keep the second assembly operating.

NOTE When removing the Module to use the Module Board Extender Card, you MUST follow the correct Module Removal and Replacement procedure.

General Service Sheet G1 - Troubleshooting Entry

Introduction

Troubleshooting information for the HP 37717C is contained in Service Sheets G1 to G15. All troubleshooting starts from Page 5-8 Troubleshooting Entry Chart. By following this chart, the detailed information contained in G2 to G15 can be quickly accessed.



Troubleshooting Preliminaries

1. Ensure no obvious damage to the instrument and that all Modules are fitted in the correct slots. Check to ensure Modules are pushed fully home in the Mainframe.
2. Check the line fuse has the correct rating and is not blown.
3. Check the Service Note listing for anything which may relate to the fault you are troubleshooting.
4. If possible, access the Product Support Line. This contains helpful and up-to-date information on all aspects of supporting the HP 37717C (including the latest Service Note index) and is available to Hewlett-Packard employees. The website address for this is "http://hpweb.sqf.hp.com/qto/support/supplayo.htm"

   Non Hewlett-Packard personnel may obtain information from Product Support by contacting the nearest Hewlett-Packard Service Center.

Troubleshooting Setup

1. Ensure the Line supply is within the required voltage and frequency range (see Instrument specifications) and connect to the unit using a suiTable cable.
2. Refer to General Service Sheet G2 (Self tests) and connect the required external cables and loopback connectors to each module in the instrument.
3. Switch on the instrument and follow the instructions in the following Flow-chart.

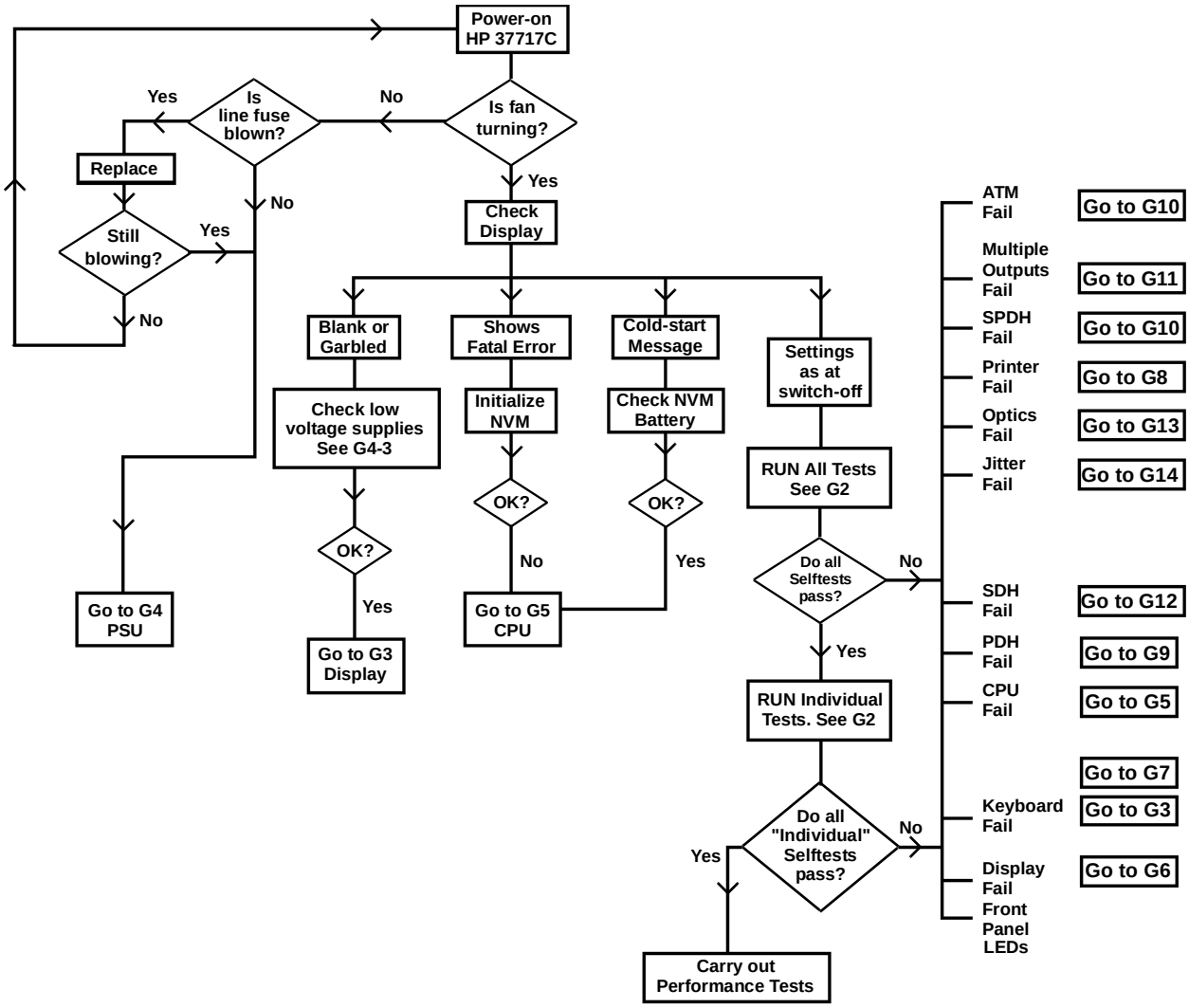


Figure 5-2 Troubleshooting Entry Chart

General Service Sheet G2 - Self Test

Introduction

Self Test consists of individual tests which are used during troubleshooting to verify each main functional block in the instrument.

Self Test is called up as part of the Main Troubleshooting Entry chart in Service Sheet G1.

This Service Sheet contains information on how to set up the instrument to run the Self Test and how to interpret Self Test results.

Description

A selftest exists for each module in the instrument. Each test is listed in the Table below.

Test No	Description	Options (See note below)	Number of Tests	Fail Codes
1	CPU (Processor)	All	16	10 to 166
2	PDH tests	UKK, [USB]	36	2010 to 2365
	Binary Interface Tests	UH3	13	2370 to 2494
3	SPDH tests	UKJ, [USA], USN	72	3010 to 3724
	SPDH tests	110	60	3830 to 3996, 18006 to 18454
	Binary Interface Tests	UH3	10	3730 to 3824
7	SDH tests	A1T, [A1U], A3R	160	711 to 791, 7101 to 7991, 2201 to 22604
8	SDH tests	US1, [US5]	96	821 to 894, 8104 to 8964
9	Optical tests	UH1/2, URU	43	911 to 951, 9101 to 9433
10	Optical (USN) tests	UKT, [USN], 130, 131	99	1011 to 1095, 10011 to 10996
11	ATM Tests (UKZ)	UKZ	99	11010 to 11998
12	ATM Tests	UKN	99	12016 to 12998
13	Service Tests		23	13002 to 13214
14	Jitter tests	UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	87	1411 to 1499, 14111 to 14948
15	ATM tests	UKN, [USE]	99	15016 to 15999

Full testing should give greater than 90% confidence that the module is operational and meeting it's published specifications.

Each test may be selected and run individually or all tests may be selected and run together by selecting "All Tests" from the menu. In some cases, it may be required to select and run a test both individually and as part of the "All Tests" suite to fully test a particular module.

Modules which fall into this category are as follows:

Dual wavelength Optics Module (Option USN)

The 1550 nm wavelength is NOT tested as part of the "All Tests" suite. This must be setup and run individually (see below).

Optical Line Jitter Module (Options A1N, A1P, [A1R] or [A1S])

This is NOT tested as part of the "All Tests" suite. Optical Line Jitter tests require separate connections, so must be run individually (see below).

SDH Pointer Sequence and Overhead Module (Option A1T [A1U)

The RS449 interface fitted to this option is NOT tested as part of the "All Tests" suite. This is tested as part of the individual A1T test (see below) and requires a special Interface Connector.

Loopbacks Required when Running "All Tests"

Loop the following I/O ports when running **"All Tests":**

On PDH Module (Options UKK, UKJ, [UKN], [110]), Loop 75Ω Signal Out to 75Ω Signal In.

On PDH Module (Options UKK, UKJ, [UKN], [110]), loop 120Ω Signal Out to 120Ω Signal In.

On PDH Module (Option UKJ, [110]), loop Mux to Demux.

On SDH Module (Option US1 [US5], A1T, [A1U]), loop 75Ω STM1 E Out to 75Ω STM1 E In.

On Optical Module loop Laser Out to Laser In.

Running "All Tests"

1. Press the OTHER key and the MORE softkey until the SELF TEST softkey is displayed at bottom of the display.
2. Press the SELF TEST softkey.
3. Move the cursor to TEST TYPE field using the ↑ keys and select TEST TYPE [ALL TESTS].
4. Press the RUN/STOP key to start the tests-the RUN/STOP LED **will not be lit**, but the display will indicate RUNNING.
5. The tests will take between 20 minutes and 1 hour to complete (depending on options fitted). If any failure occurs a FAIL NUMBER will be displayed. A list and explanation of these fail numbers is given at the end of this section. For detailed information on each selftest failure number refer to the Troubleshooting Section in this Manual.
6. When the tests have completed successfully, the display will show **ALL TESTS PASSED**.

Loopbacks Required when running Individual Tests

Loop the following I/O ports when running any individual selftest:

NOTE You need only loop ports on options (modules) which are being tested.

CPU TESTS selected:

Fit the special RS232 looping link or make the connections shown below:

Also, fit a formatted 3.5 inch Disk into the Disk-drive slot at the side of this processor module.

Refer to the Operating Manual for information on formatting disks.

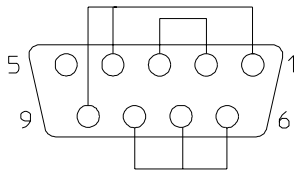


Figure 5-3 Disk-Drive CPU Module RS232 Port Selftest Loopback Connections

PDH TESTS selected:

On PDH Module (Options UKK, UKJ, [UKN], [110]), loop 75Ω Signal Out to 75Ω Signal In.

On PDH Module (Options UKK, UKJ, [UKN], [110]), loop 120Ω Signal Out to 120Ω Signal In.

On PDH Module (Option UKJ, [110]), loop Mux to Demux.

SDH TESTS selected:

On SDH Module, loop 75Ω STM1 E Out to 75Ω STM1 E In.

On SDH Module, fit Special RS449 Looping Connector or make the connections shown below:

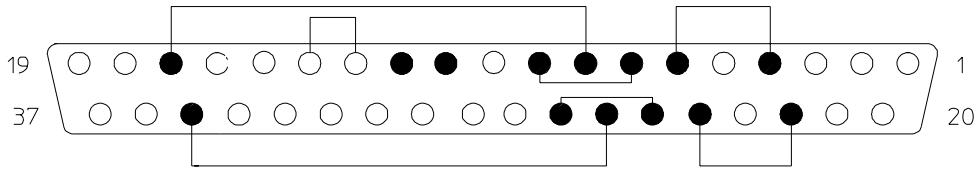


Figure 5-4 SDH Module RS449 Port Selftest Loopback Connections

OPTICAL TESTS selected:

On Optical Module (Options UH1, UH2, UKT), loop Laser Out to Laser In.

On Optical Module (Options URU, USN), Laser Out to Laser In (1550 nm) via 10 dB Optical Attenuator.

CAUTION Failure to attenuate the Optical Signal from Option URU or USN could result in damage to the Optical Receiver.

NOTE Failure to attenuate the Optical Signal from Option URU or USN will result in selftest failure.

JITTER TESTS selected:

NOTE You must have a Jitter Transmitter Module fitted to run the jitter selftest.

If PDH JITTER ONLY fitted (Options UHN, [US9])

On PDH Module, loop 75Ω Signal Out to 75Ω Signal In.

If PDH and SDH ELECTRICAL JITTER fitted (Options A1M, [A1Q])

On PDH Module, loop 75Ω Signal Out to 75Ω Signal In.

Also loop 75Ω STM1 E Out On the SDH Module to 75Ω STM1 E Jitter In on the Jitter Receive Module.

If PDH and SDH ELECTRICAL and SDH OPTICAL JITTER fitted (Options A1N, A1P [A1R], [A1S])

On the PDH Module, loop 75 Ω Signal Out to 75 Ω Signal In.

Also loop 75 Ω STM1 E Out On the SDH Module to 75 Ω STM1 E Jitter In on the Jitter Receive Module.

Also loop the Laser Out Port on the Optical Module to Laser In on the Jitter Receive Module **via 10 dB Optical Attenuator if the optical module is Option URU**. Use the 1310 nm Optical Out Port if the Optical module is Option USN.

CAUTION Failure to attenuate the Optical Signal from Option URU could result in damage to the Jitter Receiver Module.

NOTE Failure to attenuate the Optical Signal from Option URU may result in selftest failure.

Running Individual Tests

1. Press [OTHER] key the **MORE** softkey until **SELF TEST** softkey is displayed at bottom of the display.
2. Press **SELF TEST** softkey.
3. Move the cursor to TEST TYPE field using the [⇧] keys and set the TEST TYPE to the individual test you want to run.
4. Press the [RUN/STOP] key to start the test-the RUN/STOP LED **will not be lit**, but the display will indicate RUNNING.
5. The test time will depend on the option being tested. If any failure occurs a FAIL NUMBER will be displayed. A list and explanation of these fail numbers is given at the end of this section. For detailed information on each selftest failure number refer to the troubleshooting Section in this Manual.
6. When the selected test has completed successfully, the display will show **PASSED.** You can then select and run the next individual test of your choice or exit the selftest screen.

Selftest Notes

1. The user can select each test individually or run them all as a suite.
2. If you want to stop the selftest after it has commenced running, you will need to cycle power on the instrument.
3. Test failure will produce an error code number (and sometimes a message). The Error code number will usually be in the format XXYYZZ (Except for the CPU Tests) where XX is the Test Number, YY is the Subtest Number and ZZ is a number associated with a particular fail condition.
4. A test failure will normally point to a fault on a specific module in the instrument and can often point directly to the faulty board assembly.
5. When a selftest fails, the instrument will be frozen with the fail conditions still set up i.e. all transmitter and receiver parameters will be set up as in the failure mode. This allows easier troubleshooting of the fail condition and is used as the basis for many of the General Service Sheet Troubleshooting procedures.
6. An individual Selftest can be cycled continuously to help isolate an intermittent or occasional failure.

The troubleshooting in General Service Sheet G1 of the Service Manual will indicate the action to be taken on any selftest failure.

Diagnostic Tests

These routines test the operation of the Colour Display, Front Panel LEDS and keyboard as well as providing more detailed CPU and Remote Interface Tests. They will normally be run after the main selftests or if a fault on any of these functional blocks is indicated. The troubleshooting in General Service Sheet G1 will indicate the action to be taken on failure of any Diagnostic test.

Running Repeat Self Test

1. Display the Other Test Features Page by simultaneously pressing [SINGLE] and the 4th softkey from the left below the display.
2. Select Repeat Self Test by moving the cursor to [NORMAL] and changing to [REPEAT].
3. Select the test you want to run and it will cycle automatically.

To abort the tests, you will need to switch the instrument off. When switched on again, the Repeat Selftest will be disabled (i.e. returned to [NORMAL] mode).

Running Front Panel LEDS Diagnostic Test

1. Display the Other Test Features Page by simultaneously pressing [SINGLE] and the 4th softkey from the left below the Front Panel display.
2. To start testing, select LED TEST. The test will automatically light each LED in sequence, so the operator must look for an unlit LED during this sequence.
3. To stop the test, press ABORT TEST softkey. The test will stop at the end of the current sequence and the display will return to the Other Test Features page.
4. Press EXIT softkey to return to normal operation.

Running the Keyboard Diagnostic Test

1. Display the Keyboard Test Page by simultaneously pressing [SINGLE] and the 3rd softkey from the left below the Front Panel display.
2. Press each front panel key once to check operation. When the key is pressed, the display will show the key function in the Last Key Pressed field, so the operator must look for an incorrect description in this field.
3. To stop the test, press the same key twice. The instrument will return to normal operation.

Running the Display Diagnostic Test

1. Start the Display Diagnostic Test by simultaneously pressing [SINGLE] and the 2nd softkey from the left below the Front Panel display.
2. The test will automatically set up different Test Cards on the display. These are designed to show any problems with brightness, contrast and character definition on the display, so the operator must look for any obvious problems in these areas. The Display test sequence is as follows:
   The display is completely white.
   The display is completely red.
   The display is completely green.
   The display is completely blue.
   The display is swept from top to bottom until covered by a black and yellow matrix.
   The display shows a group of large alpha-numeric characters
   The display shows a group of smaller alpha-numeric characters and a square test pattern on the right-side.
3. On the final part of this test sequence, the message DISPLAY TEST ENDS will be shown at the bottom of the display and the instrument will return to normal operation.

Running the Processor Diagnostic Test

1. Display the Processor Board Test Page by simultaneously pressing [SINGLE] and the 5th softkey from the left below the Front Panel display.
2. Each of the elements below will be tested automatically and a Pass or Fail message and Error Code displayed at the end. Use the information in Service Sheet G5 to troubleshoot any of these fail codes.
3. To stop the test at any time, press ABORT TEST softkey. The test will stop at the end of the current sequence and the instrument will return to normal operation.
4. When the test ends, press the CONTINUE softkey and the instrument will return to normal operation.

Self Test Fail Numbers

The following list of self test failure codes may be used as a Quick Reference Guide to indicate the area of a failure on the HP 37717C.

When self test is run fail numbers may be displayed. The fail numbers and a description are listed in the following pages in numerical order.

No.	Description
10 to 166	CPU (Processor) all instruments

SDH Tests A1T, [A1U], A3R	
No.	**Description**
711	STM-1 Signal Loss
721	STM-1 Pattern Sync Loss
724	STM-1 Bit Errors
741	STM-1 Signal Loss
751	STM-1 Signal Loss
753	STM-1 No offset - Frequency low
754	STM-1 No offset - Frequency high
761	STM-1 Signal Loss
763	STM-1 +100 ppm - Offset low
764	STM-1 +100 ppm - Offset high
771	STM-1 Signal Loss
773	STM-1 -100 ppm - Offset low
774	STM-1 -100 ppm - Offset high
781	STM-1 Clock Loss
791	STM-1 Ref Clk div ratio = 193 but NO Clock Loss

SDH Tests US1, [US5]	
No.	**Description**
821	STM-1 Signal Loss
831	STM-1 Pattern Sync Loss
834	STM-1 Bit Errors
841	STM-1 Signal Loss
843	STM-1 No offset - Frequency low
844	STM-1 No offset - Frequency high

SDH Tests US1, [US5]	
No.	**Description**
851	STM-1 Signal Loss
853	STM-1 +100 ppm - Offset low
854	STM-1 +100 ppm - Offset high
861	STM-1 Signal Loss
863	STM-1 -100 ppm - Offset low
864	STM-1 -100 ppm - Offset high
871	STM-1 Frame or Pointer Sync Loss
884	STM-1 B1 BIP Errors
894	STM-1 B2 BIP Errors

Optical Tests UH1/2, URU	
No.	**Description**
911	STM-1 Optical Signal Loss
921	STM-1 Optical alarms present
931	STM-1 Optical Pattern Sync Loss
934	STM-1 Optical Bit Errors
941	STM-1 Optical Pattern Sync Loss
943	STM-1 Optical Bit Error Rate low
944	STM-1 Optical Bit Error Rate high
951	STM-1 Optical No Signal Loss

Optical (USN) Tests UKT, [USN]	
No.	**Description**
1010	FEPROM sum-check error
1020	SRAM error
1021	SRAM error
1022	SRAM error
1023	SRAM error
1024	SRAM address error
1040	RS232 DCD stuck low or high
1041	RS232 RI stuck low or high
1042	RS232 DSR stuck low or high

Optical (USN) Tests UKT, [USN]	
No.	**Description**
1043	RS232 CTS stuck low or high
1044	RS232 Rx too many bytes
1045	RS232 Tx time out
1046	RS232 Rx too few bytes
1047	RS232 Tx/Rx data failure
1052	HPIB driver chip fails
1060	RTC set incorrectly
1061	RTC not ticking correctly
1070	Parallel Port failed to send data
1080	Internal printer fails
1081	Keybd proc internal RAM fails
1082	Keybd proc external RAM fails
1083	Keybd proc ROM fails
1084	Front panel no response
1085	Front panel command not ok
1086	Front panel returned an invalid error number
1087	Front panel cpu or UART error
1088	Cannot detect front panel printer
1090	VRAM data error

CPU All Options	
No.	**Description**
1100	DISK : no disk in drive
1101	DISK : disk is full
1102	DISK : disk write failure
1103	DISK : disk read failure
1104	DISK : disk verify read/write failure
1110	LAN failed 'power on' test
1111	LAN test returned an invalid error number
1112	No LAN hardware found
1113	LAN fitted, no test result available
1120	Front panel no response
1121	Front panel command not ok
1122	Front panel returned an invalid error number

CPU All Options	
No.	**Description**
1123	Dual Port SRAM data error
1124	Dual Port SRAM address error
1130	Front panel no response
1131	Front panel command not ok
1132	Front panel returned an invalid error number
1133	Front panel FEPROM sum-check error
1140	Front panel no response
1141	Front panel command not ok
1142	Front panel returned an invalid error number
1143	Front panel SRAM data error
1144	Front panel SRAM address error
1145	Front panel : requested address range not valid
1150	Front panel no response
1151	Front panel command not ok
1152	Front panel returned an invalid error number
1153	Front panel VRAM data error
1154	Front panel stored fonts are corrupted
1155	Front panel requested address range not valid
1156	Front panel VGA controller error
1160	Front panel no response
1161	Front panel command not ok
1162	Front panel returned an invalid error number
1163	Front panel UART Tx/Rx error (internal loop-back)
1164	Front panel failed to reset internal loop-back
1165	Front panel : operator indicated lid-printer power failure
1166	Front panel UART Tx/Rx error (external loop-back)

Jitter Tests UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	
No.	**Description**
1411	JITTER GEN 140 Mb/s PRBS23 10 UI 2 kHz - PDH errors
1419	JITTER GEN 140 Mb/s - VCO not settled
1421	JITTER GEN 140 Mb/s PRBS23 10 UI 5 kHz - PDH errors
1431	JITTER GEN 34 Mb/s PRBS23 10 UI 2 kHz - PDH errors
1439	JITTER GEN 34 Mb/s - VCO not settled
1441	JITTER GEN 34 Mb/s PRBS23 10 UI 5 kHz - PDH errors
1452	JITTER GEN 34 Mb/s PRBS23 10 UI 100 kHz - no PDH errors
1461	JITTER GEN 8 Mb/s PRBS23 10 UI 2 kHz - PDH errors
1469	JITTER GEN 8 Mb/s - VCO not settled
1471	JITTER GEN 8 Mb/s PRBS23 10 UI 5 kHz - PDH errors
1482	JITTER GEN 8 Mb/s PRBS23 10 UI 50 kHz - no PDH errors
1491	JITTER GEN 2 Mb/s PRBS23 10 UI 2 kHz - PDH errors
1499	JITTER GEN 2 Mb/s - VCO not settled

PDH Tests UKK, [USB]	
No.	**Description**
2010	UPDH (Unbalanced) Signal Loss
2011	UPDH 139 Mb/s PRBS(23) Pattern loss
2014	UPDH 139 Mb/s PRBS(23) Errors present
2020	UPDH (Unbalanced) Signal Loss
2021	UPDH 34 Mb/s PRBS(23) Pattern loss
2024	UPDH 34 Mb/s PRBS(23) Errors present
2030	UPDH (Unbalanced) Signal Loss
2031	UPDH 8 Mb/s PRBS(15) Pattern loss
2034	UPDH 8 Mb/s PRBS(15) Errors present
2040	UPDH (Unbalanced) Signal Loss
2041	UPDH 2 Mb/s PRBS(15) HDB3 Pattern loss
2044	UPDH 2 Mb/s PRBS(15) HBD3 Errors present
2050	UPDH (Unbalanced) Signal Loss
2051	UPDH 2 Mb/s PRBS(15) AMI Pattern loss
2054	UPDH 2 Mb/s PRBS(15) AMI Errors present
2060	UPDH (Unbalanced) Signal Loss
2061	UPDH 704 kb/s PRBS(15) HDB3 Pattern loss

PDH Tests UKK, [USB]	
No.	**Description**
2064	UPDH 704 kb/s PRBS(15) HBD3 Errors present
2070	UPDH (Unbalanced) Signal Loss
2071	UPDH 704 kb/s PRBS(15) AMI Pattern loss
2074	UPDH 704 kb/s PRBS(15) AMI Errors present
2080	UPDH (Unbalanced) Signal Loss
2081	UPDH 139 Mb/s WORD_2 Pattern loss
2084	UPDH 139 Mb/s WORD_2 Errors present
2090	UPDH (Unbalanced) Signal Loss
2091	UPDH 139 Mb/s WORD_1 Pattern loss
2094	UPDH 139 Mb/s WORD_1 Errors present
2100	UPDH (Unbalanced) Signal Loss
2101	UPDH 704 kb/s WORD_2 AMI Pattern loss
2104	UPDH 704 kb/s WORD_2 AMI Errors present
2110	UPDH (Balanced) Signal Loss
2111	UPDH 2 Mb/s PRBS(15) (Bal) HDB3 Pattern loss
2114	UPDH 2 Mb/s PRBS(15) (Bal) HBD3 Errors present
2120	UPDH (Balanced) Signal Loss
2121	UPDH 704 kb/s WORD_2 (Bal) AMI Pattern loss
2124	UPDH 704 kb/s WORD_2 (Bal) AMI Errors present
2130	UPDH (Unbalanced) Signal Loss
2133	UPDH 704 kb/s - Offset = 0 ppm Result low
2134	UPDH 704 kb/s - Offset = 0 ppm Result high
2140	UPDH (Unbalanced) Signal Loss
2143	UPDH 2 Mb/s - Offset = 0 ppm Result low
2144	UPDH 2 Mb/s - Offset = 0 ppm Result high
2150	UPDH (Unbalanced) Signal Loss
2153	UPDH 8 Mb/s - Offset = 0 ppm Result low
2154	UPDH 8 Mb/s - Offset = 0 ppm Result high
2160	UPDH (Unbalanced) Signal Loss
2163	UPDH 8 Mb/s - Offset = -100 ppm Result low
2164	UPDH 8 Mb/s - Offset = -100 ppm Result high
2170	UPDH (Unbalanced) Signal Loss
2173	UPDH 8 Mb/s - Offset = +100 ppm Result low
2174	UPDH 8 Mb/s - Offset = +100 ppm Result high
2180	UPDH (Unbalanced) Signal Loss

PDH Tests UKK, [USB]	
No.	**Description**
2183	UPDH 34 Mb/s - Offset = 0 ppm Result low
2184	UPDH 34 Mb/s - Offset = 0 ppm Result high
2190	UPDH (Unbalanced) Signal Loss
2193	UPDH 34 Mb/s - Offset = -100 ppm Result low
2194	UPDH 34 Mb/s - Offset = -100 ppm Result high
2200	UPDH (Unbalanced) Signal Loss
2203	UPDH 34 Mb/s - Offset = +100 ppm Result low
2204	UPDH 34 Mb/s - Offset = +100 ppm Result high
2210	UPDH (Unbalanced) Signal Loss
2213	UPDH 140 Mb/s - Offset = 0 ppm Result low
2214	UPDH 140 Mb/s - Offset = 0 ppm Result high
2220	UPDH (Unbalanced) Signal Loss
2223	UPDH 140 Mb/s - Offset = -100 ppm Result low
2224	UPDH 140 Mb/s - Offset = -100 ppm Result high
2230	UPDH (Unbalanced) Signal Loss
2233	UPDH 140 Mb/s - Offset = +100 ppm Result low
2234	UPDH 140 Mb/s - Offset = +100 ppm Result high
2240	UPDH (Unbalanced) Signal Loss
2243	UPDH 140 Mb/s - Error Add = Off Result low
2244	UPDH 140 Mb/s - Error Add = Off Result high
2250	UPDH (Unbalanced) Signal Loss
2253	UPDH 140 Mb/s - Error Add = Single Result low
2254	UPDH 140 Mb/s - Error Add = Single Result high
2260	UPDH (Unbalanced) Signal Loss
2263	UPDH 140 Mb/s - Error Add = On Result low
2264	UPDH 140 Mb/s - Error Add = On Result high
2273	UPDH 704 kb/s - Clock Recovery Result low
2274	UPDH 704 kb/s - Clock Recovery Result high
2283	UPDH 2 Mb/s - Clock Recovery Result low
2284	UPDH 2 Mb/s - Clock Recovery Result high
2293	UPDH 8 Mb/s - Clock Recovery Result low
2294	UPDH 8 Mb/s - Clock Recovery Result high
2303	UPDH 34 Mb/s - Clock Recovery Result low
2304	UPDH 34 Mb/s - Clock Recovery Result high
2313	UPDH 140 Mb/s - Clock Recovery Result low

PDH Tests UKK, [USB]	
No.	**Description**
2314	UPDH 140 Mb/s - Clock Recovery Result high
2320	UPDH FAS register write error
2330	UPDH FAS - No signal
2335	UPDH FAS - LCA not locked
2340	UPDH FAS 8 Mb/s - No signal
2341	UPDH FAS 8 Mb/s - Not locked (1)
2344	UPDH FAS 8 Mb/s - Errors present
2345	UPDH FAS 8 Mb/s - Not locked (2)
2350	UPDH FAS 34 Mb/s - No signal
2351	UPDH FAS 34 Mb/s - Not locked (1)
2354	UPDH FAS 34 Mb/s - Errors present
2355	UPDH FAS 34 Mb/s - Not locked (2)
2360	UPDH FAS 140 Mb/s - No signal
2361	UPDH FAS 140 Mb/s - Not locked (1)
2364	UPDH FAS 140 Mb/s - Errors present
2365	UPDH FAS 140 Mb/s - Not locked (2)

Binary Interface Tests UH3	
No.	**Description**
2370	UPDH BIN ECL 140 Mb/s Signal Loss
2373	UPDH BIN ECL 140 Mb/s Result low
2374	UPDH BIN ECL 140 Mb/s Result high
2380	UPDH BIN ECL 140 Mb/s Signal Loss
2384	UPDH BIN ECL 140 Mb/s Result high
2390	UPDH BIN TTL 34 Mb/s Signal Loss
2393	UPDH BIN TTL 34 Mb/s Result low
2394	UPDH BIN TTL 34 Mb/s Result high
2400	UPDH BIN TTL 34 Mb/s Signal Loss
2404	UPDH BIN TTL 34 Mb/s Result high
2410	UPDH BIN TTL 8 Mb/s Signal Loss
2413	UPDH BIN TTL 8 Mb/s Result low
2414	UPDH BIN TTL 8 Mb/s Result high
2420	UPDH BIN TTL 8 Mb/s Signal Loss
2424	UPDH BIN TTL 8 Mb/s Result high

Binary Interface Tests UH3	
No.	**Description**
2430	UPDH BIN TTL 2 Mb/s Signal Loss
2433	UPDH BIN TTL 2 Mb/s Result low
2434	UPDH BIN TTL 2 Mb/s Result high
2440	UPDH BIN TTL 2 Mb/s Signal Loss
2444	UPDH BIN TTL 2 Mb/s Result high
2450	UPDH BIN TTL 704 kb/s Signal Loss
2453	UPDH BIN TTL 704 kb/s Result low
2454	UPDH BIN TTL 704 kb/s Result high
2460	UPDH BIN TTL 704 kb/s Signal Loss
2464	UPDH BIN TTL 704 kb/s Result high
2470	UPDH BIN ECL 140 Mb/s Signal Loss
2474	UPDH BIN ECL 140 Mb/s User Pattern Result high
2480	UPDH BIN TTL 704 kb/s User Pattern Signal Loss
2484	UPDH BIN TTL 704 kb/s User Pattern Result high
2490	UPDH BIN TTL 34 Mb/s User Pattern Signal Loss
2494	UPDH BIN TTL 34 Mb/s User Pattern Result high

SPDH Tests UKJ, [USA], UKN	
No.	**Description**
3010	SPDH (Unbalanced) Signal Loss
3011	SPDH 140 Mb/s PRBS(23) Pattern loss
3014	SPDH 140 Mb/s PRBS(23) Errors present
3020	SPDH (Unbalanced) Signal Loss
3021	SPDH 140 Mb/s WORD1 Pattern loss
3024	SPDH 140 Mb/s WORD1 Errors present
3030	SPDH (Unbalanced) Signal Loss
3031	SPDH 140 Mb/s WORD2 Pattern loss
3034	SPDH 140 Mb/s WORD2 Errors present
3040	SPDH (Unbalanced) Signal Loss
3041	SPDH 34 Mb/s PRBS(23) HDB3 Pattern loss
3044	SPDH 34 Mb/s PRBS(23) HBD3 Errors present
3050	SPDH (Unbalanced) Signal Loss
3051	SPDH 8 Mb/s PRBS(15) HDB3 Pattern loss
3054	SPDH 8 Mb/s PRBS(15) HDB3 Errors present

SPDH Tests UKJ, [USA], UKN	
No.	**Description**
3060	SPDH (Unbalanced) Signal Loss
3061	SPDH 2 Mb/S PRBS(15) HDB3 Pattern loss
3064	SPDH 2 Mb/S PRBS(15) HBD3 Errors present
3070	SPDH (Unbalanced) Signal Loss
3071	SPDH 2 Mb/s PRBS(15) AMI Pattern loss
3074	SPDH 2 Mb/s PRBS(15) AMI Errors present
3080	SPDH (Balanced) Signal Loss
3081	SPDH 2 Mb/s PRBS(15) (Bal) HDB3 Pattern loss
3084	SPDH 2 Mb/s PRBS(15) (Bal) HBD3 Errors present
3090	SPDH (Balanced) Signal Loss
3091	SPDH 2 Mb/s PRBS(15) (Bal) AMI Pattern loss
3094	SPDH 2 Mb/s PRBS(15) (Bal) AMI Errors present
3100	SPDH (Unbalanced) Signal Loss
3102	SPDH 140 Mb/s - Offset = 0 ppm VCXO Not Settled
3103	SPDH 140 Mb/s - Offset = 0 ppm Result low
3104	SPDH 140 Mb/s - Offset = 0 ppm Result high
3110	SPDH (Unbalanced) Signal Loss
3112	SPDH 140 Mb/s - Offset = +100 ppm VCXO Not Settled
3113	SPDH 140 Mb/s - Offset = +100 ppm Result low
3114	SPDH 140 Mb/s - Offset = +100 ppm Result high
3120	SPDH (Unbalanced) Signal Loss
3122	SPDH 140 Mb/s - Offset = -100 ppm VCXO Not Settled
3123	SPDH 140 Mb/s - Offset = -100 ppm Result low
3124	SPDH 140 Mb/s - Offset = -100 ppm Result high
3130	SPDH (Unbalanced) Signal Loss
3132	SPDH 34 Mb/s - Offset = 0 ppm VCXO Not Settled
3133	SPDH 34 Mb/s - Offset = 0 ppm Result low
3134	SPDH 34 Mb/s - Offset = 0 ppm Result high
3140	SPDH (Unbalanced) Signal Loss
3142	SPDH 34 Mb/s - Offset = +100 ppm VCXO Not Settled
3143	SPDH 34 Mb/s - Offset = +100 ppm Result low
3144	SPDH 34 Mb/s - Offset = +100 ppm Result high
3150	SPDH (Unbalanced) Signal Loss
3152	SPDH 34 Mb/s - Offset = -100 ppm VCXO Not Settled
3153	SPDH 34 Mb/s - Offset = -100 ppm Result low

SPDH Tests UKJ, [USA], UKN	
No.	**Description**
3154	SPDH 34 Mb/s - Offset = -100 ppm Result high
3160	SPDH (Unbalanced) Signal Loss
3162	SPDH 8 Mb/s - Offset = 0 ppm VCXO Not Settled
3163	SPDH 8 Mb/s - Offset = 0 ppm Result low
3164	SPDH 8 Mb/s - Offset = 0 ppm Result high
3170	SPDH (Unbalanced) Signal Loss
3172	SPDH 8 Mb/s - Offset = +100 ppm VCXO Not Settled
3173	SPDH 8 Mb/s - Offset = +100 ppm Result low
3174	SPDH 8 Mb/s - Offset = +100 ppm Result high
3180	SPDH (Unbalanced) Signal Loss
3182	SPDH 8 Mb/s - Offset = -100 ppm VCXO Not Settled
3183	SPDH 8 Mb/s - Offset = -100 ppm Result low
3184	SPDH 8 Mb/s - Offset = -100 ppm Result high
3190	SPDH (Unbalanced) Signal Loss
3192	SPDH 2 Mb/s - Offset = 0 ppm VCXO Not Settled
3193	SPDH 2 Mb/s - Offset = 0 ppm Result low
3194	SPDH 2 Mb/s - Offset = 0 ppm Result high
3200	SPDH (Unbalanced) Signal Loss
3202	SPDH 2 Mb/s - Offset = +100 ppm VCXO Not Settled
3203	SPDH 2 Mb/s - Offset = +100 ppm Result low
3204	SPDH 2 Mb/s - Offset = +100 ppm Result high
3210	SPDH (Unbalanced) Signal Loss
3212	SPDH 2 Mb/s - Offset = -100 ppm VCXO Not Settled
3213	SPDH 2 Mb/s - Offset = -100 ppm Result low
3214	SPDH 2 Mb/s - Offset = -100 ppm Result high
3223	SPDH 34 Mb/s - CODE error add = OFF Result low
3224	SPDH 34 Mb/s - CODE error add = OFF Result high
3226	SPDH 34 Mb/s - CODE error add = OFF Result Invalid
3233	SPDH 34 Mb/s - CODE error add = SINGLE Result low
3234	SPDH 34 Mb/s - CODE error add = SINGLE Result high
3236	SPDH 34 Mb/s - CODE error add = SINGLE Result Invalid
3243	SPDH 34 Mb/s - CODE error add = 1.0E-3 Result low
3244	SPDH 34 Mb/s - CODE error add = 1.0E-3 Result high
3246	SPDH 34 Mb/s - CODE error add = 1.0E-3 Result Invalid
3253	SPDH 34 Mb/s - FAS error add = OFF Result low

SPDH Tests UKJ, [USA], UKN	
No.	**Description**
3254	SPDH 34 Mb/s - FAS error add = OFF Result high
3256	SPDH 34 Mb/s - FAS error add = OFF Result Invalid
3263	SPDH 34 Mb/s - FAS error add = SINGLE Result low
3264	SPDH 34 Mb/s - FAS error add = SINGLE Result high
3266	SPDH 34 Mb/s - FAS error add = SINGLE Result Invalid
3273	SPDH 34 Mb/s - FAS error add = 1.0E-3 Result low
3274	SPDH 34 Mb/s - FAS error add = 1.0E-3 Result high
3276	SPDH 34 Mb/s - FAS error add = 1.0E-3 Result Invalid
3283	SPDH 34 Mb/s - BIT error add = OFF Result low
3284	SPDH 34 Mb/s - BIT error add = OFF Result high
3286	SPDH 34 Mb/s - BIT error add = OFF Result Invalid
3293	SPDH 34 Mb/s - BIT error add = SINGLE Result low
3294	SPDH 34 Mb/s - BIT error add = SINGLE Result high
3296	SPDH 34 Mb/s - BIT error add = SINGLE Result Invalid
3303	SPDH 34 Mb/s - BIT error add = 1.0E-3 Result low
3304	SPDH 34 Mb/s - BIT error add = 1.0E-3 Result high
3306	SPDH 34 Mb/s - BIT error add = 1.0E-3 Result Invalid
3313	SPDH 2 Mb/s - FAS error add = OFF Result low
3314	SPDH 2 Mb/s - FAS error add = OFF Result high
3316	SPDH 2 Mb/s - FAS error add = OFF Result Invalid
3323	SPDH 2 Mb/s - FAS error add = SINGLE Result low
3324	SPDH 2 Mb/s - FAS error add = SINGLE Result high
3326	SPDH 2 Mb/s - FAS error add = SINGLE Result Invalid
3333	SPDH 2 Mb/s - FAS error add = 1.0E-3 Result low
3334	SPDH 2 Mb/s - FAS error add = 1.0E-3 Result high
3336	SPDH 2 Mb/s - FAS error add = 1.0E-3 Result Invalid
3343	SPDH 2 Mb/s - BIT error add = OFF Result low
3344	SPDH 2 Mb/s - BIT error add = OFF Result high
3346	SPDH 2 Mb/s - BIT error add = OFF Result Invalid
3353	SPDH 2 Mb/s - BIT error add = SINGLE Result low
3354	SPDH 2 Mb/s - BIT error add = SINGLE Result high
3356	SPDH 2 Mb/s - BIT error add = SINGLE Result Invalid
3363	SPDH 2 Mb/s - BIT error add = 1.0E-3 Result low
3364	SPDH 2 Mb/s - BIT error add = 1.0E-3 Result high
3366	SPDH 2 Mb/s - BIT error add = 1.0E-3 Result Invalid

SPDH Tests UKJ, [USA], UKN	
No.	**Description**
3377	SPDH 140 Mb/s Unframed - Loss Of Frame Detected
3386	SPDH 140 Mb/s Framed - Loss Of Frame Not Detected
3387	SPDH 140 Mb/s Framed - Loss Of Frame Detected
3396	SPDH 2 Mb/s Unframed - Loss Of Frame Not Detected
3397	SPDH 2 Mb/s Unframed - Loss Of Frame Detected
3406	SPDH 2 Mb/s PCM30 - Loss Of Frame Not Detected
3407	SPDH 2 Mb/s PCM30 - Loss Of Frame Detected
3408	SPDH 2 Mb/s PCM30 - Loss Of Multiframe Not Detected
3409	SPDH 2 Mb/s PCM30 - Loss Of Multiframe Detected
3416	SPDH 2 Mb/s PCM31 - Loss Of Frame Not Detected
3417	SPDH 2 Mb/s PCM31 - Loss Of Frame Detected
3426	SPDH 2 Mb/s PCM30CRC - Loss Of Frame Not Detected
3427	SPDH 2 Mb/s PCM30CRC - Loss Of Frame Detected
3428	SPDH 2 Mb/s PCM30CRC - Loss Of Multiframe Not Detected
3429	SPDH 2 Mb/s PCM30CRC - Loss Of Multiframe Detected
3436	SPDH 2 Mb/s PCM31CRC - Loss Of Frame Not Detected
3437	SPDH 2 Mb/s PCM31CRC - Loss Of Frame Detected
3446	SPDH 2 Mb/s Drop - Loss Of Frame Not Detected
3447	SPDH 2 Mb/s Drop - Loss Of Frame Detected
3448	SPDH 2 Mb/s Drop - Loss Of Multiframe Not Detected
3449	SPDH 2 Mb/s Drop - Loss Of Multiframe Detected
3451	SPDH 140 Mb/s struct 34 Mb/s - Pattern Loss
3454	SPDH 140 Mb/s struct 34 Mb/s - Pattern Errors Present
3461	SPDH 140 Mb/s struct 8 Mb/s - Pattern Loss
3464	SPDH 140 Mb/s struct 8 Mb/s - Pattern Errors Present
3471	SPDH 140 Mb/s struct 2 Mb/s - Pattern Loss
3474	SPDH 140 Mb/s struct 2 Mb/s - Pattern Errors Present
3481	SPDH 140 Mb/s struct 64 kb/s - Pattern Loss
3484	SPDH 140 Mb/s struct 64 kb/s - Pattern Errors Present
3491	SPDH 140 Mb/s struct Nx64 kb/s (odd channels) - Pattern Loss
3494	SPDH 140 Mb/s struct Nx64 kb/s (odd channels) - Pattern Errors Present
3501	SPDH 140 Mb/s struct Nx64 kb/s (even channels) - Pattern Loss
3504	SPDH 140 Mb/s struct Nx64 kb/s (even channels) - Pattern Errors Present
3511	SPDH 34 Mb/s struct 8 Mb/s - Pattern Loss
3514	SPDH 34 Mb/s struct 8 Mb/s - Pattern Errors Present

SPDH Tests UKJ, [USA], UKN	
No.	**Description**
3521	SPDH 34 Mb/s struct 2 Mb/s - Pattern Loss
3524	SPDH 34 Mb/s struct 2 Mb/s - Pattern Errors Present
3531	SPDH 8 Mb/s struct 2 Mb/s - Pattern Loss
3534	SPDH 8 Mb/s struct 2 Mb/s - Pattern Errors Present
3541	SPDH 140 Mb/s Unframed - PRBS(9) INV Pattern Loss
3544	SPDH 140 Mb/s Unframed - PRBS(9) INV Pattern Errors Present
3551	SPDH 140 Mb/s Unframed - PRBS(11) NON-INV Pattern Loss
3554	SPDH 140 Mb/s Unframed - PRBS(11) NON-INV Pattern Errors Present
3561	SPDH 140 Mb/s Unframed - PRBS(15) INV Pattern Loss
3564	SPDH 140 Mb/s Unframed - PRBS(15) INV Pattern Errors Present
3571	SPDH 140 Mb/s Unframed - PRBS(23) NON-INV Pattern Loss
3574	SPDH 140 Mb/s Unframed - PRBS(23) NON-INV Pattern Errors Present
3581	SPDH 140 Mb/s Unframed - User Word Pattern Loss
3584	SPDH 140 Mb/s Unframed - User Word Pattern Errors Present
3591	SPDH 2 Mb/s Unframed - PRBS(9) NON-INV Pattern Loss
3594	SPDH 2 Mb/s Unframed - PRBS(9) NON-INV Pattern Errors Present
3601	SPDH 2 Mb/s Unframed - PRBS(11) INV Pattern Loss
3604	SPDH 2 Mb/s Unframed - PRBS(11) INV Pattern Errors Present
3611	SPDH 2 Mb/s Unframed - PRBS(15) NON-INV Pattern Loss
3614	SPDH 2 Mb/s Unframed - PRBS(15) NON-INV Pattern Errors Present
3621	SPDH 2 Mb/s Unframed - PRBS(23) INV Pattern Loss
3624	SPDH 2 Mb/s Unframed - PRBS(23) INV Pattern Errors Present
3631	SPDH 2 Mb/s Unframed - User Word Pattern Loss
3634	SPDH 2 Mb/s Unframed - User Word Pattern Errors Present
3641	SPDH 8 Mb/s struct 2 Mb/s insert/drop - Insert Port Not Settled
3644	SPDH 8 Mb/s struct 2 Mb/s insert/drop - Drop Port Not Settled
3651	SPDH 140 Mb/s struct 64 kb/s delay = 0s - Result Invalid
3652	SPDH 140 Mb/s struct 64 kb/s delay = 0s - Timeout
3653	SPDH 140 Mb/s struct 64 kb/s delay = 0s - Result low
3654	SPDH 140 Mb/s struct 64 kb/s delay = 0s - Result high
3661	SPDH 140 Mb/s struct 64 kb/s delay = 2s - Result Invalid
3662	SPDH 140 Mb/s struct 64 kb/s delay = 2s - Timeout
3663	SPDH 140 Mb/s struct 64 kb/s delay = 2s - Result low
3664	SPDH 140 Mb/s struct 64 kb/s delay = 2s - Result high
3671	SPDH 34 Mb/s struct 64 kb/s delay = 0s - Result Invalid

SPDH Tests UKJ, [USA], UKN	
No.	**Description**
3672	SPDH 34 Mb/s struct 64 kb/s delay = 0s - Timeout
3673	SPDH 34 Mb/s struct 64 kb/s delay = 0s - Result low
3674	SPDH 34 Mb/s struct 64 kb/s delay = 0s - Result high
3681	SPDH 34 Mb/s struct 64 kb/s delay = 2s - Result Invalid
3682	SPDH 34 Mb/s struct 64 kb/s delay = 2s - Timeout
3683	SPDH 34 Mb/s struct 64 kb/s delay = 2s - Result low
3684	SPDH 34 Mb/s struct 64 kb/s delay = 2s - Result high
3691	SPDH 8 Mb/s struct 64 kb/s delay = 0s - Result Invalid
3692	SPDH 8 Mb/s struct 64 kb/s delay = 0s - Timeout
3693	SPDH 8 Mb/s struct 64 kb/s delay = 0s - Result low
3694	SPDH 8 Mb/s struct 64 kb/s delay = 0s - Result high
3701	SPDH 8 Mb/s struct 64 kb/s delay = 2s - Result Invalid
3702	SPDH 8 Mb/s struct 64 kb/s delay = 2s - Timeout
3703	SPDH 8 Mb/s struct 64 kb/s delay = 2s - Result low
3704	SPDH 8 Mb/s struct 64 kb/s delay = 2s - Result high
3711	SPDH 2 Mb/s struct 64 kb/s delay = 0s - Result Invalid
3712	SPDH 2 Mb/s struct 64 kb/s delay = 0s - Timeout
3713	SPDH 2 Mb/s struct 64 kb/s delay = 0s - Result low
3714	SPDH 2 Mb/s struct 64 kb/s delay = 0s - Result high
3721	SPDH 2 Mb/s struct 64 kb/s delay = 2s - Result Invalid
3722	SPDH 2 Mb/s struct 64 kb/s delay = 2s - Timeout
3723	SPDH 2 Mb/s struct 64 kb/s delay = 2s - Result low
3724	SPDH 2 Mb/s struct 64 kb/s delay = 2s - Result high

Binary Interface Tests UH3	
No.	**Description**
3730	SPDH BIN ECL 140 Mb/s Signal Loss
3731	SPDH BIN ECL 140 Mb/s Pattern Loss
3733	SPDH BIN ECL 140 Mb/s Result low
3734	SPDH BIN ECL 140 Mb/s Result high
3740	SPDH BIN ECL 140 Mb/s Signal Loss
3741	SPDH BIN ECL 140 Mb/s Pattern Loss
3744	SPDH BIN ECL 140 Mb/s Result high
3750	SPDH BIN TTL 34 Mb/s Signal Loss

Binary Interface Tests UH3	
No.	**Description**
3751	SPDH BIN TTL 34 Mb/s Pattern Loss
3753	SPDH BIN TTL 34 Mb/s Result low
3754	SPDH BIN TTL 34 Mb/s Result high
3760	SPDH BIN TTL 34 Mb/s Signal Loss
3761	SPDH BIN TTL 34 Mb/s Pattern Loss
3764	SPDH BIN TTL 34 Mb/s Result high
3770	SPDH BIN TTL 8 Mb/s Signal Loss
3771	SPDH BIN TTL 8 Mb/s Pattern Loss
3773	SPDH BIN TTL 8 Mb/s Result low
3774	SPDH BIN TTL 8 Mb/s Result high
3780	SPDH BIN TTL 8 Mb/s Signal Loss
3781	SPDH BIN TTL 8 Mb/s Pattern Loss
3784	SPDH BIN TTL 8 Mb/s Result high
3790	SPDH BIN TTL 2 Mb/s Signal Loss
3791	SPDH BIN TTL 2 Mb/s Pattern Loss
3793	SPDH BIN TTL 2 Mb/s Result low
3794	SPDH BIN TTL 2 Mb/s Result high
3800	SPDH BIN TTL 2 Mb/s Signal Loss
3801	SPDH BIN TTL 2 Mb/s Pattern Loss
3804	SPDH BIN TTL 2 Mb/s Result high
3810	SPDH BIN ECL 140 Mb/s Signal Loss
3811	SPDH BIN ECL 140 Mb/s Pattern Loss
3814	SPDH BIN ECL 140 Mb/s User Pattern Result high
3820	SPDH BIN TTL 34 Mb/s User Pattern Signal Loss
3821	SPDH BIN TTL 34 Mb/s User Pattern Pattern Loss
3824	SPDH BIN TTL 34 Mb/s User Pattern Result high
3830	SPDH (Unbalanced) Signal Loss
3831	SPDH DS3 PRBS(23) Pattern Loss
3834	SPDH DS3 PRBS(23) Errors present
3840	SPDH (Unbalanced) Signal Loss
3841	SPDH DS3 WORD1 Pattern Loss
3844	SPDH DS3 WORD1 Errors present
3850	SPDH (Unbalanced) Signal Loss
3851	SPDH DS3 WORD2 Pattern Loss
3854	SPDH DS3 WORD2 Errors present

Binary Interface Tests UH3	
No.	**Description**
3860	SPDH (Unbalanced) Signal Loss
3861	SPDH DS1 PRBS(20) Pattern Loss
3864	SPDH DS1 PRBS(20) Errors present
3870	SPDH (Balanced) Signal Loss
3871	SPDH DS1 PRBS(15) (Bal) B8ZS Pattern Loss
3874	SPDH DS1 PRBS(15) (Bal) B8ZS Errors Present
3880	SPDH (Balanced) Signal Loss
3881	SPDH DS1 QRSS (Bal) AMI Pattern Loss
3884	SPDH DS1 QRSS (Bal) AMI Errors Present
3890	SPDH (Unbalanced) Signal Loss
3891	SPDH DS3 - Offset = 0 ppm VCXO Not Settled
3893	SPDH DS3 - Offset = 0 ppm Result low
3894	SPDH DS3 - Offset = 0 ppm Result high
3900	SPDH (Unbalanced) Signal Loss
3901	SPDH DS3 - Offset = +100 ppm VCXO Not Settled
3903	SPDH DS3 - Offset = +100 ppm Result low
3904	SPDH DS3 - Offset = +100 ppm Result high
3910	SPDH (Unbalanced) Signal Loss
3911	SPDH DS3 - Offset = -100 ppm VCXO Not Settled
3913	SPDH DS3 - Offset = -100 ppm Result low
3914	SPDH DS3 - Offset = -100 ppm Result high
3920	SPDH (Unbalanced) Signal Loss
3921	SPDH DS1 - Offset = 0 ppm VCXO Not Settled
3923	SPDH DS1 - Offset = 0 ppm Result low
3924	SPDH DS1 - Offset = 0 ppm Result high
3930	SPDH (Unbalanced) Signal Loss
3931	SPDH DS1 - Offset = +100 ppm VCXO Not Settled
3933	SPDH DS1 - Offset = +100 ppm Result low
3934	SPDH DS1 - Offset = +100 ppm Result high
3940	SPDH (Unbalanced) Signal Loss
3941	SPDH DS1 - Offset = -100 ppm VCXO Not Settled
3943	SPDH DS1 - Offset = -100 ppm Result low
3944	SPDH DS1 - Offset = -100 ppm Result high
3953	SPDH DS3 - CODE error add = OFF Result low
3954	SPDH DS3 - CODE error add = OFF Result high

Binary Interface Tests UH3	
No.	**Description**
3956	SPDH DS3 - CODE error add = OFF Result Invalid
3963	SPDH DS3 - CODE error add = SINGLE Result low
3964	SPDH DS3 - CODE error add = SINGLE Result high
3966	SPDH DS3 - CODE error add = SINGLE Result Invalid
3973	SPDH DS3 - CODE error add = 1.0E-3 Result low
3974	SPDH DS3 - CODE error add = 1.0E-3 Result high
3976	SPDH DS3 - CODE error add = 1.0E-3 Result Invalid
3983	SPDH DS3 - FAS error add = OFF Result low
3984	SPDH DS3 - FAS error add = OFF Result high
3986	SPDH DS3 - FAS error add = OFF Result Invalid
3993	SPDH DS3 - FAS error add = SINGLE Result low
3994	SPDH DS3 - FAS error add = SINGLE Result high
3996	SPDH DS3 - FAS error add = SINGLE Result Invalid

SDH Tests A1T, [A1U], A3R	
No.	**Description**
7101	ODL not running
7102	STM-1 POH Test Failed
7104	STM-1 SOH Test Failed
7111	STM-1 VC-4 POH message failure
7121	STM-1 Frame or Pointer Sync Loss
7123	STM-1 B1 BIP Errors low
7124	STM-1 B1 BIP Errors high
7131	STM-1 Frame or Pointer Sync Loss
7133	STM-1 B2 BIP Errors low
7134	STM-1 B2 BIP Errors high
7141	STM-1 Frame or Pointer Sync Loss
7143	STM-1 B3 BIP Errors low
7144	STM-1 B3 BIP Errors high
7151	STM-1 Frame or Pointer Sync Loss
7153	STM-1 (M1) MS-REI Errors low
7154	STM-1 (M1) MS-REI Errors high
7161	STM-1 Frame or Pointer Sync Loss
7163	STM-1 (Z5) AU-4 HP-IEC Errors low

SDH Tests A1T, [A1U], A3R	
No.	**Description**
7164	STM-1 (Z5) AU-4 HP-IEC Errors high
7171	STM-1 Frame A1A2 errors OFF, LOF
7172	STM-1 Frame A1A2 1 in 4 errors, LOF
7173	STM-1 Frame A1A2 2 in 4 errors, LOF
7174	STM-1 Frame A1A2 3 in 4 errors, LOF
7175	STM-1 Frame A1A2 4 in 4 errors, NO LOF
7176	STM-1 Frame A1A2 3 in 4 errors, NO LOF
7177	STM-1 Frame A1A2 2 in 4 errors, LOF
7178	STM-1 Frame A1A2 1 in 4 errors, LOF
7179	STM-1 Frame A1A2 errors OFF, LOF
7181	STM-1 140M Pattern Sync loss
7183	STM-1 140M Bit Errors low
7184	STM-1 140M Bit Errors high
7191	STM-1 140M +100 ppm Pattern Sync loss
7193	STM-1 140M +100 ppm Bit Errors low
7194	STM-1 140M +100 ppm Bit Errors high
7201	STM-1 140M -100 ppm Pattern Sync loss
7203	STM-1 140M -100 ppm Bit Errors low
7204	STM-1 140M -100 ppm Bit Errors high
7211	STM-1 VC-3 POH message failure
7221	STM-1 Frame or Pointer Sync Loss
7223	STM-1 VC-3 B3 BIP Errors low
7224	STM-1 VC-3 B3 BIP Errors high
7231	STM-1 Frame or Pointer Sync Loss
7233	STM-1 VC-3 LP-REI Errors low
7234	STM-1 VC-3 LP-REI Errors high
7241	STM-1 TU3 Pattern Sync loss
7243	STM-1 TU3 Bit Errors low
7244	STM-1 TU3 Bit Errors high
7251	STM-1 TU3 TUG[2] Pattern Sync loss
7261	STM-1 TU3 TUG[1] 01010110 Pattern Sync loss
7262	STM-1 TU3 TUG[3] 00001110 Pattern Sync loss
7271	STM-1 TU12 Async, Frame or Pointer Sync Loss
7284	STM-1 TU12 Async, B1 BIP Errors
7294	STM-1 TU12 Async, B2 BIP Errors

SDH Tests A1T, [A1U], A3R	
No.	**Description**
7304	STM-1 TU12 Async, B3 BIP Errors
7314	STM-1 TU12 Async, HP-REI Errors
7324	STM-1 TU12 Async, VC-12 V5 BIP Errors
7334	STM-1 TU12 Async, VC-12 V5 LP-REI Errors
7341	STM-1 TU12 Fl Byte sync, Frame or Pointer Sync Loss
7354	STM-1 TU12 Fl Byte sync, B1 BIP Errors
7364	STM-1 TU12 Fl Byte sync, B2 BIP Errors
7374	STM-1 TU12 Fl Byte sync, B3 BIP Errors
7384	STM-1 TU12 Fl Byte sync, HP-REI Errors
7394	STM-1 TU12 Fl Byte sync, VC-12 V5 BIP Errors
7404	STM-1 TU12 Fl Byte sync, VC-12 V5 LP-REI Errors
7411	STM-1 Frame or Pointer Sync Loss
7413	STM-1 VC-12 V5 BIP Error Rate low
7414	STM-1 VC-12 V5 BIP Error Rate high
7421	STM-1 Frame or Pointer Sync Loss
7423	STM-1 VC-12 V5 LP-REI Error Rate low
7424	STM-1 VC-12 V5 LP-REI Error Rate high
7431	STM-1 TU12 Async, Pattern Sync loss
7433	STM-1 TU12 Async, Bit Errors low
7434	STM-1 TU12 Async, Bit Errors high
7441	STM-1 TU12 Fl Byte sync, Pattern Sync loss
7443	STM-1 TU12 Fl Byte sync, Bit Errors low
7444	STM-1 TU12 Fl Byte sync, Bit Errors high
7451	STM-1 140M PRBS 23 Pattern Sync Loss
7453	STM-1 140M PRBS 23 Bit Errors low
7454	STM-1 140M PRBS 23 Bit Errors high
7461	STM-1 TU3 PRBS 15 Pattern Sync Loss
7463	STM-1 TU3 PRBS 15 Bit Errors low
7464	STM-1 TU3 PRBS 15 Bit Errors high
7471	STM-1 TU12 1100010011110110 Pattern Sync Loss
7473	STM-1 TU12 1100010011110110 Bit Errors low
7474	STM-1 TU12 1100010011110110 Bit Errors high
7481	STM-1 TU2 PRBS 9 Pattern Sync Loss
7483	STM-1 TU2 PRBS 9 Bit Errors low
7484	STM-1 TU2 PRBS 9 Bit Errors high

SDH Tests A1T, [A1U], A3R	
No.	**Description**
7491	STM-1 TU12 Background Pattern same as Test Pattern
7501	STM-1 TU12 Background Pattern failure
7511	STM-1 TU2 Pattern Sync loss
7513	STM-1 TU2 Bit Errors low
7514	STM-1 TU2 Bit Errors high
7521	STM-1 140M Freq Off Ptr Mvts: Frame Sync Loss
7531	STM-1 140M Freq Off Ptr Mvts: Pointer Sync Loss
7544	STM-1 140M Freq Off Ptr Mvts: B1 BIP Errors
7554	STM-1 140M Freq Off Ptr Mvts: B2 BIP Errors
7564	STM-1 140M Freq Off Ptr Mvts: B3 BIP Errors
7573	STM-1 140M Freq Off Ptr Mvts: +100 ppm, Imp VC Offset low
7574	STM-1 140M Freq Off Ptr Mvts: +100 ppm, Imp VC Offset high
7583	STM-1 140M Freq Off Ptr Mvts: -100 ppm, Imp VC Offset low
7584	STM-1 140M Freq Off Ptr Mvts: -100 ppm, Imp VC Offset high
7591	STM-1 TU3 Freq Off Ptr Mvts: Frame Sync Loss
7601	STM-1 TU3 Freq Off Ptr Mvts: Pointer Sync Loss
7614	STM-1 TU3 Freq Off Ptr Mvts: B1 BIP Errors
7624	STM-1 TU3 Freq Off Ptr Mvts: B2 BIP Errors
7634	STM-1 TU3 Freq Off Ptr Mvts: B3 BIP Errors
7644	STM-1 TU3 Freq Off Ptr Mvts: TU BIP Errors
7653	STM-1 TU3 Freq Off Ptr Mvts: +100 ppm, Imp VC Offset low
7654	STM-1 TU3 Freq Off Ptr Mvts: +100 ppm, Imp VC Offset high
7663	STM-1 TU3 Freq Off Ptr Mvts: -100 ppm, Imp VC Offset low
7664	STM-1 TU3 Freq Off Ptr Mvts: -100 ppm, Imp VC Offset high
7671	STM-1 TU12 Freq Off Ptr Mvts: Frame Sync Loss
7681	STM-1 TU12 Freq Off Ptr Mvts: Pointer Sync Loss
7694	STM-1 TU12 Freq Off Ptr Mvts: B1 BIP Errors
7704	STM-1 TU12 Freq Off Ptr Mvts: B2 BIP Errors
7714	STM-1 TU12 Freq Off Ptr Mvts: B3 BIP Errors
7724	STM-1 TU12 Freq Off Ptr Mvts: TU BIP Errors
7733	STM-1 TU12 Freq Off Ptr Mvts: +100 ppm, Imp VC Offset low
7734	STM-1 TU12 Freq Off Ptr Mvts: +100 ppm, Imp VC Offset high
7743	STM-1 TU12 Freq Off Ptr Mvts: -100 ppm, Imp VC Offset low
7744	STM-1 TU12 Freq Off Ptr Mvts: -100 ppm, Imp VC Offset high
7751	STM-1 Thru Mode - No H4 Frame Alignment

SDH Tests A1T, [A1U], A3R	
No.	**Description**
7761	STM-1 RSOH DCC Test Failure
7771	STM-1 MSOH DCC Test Failure
7781	STM-1 AU-4 Bulk TX, AU-4 Unfrm RX : Fail to get PSL
7782	STM-1 AU-4 Bulk: Pattern Sync Loss
7791	STM-1 TU-3 Bulk TX, AU-4 Unfrm RX : Fail to get PSL
7792	STM-1 TU-3 Bulk: Pattern Sync Loss
7801	STM-1 TU-12 Bulk TX, AU-4 Unfrm RX : Fail to get PSL
7802	STM-1 TU-12 Bulk: Pattern Sync Loss
7811	STM-1 DS-3 Unfrm TX, AU-4 Unfrm RX : Fail to get PSL
7812	STM-1 DS-3 Unfrm: Pattern Sync Loss
7821	STM-1 DS-3 M13 TX, AU-4 Unfrm RX : Fail to get PSL
7822	STM-1 DS-3 M13: Pattern Sync Loss
7831	STM-1 DS-3 C-Bit TX, AU-4 Unfrm RX : Fail to get PSL
7832	STM-1 DS-3 C-Bit: Pattern Sync Loss
7841	STM-1 DS-1 Unfrm TX, AU-4 Unfrm RX : Fail to get PSL
7842	STM-1 DS-1 Unfrm: Pattern Sync Loss
7851	STM-1 DS-1 D4 TX, AU-4 Unfrm RX : Fail to get PSL
7852	STM-1 DS-1 D4: Pattern Sync Loss
7861	STM-1 DS-1 ESF TX, AU-4 Unfrm RX : Fail to get PSL
7862	STM-1 DS-1 ESF: Pattern Sync Loss
7871	STM-1 DS-1 SLC-96 TX, AU-4 Unfrm RX : Fail to get PSL
7872	STM-1 DS-1 SLC-96: Pattern Sync Loss
7881	STM-1 AU-4 J0 message failure
7891	STM-1 AU-4 Bulk PRBS 11 Pattern Sync Loss
7893	STM-1 AU-4 Bulk PRBS 11 Bit Errors low
7894	STM-1 AU-4 Bulk PRBS 11 Bit Errors high
7901	STM-1 TU-3 Bulk PRBS 9 Pattern Sync Loss
7903	STM-1 TU-3 Bulk PRBS 9 Bit Errors low
7904	STM-1 TU-3 Bulk PRBS 9 Bit Errors high
7911	STM-1 TU-12 Bulk 1100010011110110 Pattern Sync Loss
7913	STM-1 TU-12 Bulk 1100010011110110 Bit Errors low
7914	STM-1 TU-12 Bulk 1100010011110110 Bit Errors high
7921	STM-1 DS-3 Unfrm PRBS 20 Pattern Sync Loss
7923	STM-1 DS-3 Unfrm PRBS 20 Bit Errors low
7924	STM-1 DS-3 Unfrm PRBS 20 Bit Errors high

SDH Tests A1T, [A1U], A3R	
No.	**Description**
7931	STM-1 DS-1 Unfrm QRSS Pattern Sync Loss
7933	STM-1 DS-1 Unfrm QRSS Bit Errors low
7934	STM-1 DS-1 Unfrm QRSS Bit Errors high
7941	STM-1 TU-3 Mixed Payl: TUG3#2 TU-12 mapping shows PSL
7945	STM-1 TU-3 Mixed Payl: TUG3#2 TU-12 mapping shows TU-AIS"
7946	STM-1 TU-3 Mixed Payl: TUG3#2 TU-12 mapping shows LP-RDI
7947	STM-1 TU-3 Mixed Payl: TUG3#2 TU-12 mapping shows TU-LOP"
7951	STM-1 TU-3 Mixed Payl: TUG3#1 TU-3 mapping shows PSL
7961	STM-1 TU-3 Mixed Payl: TUG3#3 TU-3 mapping shows PSL
7971	STM-1 TU-12 Mixed Payl: TUG3#1 TU-3 mapping shows PSL
7975	STM-1 TU-12 Mixed Payl: TUG3#1 TU-3 mapping shows TU-AIS"
7976	STM-1 TU-12 Mixed Payl: TUG3#1 TU-3 mapping shows LP-RDI
7977	STM-1 TU-12 Mixed Payl: TUG3#1 TU-3 mapping shows TU-LOP"
7981	STM-1 TU-12 Mixed Payl: TUG3#2 TU-12 mapping shows PSL
7991	STM-1 TU-12 Mixed Payl: TUG3#3 TU-12 mapping shows PSL

SDH Tests US1, [US5]	
No.	**Description**
8104	STM-1 B3 BIP Errors
8114	STM-1 HP-REI Errors
8121	STM-1 VC-4 POH message failure
8131	STM-1 Frame or Pointer Sync Loss
8133	STM-1 B1 BIP Errors low
8134	STM-1 B1 BIP Errors high
8141	STM-1 Frame or Pointer Sync Loss
8143	STM-1 B2 BIP Errors low
8144	STM-1 B2 BIP Errors high
8151	STM-1 Frame or Pointer Sync Loss
8153	STM-1 B3 BIP Errors low
8161	STM-1 140M Pattern Sync loss
8163	STM-1 140M Bit Errors low
8164	STM-1 140M Bit Errors high
8171	STM-1 Frame or Pointer Sync Loss
8184	STM-1 B1 BIP Errors

SDH Tests US1, [US5]	
No.	**Description**
8194	STM-1 B2 BIP Errors
8204	STM-1 VC-3 B3 BIP Errors
8214	STM-1 VC-3 LP-REI Errors
8221	STM-1 VC-3 POH message failure
8231	STM-1 Frame or Pointer Sync Loss
8233	STM-1 VC-3 LP-REI Error Rate low
8234	STM-1 VC-3 LP-REI Error Rate high
8241	STM-1 34M Pattern Sync loss
8243	STM-1 34M Bit Error Rate low
8244	STM-1 34M Bit Error Rate high
8251	STM-1 Frame or Pointer Sync Loss
8264	STM-1 B1 BIP Errors
8274	STM-1 B2 BIP Errors
8284	STM-1 B3 BIP Errors
8294	STM-1 HP-REI Errors
8304	STM-1 VC-12 V5 BIP Errors
8314	STM-1 VC-12 V5 LP-REI Errors
8321	STM-1 Frame or Pointer Sync Loss
8323	STM-1 VC-12 V5 BIP Error Rate low
8324	STM-1 VC-12 V5 BIP Error Rate high
8331	STM-1 Frame or Pointer Sync Loss
8333	STM-1 VC-12 V5 LP-REI Error Rate low
8334	STM-1 VC-12 V5 LP-REI Error Rate high
8341	STM-1 2M Pattern Sync loss
8343	STM-1 2M Bit Error Rate low
8344	STM-1 2M Bit Error Rate high
8351	STM-1 140M PRBS 23 Pattern Sync Loss
8354	STM-1 140M PRBS 23 Bit Errors
8361	STM-1 34M PRBS 23 Pattern Sync Loss
8364	STM-1 34M PRBS 23 Bit Errors
8371	STM-1 2M PRBS 23 Pattern Sync Loss
8374	STM-1 2M PRBS 23 Bit Errors
8381	STM-1 2M PRBS 15 Pattern Sync Loss
8384	STM-1 2M PRBS 15 Bit Errors
8391	STM-1 34M PRBS 15 Pattern Sync Loss

SDH Tests US1, [US5]	
No.	**Description**
8394	STM-1 34M PRBS 15 Bit Errors
8401	STM-1 140M PRBS 15 Pattern Sync Loss
8404	STM-1 140M PRBS 15 Bit Errors
8411	STM-1 2M All Ones Pattern Sync Loss
8414	STM-1 2M All Ones Bit Errors
8421	STM-1 34M All Zeros Pattern Sync Loss
8424	STM-1 34M All Zeros Bit Errors
8431	STM-1 140M All Ones Pattern Sync Loss
8434	STM-1 140M All Ones Bit Errors
8441	STM-1 140M 1010 Pattern Sync Loss
8444	STM-1 140M 1010 Bit Errors
8451	STM-1 140M 1100010011110110 Pattern Sync Loss
8454	STM-1 140M 1100010011110110 Bit Errors
8461	STM-1 34M 1111111111111110 Pattern Sync Loss
8464	STM-1 34M 1111111111111110 Bit Errors
8471	STM-1 2M 1100010011110110 Pattern Sync Loss
8474	STM-1 2M 1100010011110110 Bit Errors
8481	STM-1 2M Background Pattern same as Test Pattern
8491	STM-1 2M Background Pattern failure
8511	STM-1 Out of Frame
8512	STM-1 Frame Loss
8521	STM-1 No Out of Frame history
8522	STM-1 Frame Loss history
8531	STM-1 Out of Frame not cancelled
8532	STM-1 Frame Loss
8541	STM-1 Pattern Sync Loss
8553	STM-1 No MS-AIS alarm
8564	STM-1 MS-AIS alarm not cancelled
8571	STM-1 Pattern Sync Loss
8583	STM-1 No MS-RDI alarm
8594	STM-1 MS-RDI alarm not cancelled
8601	STM-1 Pattern Sync Loss
8613	STM-1 No AU-AIS alarm
8624	STM-1 AU-AIS alarm not cancelled
8661	STM-1 Pattern Sync Loss

SDH Tests US1, [US5]	
No.	**Description**
8673	STM-1 No TU3 TU-AIS alarm
8684	STM-1 TU3 TU-AIS alarm not cancelled
8691	STM-1 Pattern Sync Loss
8703	STM-1 No TU3 LP-RDI alarm
8714	STM-1 TU3 LP-RDI alarm not cancelled
8721	STM-1 Pattern Sync Loss
8733	STM-1 No TU12 TU-AIS alarm
8744	STM-1 TU12 TU-AIS alarm not cancelled
8751	STM-1 Pattern Sync Loss
8763	STM-1 No TU12 LP-RDI alarm
8774	STM-1 TU12 LP-RDI alarm not cancelled
8781	STM-1 Clock Loss
8791	STM-1 No Clock Loss
8801	STM-1 Frame or Pointer Sync Loss
8803	STM-1 VC-3 B3 BIP Error Rate low
8804	STM-1 VC-3 B3 BIP Error Rate high
8811	STM-1 K1 byte not equal to 00000000
8812	STM-1 K2 byte not equal to 00000000
8821	STM-1 K1 byte not equal to 11101111
8822	STM-1 K2 byte not equal to 11111101
8831	STM-1 S1 bits not equal to 0000
8841	STM-1 S1 bits not equal to 1111
8851	STM-1 AU-LOP not detected
8852	STM-1 AU-LOP detected
8861	STM-1 TU-LOP not detected
8862	STM-1 TU-LOP detected
8871	STM-1 LOF not detected
8872	STM-1 LOF detected
8883	STM-1 2 Mb/s TU BIP Error Rate low
8884	STM-1 2 Mb/s TU BIP Error Rate high
8893	STM-1 2 Mb/s LP-REI Error Rate low
8894	STM-1 2 Mb/s LP-REI Error Rate high
8901	STM-1 A1A2 OFF - LOF detected
8902	STM-1 A1A2 1 in 4 - LOF detected
8903	STM-1 A1A2 2 in 4 - LOF detected

SDH Tests US1, [US5]	
No.	**Description**
8904	STM-1 A1A2 3 in 4 - LOF detected
8905	STM-1 A1A2 4 in 4 - LOF not detected
8906	STM-1 A1A2 3 in 4 - LOF not detected
8907	STM-1 A1A2 2 in 4 - LOF detected
8908	STM-1 A1A2 1 in 4 - LOF detected
8909	STM-1 A1A2 OFF - LOF detected
8911	STM-1 140 Mb/s struct 64 kb/s delay = 0s - Pattern Loss
8912	STM-1 140 Mb/s struct 64 kb/s delay = 0s - Timeout
8913	STM-1 140 Mb/s struct 64 kb/s delay = 0s - Result low
8914	STM-1 140 Mb/s struct 64 kb/s delay = 0s - Result high
8921	STM-1 140 Mb/s struct 64 kb/s delay = 2s - Pattern Loss
8922	STM-1 140 Mb/s struct 64 kb/s delay = 2s - Timeout
8923	STM-1 140 Mb/s struct 64 kb/s delay = 2s - Result low
8924	STM-1 140 Mb/s struct 64 kb/s delay = 2s - Result high
8931	STM-1 34 Mb/s struct 64 kb/s delay = 0s - Pattern Loss
8932	STM-1 34 Mb/s struct 64 kb/s delay = 0s - Timeout
8933	STM-1 34 Mb/s struct 64 kb/s delay = 0s - Result low
8934	STM-1 34 Mb/s struct 64 kb/s delay = 0s - Result high
8941	STM-1 34 Mb/s struct 64 kb/s delay = 2s - Pattern Loss
8942	STM-1 34 Mb/s struct 64 kb/s delay = 2s - Timeout
8943	STM-1 34 Mb/s struct 64 kb/s delay = 2s - Result low
8944	STM-1 34 Mb/s struct 64 kb/s delay = 2s - Result high
8951	STM-1 2 Mb/s struct 64 kb/s delay = 0s - Pattern Loss
8952	STM-1 2 Mb/s struct 64 kb/s delay = 0s - Timeout
8953	STM-1 2 Mb/s struct 64 kb/s delay = 0s - Result low
8954	STM-1 2 Mb/s struct 64 kb/s delay = 0s - Result high
8961	STM-1 2 Mb/s struct 64 kb/s delay = 2s - Pattern Loss
8962	STM-1 2 Mb/s struct 64 kb/s delay = 2s - Timeout
8963	STM-1 2 Mb/s struct 64 kb/s delay = 2s - Result low
8964	STM-1 2 Mb/s struct 64 kb/s delay = 2s - Result high

Optical Tests UH1/2, URU	
No.	**Description**
9101	STM-1 Optical Signal Loss
9111	STM-1 Optical alarms present
9121	STM-1 Optical Pattern Sync Loss
9124	STM-1 Optical Bit Errors
9131	STM-1 Optical Pattern Sync Loss
9133	STM-1 Optical Bit Error Rate low
9134	STM-1 Optical Bit Error Rate high
9141	STM-1 Optical No Signal Loss
9151	STM-4 Optical STM-1 #1 Signal Loss
9161	STM-4 Optical STM-1 #1 alarms present
9171	STM-4 Optical STM-1 #1 Pattern Sync Loss
9174	STM-4 Optical STM-1 #1 Bit Errors
9181	STM-4 Optical STM-1 #1 Pattern Sync Loss
9183	STM-4 Optical STM-1 #1 Bit Error Rate low
9184	STM-4 Optical STM-1 #1 Bit Error Rate high
9191	STM-4 Optical STM-1 #1 No Signal Loss
9201	STM-4 Optical STM-1 #2 Signal Loss
9211	STM-4 Optical STM-1 #2 alarms present
9221	STM-4 Optical STM-1 #2 Pattern Sync Loss
9224	STM-4 Optical STM-1 #2 Bit Errors
9231	STM-4 Optical STM-1 #2 Pattern Sync Loss
9233	STM-4 Optical STM-1 #2 Bit Error Rate low
9234	STM-4 Optical STM-1 #2 Bit Error Rate high
9241	STM-4 Optical STM-1 #2 No Signal Loss
9251	STM-4 Optical STM-1 #3 Signal Loss
9261	STM-4 Optical STM-1 #3 alarms present
9271	STM-4 Optical STM-1 #3 Pattern Sync Loss
9274	STM-4 Optical STM-1 #3 Bit Errors
9281	STM-4 Optical STM-1 #3 Pattern Sync Loss
9283	STM-4 Optical STM-1 #3 Bit Error Rate low
9284	STM-4 Optical STM-1 #3 Bit Error Rate high
9291	STM-4 Optical STM-1 #3 No Signal Loss
9301	STM-4 Optical STM-1 #4 Signal Loss
9311	STM-4 Optical STM-1 #4 alarms present
9321	STM-4 Optical STM-1 #4 Pattern Sync Loss

Optical Tests UH1/2, URU	
No.	**Description**
9324	STM-4 Optical STM-1 #4 Bit Errors
9331	STM-4 Optical STM-1 #4 Pattern Sync Loss
9333	STM-4 Optical STM-1 #4 Bit Error Rate low
9334	STM-4 Optical STM-1 #4 Bit Error Rate high
9341	STM-4 Optical STM-1 #4 No Signal Loss
9351	STM-4 Optical Frame or Pointer Sync Loss
9364	STM-4 Optical B1 BIP Errors
9374	STM-4 Optical B2 BIP Errors
9382	STM-4 Tx#1 Rx#2 Pattern Loss Not Detected
9383	STM-4 Tx#1 Rx#3 Pattern Loss Not Detected
9384	STM-4 Tx#1 Rx#4 Pattern Loss Not Detected
9391	STM-4 Tx#2 Rx#1 Pattern Loss Not Detected
9393	STM-4 Tx#2 Rx#3 Pattern Loss Not Detected
9394	STM-4 Tx#2 Rx#4 Pattern Loss Not Detected
9401	STM-4 Tx#3 Rx#1 Pattern Loss Not Detected
9402	STM-4 Tx#3 Rx#2 Pattern Loss Not Detected
9404	STM-4 Tx#3 Rx#4 Pattern Loss Not Detected
9411	STM-4 Tx#4 Rx#1 Pattern Loss Not Detected
9412	STM-4 Tx#4 Rx#2 Pattern Loss Not Detected
9413	STM-4 Tx#4 Rx#3 Pattern Loss Not Detected
9421	STM-4 Optical Pattern Sync Loss
9422	STM-4 Optical No MS-AIS alarm
9423	STM-4 Optical MS-AIS alarm not cancelled
9431	STM-4 Optical Pattern Sync Loss
9432	STM-4 Optical No MS-RDI alarm
9433	STM-4 Optical MS-RDI alarm not cancelled

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10011	STM-1 Pattern Sync Loss
10012	STM-1 Signal Loss
10015	STM-1 Pattern Sync Loss
10016	STM-1 Signal Loss
10021	STM-1 LOF, OOF or LOP
10022	STM-1 LOF, OOF or LOP

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10025	STM-1 LOF, OOF or LOP
10026	STM-1 LOF, OOF or LOP
10031	STM-1 Pattern Sync Loss
10033	STM-1 Payload bit error rate low
10034	STM-1 Payload bit error rate high
10035	STM-1 Pattern Sync Loss
10037	STM-1 Payload bit error rate low
10038	STM-1 Payload bit error rate high
10041	STM-1 No LOF, OOF or LOP
10042	STM-1 No signal Loss
10045	STM-1 No LOF, OOF or LOP
10046	STM-1 No signal Loss
10051	STM-1 Stress test LOF or OOF
10055	STM-1 Stress test LOF or OOF
10061	STM-1 Stress test OOF detected
10065	STM-1 Stress test OOF detected
10071	STM-4, STM-1#1 LOF, OOF or LOP
10072	STM-4, STM-1#1 Signal Loss
10075	STM-4, STM-1#1 LOF, OOF or LOP
10076	STM-4, STM-1#1 Signal Loss
10081	STM-4, STM-1#1 Pattern Sync Loss
10083	STM-4, STM-1#1 Payload bit error rate low
10084	STM-4, STM-1#1 Payload bit error rate high
10085	STM-4, STM-1#1 Pattern Sync Loss
10087	STM-4, STM-1#1 Payload bit error rate low
10088	STM-4, STM-1#1 Payload bit error rate high
10091	STM-4, STM-1#1 No LOF, OOF or LOP
10092	STM-4, STM-1#1 No signal Loss
10095	STM-4, STM-1#1 No LOF, OOF or LOP
10096	STM-4, STM-1#1 No signal Loss
10101	STM-4, STM-1#2 LOF, OOF or LOP
10102	STM-4, STM-1#2 Signal Loss
10105	STM-4, STM-1#2 LOF, OOF or LOP
10106	STM-4, STM-1#2 Signal Loss
10111	STM-4, STM-1#2 Pattern Sync Loss

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10113	STM-4, STM-1#2 Payload bit error rate low
10114	STM-4, STM-1#2 Payload bit error rate high
10115	STM-4, STM-1#2 Pattern Sync Loss
10117	STM-4, STM-1#2 Payload bit error rate low
10118	STM-4, STM-1#2 Payload bit error rate high
10121	STM-4, STM-1#2 No LOF, OOF or LOP
10122	STM-4, STM-1#2 No signal Loss
10125	STM-4, STM-1#2 No LOF, OOF or LOP
10126	STM-4, STM-1#2 No signal Loss
10131	STM-4, STM-1#3 LOF, OOF or LOP
10132	STM-4, STM-1#3 Signal Loss
10135	STM-4, STM-1#3 LOF, OOF or LOP
10136	STM-4, STM-1#3 Signal Loss
10141	STM-4, STM-1#3 Pattern Sync Loss
10143	STM-4, STM-1#3 Payload bit error rate low
10144	STM-4, STM-1#3 Payload bit error rate high
10145	STM-4, STM-1#3 Pattern Sync Loss
10147	STM-4, STM-1#3 Payload bit error rate low
10148	STM-4, STM-1#3 Payload bit error rate high
10151	STM-4, STM-1#3 No LOF, OOF or LOP
10152	STM-4, STM-1#3 No signal Loss
10155	STM-4, STM-1#3 No LOF, OOF or LOP
10156	STM-4, STM-1#3 No signal Loss
10161	STM-4, STM-1#4 LOF, OOF or LOP
10162	STM-4, STM-1#4 Signal Loss
10165	STM-4, STM-1#4 LOF, OOF or LOP
10166	STM-4, STM-1#4 Signal Loss
10171	STM-4, STM-1#4 Pattern Sync Loss
10173	STM-4, STM-1#4 Payload bit error rate low
10174	STM-4, STM-1#4 Payload bit error rate high
10175	STM-4, STM-1#4 Pattern Sync Loss
10177	STM-4, STM-1#4 Payload bit error rate low
10178	STM-4, STM-1#4 Payload bit error rate high
10181	STM-4, STM-1#4 No LOF, OOF or LOP
10182	STM-4, STM-1#4 No signal Loss

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10185	STM-4, STM-1#4 No LOF, OOF or LOP
10186	STM-4, STM-1#4 No signal Loss
10191	STM-4, STM-1#1 LOF, OOF or LOP
10192	STM-4, STM-1#1 RS B1 BIP Errors >0
10195	STM-4, STM-1#1 LOF, OOF or LOP
10196	STM-4, STM-1#1 RS B1 BIP Errors >0
10202	STM-4, STM-1#1 MS B2 BIP Errors >0
10206	STM-4, STM-1#1 MS B2 BIP Errors >0
10211	STM-4, STM-1#1 LOF or OOF
10213	STM-4, STM-1#1 MS B2 BIP Errors low
10214	STM-4, STM-1#1 MS B2 BIP Errors high
10215	STM-4, STM-1#1 LOF or OOF
10217	STM-4, STM-1#1 MS B2 BIP Errors low
10218	STM-4, STM-1#1 MS B2 BIP Errors high
10221	STM-4, STM-1#1 LOF, OOF or LOP
10222	STM-4, STM-1#1 Signal Loss
10225	STM-4, STM-1#1 LOF, OOF or LOP
10226	STM-4, STM-1#1 Signal Loss
10231	STM-4,Clock Recovery LOF, OOF or LOP
10235	STM-4,Clock Recovery LOF, OOF or LOP
10241	STM-4,Clock Recovery LOF, OOF or LOP
10245	STM-4,Clock Recovery LOF, OOF or LOP
10251	STM-4,Clock Recovery LOF, OOF or LOP
10255	STM-4,Clock Recovery LOF, OOF or LOP
10261	STM-4 SOH test sync loss
10262	STM-4 MUX4-SOH col147 'a5' error
10265	STM-4 SOH test sync loss
10266	STM-4 MUX4-SOH col147 'a5' error
10271	STM-4 SOH test sync loss
10272	STM-4 MUX4-SOH col147 '5a' error
10275	STM-4 SOH test sync loss
10276	STM-4 MUX4-SOH col147 '5a' error
10281	STM-4 SOH test sync loss
10282	STM-4 MUX4-SOH col147 'a5' error
10285	STM-4 SOH test sync loss

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10286	STM-4 MUX4-SOH col147 'a5' error
10291	STM-4 SOH test sync loss
10292	STM-4 MUX4-SOH col258 'a5' error
10295	STM-4 SOH test sync loss
10296	STM-4 MUX4-SOH col258 'a5' error
10301	STM-4 SOH test sync loss
10302	STM-4 MUX4-SOH col369 'a5' error
10305	STM-4 SOH test sync loss
10306	STM-4 MUX4-SOH col369 'a5' error
10311	STM-4 SOH test sync loss
10312	STM-4 MUX4-SOH col147 '5a' error
10315	STM-4 SOH test sync loss
10316	STM-4 MUX4-SOH col147 '5a' error
10321	STM-4 SOH test sync loss
10322	STM-4 MUX4-SOH col258 '5a' error
10325	STM-4 SOH test sync loss
10326	STM-4 MUX4-SOH col258 '5a' error
10331	STM-4 SOH test sync loss
10332	STM-4 MUX4-SOH col369 '5a' error
10335	STM-4 SOH test sync loss
10336	STM-4 MUX4-SOH col369 '5a' error
10341	STM-4 SOH test sync loss
10342	STM-4#RAM1 SOH col147 pattern error
10345	STM-4 SOH test sync loss
10346	STM-4#RAM1 SOH col147 pattern error
10351	STM-4 SOH test sync loss
10352	STM-4#RAM1 SOH col258 pattern error
10355	STM-4 SOH test sync loss
10356	STM-4#RAM1 SOH col258 pattern error
10361	STM-4 SOH test sync loss
10362	STM-4#RAM1 SOH col369 pattern error
10365	STM-4 SOH test sync loss
10366	STM-4#RAM1 SOH col369 pattern error
10371	STM-4 SOH test sync loss
10372	STM-4#RAM2 SOH col147 pattern error

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10375	STM-4 SOH test sync loss
10376	STM-4#RAM2 SOH col147 pattern error
10381	STM-4 SOH test sync loss
10382	STM-4#RAM2 SOH col258 pattern error
10385	STM-4 SOH test sync loss
10386	STM-4#RAM2 SOH col258 pattern error
10391	STM-4 SOH test sync loss
10392	STM-4#RAM2 SOH col369 pattern error
10395	STM-4 SOH test sync loss
10396	STM-4#RAM2 SOH col369 pattern error
10401	STM-4 SOH test sync loss
10402	STM-4#RAM3 SOH col147 pattern error
10405	STM-4 SOH test sync loss
10406	STM-4#RAM3 SOH col147 pattern error
10411	STM-4 SOH test sync loss
10412	STM-4#RAM3 SOH col258 pattern error
10415	STM-4 SOH test sync loss
10416	STM-4#RAM3 SOH col258 pattern error
10421	STM-4 SOH test sync loss
10422	STM-4#RAM3 SOH col369 pattern error
10425	STM-4 SOH test sync loss
10426	STM-4#RAM3 SOH col369 pattern error
10431	STM-4 SOH test sync loss
10432	STM-4#RAM4 SOH col147 pattern error
10435	STM-4 SOH test sync loss
10436	STM-4#RAM4 SOH col147 pattern error
10441	STM-4 SOH test sync loss
10442	STM-4#RAM4 SOH col258 pattern error
10445	STM-4 SOH test sync loss
10446	STM-4#RAM4 SOH col258 pattern error
10451	STM-4 SOH test sync loss
10452	STM-4#RAM4 SOH col369 pattern error
10455	STM-4 SOH test sync loss
10456	STM-4#RAM4 SOH col369 pattern error
10461	STM-4 SOH test sync loss

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10462	STM-4#RAM1 SOH col147 pattern error
10465	STM-4 SOH test sync loss
10466	STM-4#RAM1 SOH col147 pattern error
10471	STM-4 SOH test sync loss
10472	STM-4#RAM1 SOH col258 pattern error
10475	STM-4 SOH test sync loss
10476	STM-4#RAM1 SOH col258 pattern error
10481	STM-4 SOH test sync loss
10482	STM-4#RAM1 SOH col369 pattern error
10485	STM-4 SOH test sync loss
10486	STM-4#RAM1 SOH col369 pattern error
10491	STM-4 SOH test sync loss
10492	STM-4#RAM2 SOH col147 pattern error
10495	STM-4 SOH test sync loss
10496	STM-4#RAM2 SOH col147 pattern error
10501	STM-4 SOH test sync loss
10502	STM-4#RAM2 SOH col258 pattern error
10505	STM-4 SOH test sync loss
10506	STM-4#RAM2 SOH col258 pattern error
10511	STM-4 SOH test sync loss
10512	STM-4#RAM2 SOH col369 pattern error
10515	STM-4 SOH test sync loss
10516	STM-4#RAM2 SOH col369 pattern error
10521	STM-4 SOH test sync loss
10522	STM-4#RAM3 SOH col147 pattern error
10525	STM-4 SOH test sync loss
10526	STM-4#RAM3 SOH col147 pattern error
10531	STM-4 SOH test sync loss
10532	STM-4#RAM3 SOH col258 pattern error
10535	STM-4 SOH test sync loss
10536	STM-4#RAM3 SOH col258 pattern error
10541	STM-4 SOH test sync loss
10542	STM-4#RAM3 SOH col369 pattern error
10545	STM-4 SOH test sync loss
10546	STM-4#RAM3 SOH col369 pattern error

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10551	STM-4 SOH test sync loss
10552	STM-4#RAM4 SOH col147 pattern error
10555	STM-4 SOH test sync loss
10556	STM-4#RAM4 SOH col147 pattern error
10561	STM-4 SOH test sync loss
10562	STM-4#RAM4 SOH col258 pattern error
10565	STM-4 SOH test sync loss
10566	STM-4#RAM4 SOH col258 pattern error
10571	STM-4 SOH test sync loss
10572	STM-4#RAM4 SOH col369 pattern error
10575	STM-4 SOH test sync loss
10576	STM-4#RAM4 SOH col369 pattern error
10591	STM-4 OOF
10592	STM-4 LOF
10595	STM-4 OOF
10596	STM-4 LOF
10601	STM-4 3 in 4 Frame errors, History OOF
10602	STM-4 3 in 4 Frame errors, History LOF
10605	STM-4 3 in 4 Frame errors, History OOF
10606	STM-4 3 in 4 Frame errors, History LOF
10611	Pattern Sync Loss
10615	Pattern Sync Loss
10622	STM-4 No MS AIS alarm detected
10626	STM-4 No MS AIS alarm detected
10632	STM-4 MS AIS alarm detected
10636	STM-4 MS AIS alarm detected
10641	Pattern Sync Loss
10645	Pattern Sync Loss
10652	STM-4 No MS-RDI alarm detected
10656	STM-4 No MS-RDI alarm detected
10662	STM-4 MS-RDI alarm detected
10666	STM-4 MS-RDI alarm detected
10671	STM-0 Pattern Sync Loss
10672	STM-0 Signal Loss
10675	STM-0 Pattern Sync Loss

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10676	STM-0 Signal Loss
10681	STM-0 LOF, OOF or LOP
10682	STM-0 LOF, OOF or LOP
10685	STM-0 LOF, OOF or LOP
10686	STM-0 LOF, OOF or LOP
10691	STM-0 Pattern Sync Loss
10693	STM-0 Payload bit error rate low
10694	STM-0 Payload bit error rate high
10695	STM-0 Pattern Sync Loss
10697	STM-0 Payload bit error rate low
10698	STM-0 Payload bit error rate high
10701	Pattern Sync Loss
10702	STM-1 Signal Loss
10705	Pattern Sync Loss
10706	STM-1 Signal Loss
10712	STM-1 LOF, OOF or LOP
10716	STM-1 LOF, OOF or LOP
10721	STM-1 Pattern Sync Loss
10723	STM-1 Payload bit error rate low
10724	STM-1 Payload bit error rate high
10725	STM-1 Pattern Sync Loss
10727	STM-1 Payload bit error rate low
10728	STM-1 Payload bit error rate high
10751	STM-4 LOF, OOF or LOP
10752	STM-4 Signal Loss
10755	STM-4 LOF, OOF or LOP
10756	STM-4 Signal Loss
10761	STM-4 Pattern Sync Loss
10763	STM-4, STM-1#1 Payload bit error rate low
10764	STM-4, STM-1#1 Payload bit error rate high
10765	STM-4 Pattern Sync Loss
10767	STM-4, STM-1#1 Payload bit error rate low
10768	STM-4, STM-1#1 Payload bit error rate high
10771	STM-4, STM-1#1 No LOF, OOF or LOP
10772	STM-4, STM-1#1 No signal Loss

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10775	STM-4, STM-1#1 No LOF, OOF or LOP
10776	STM-4, STM-1#1 No signal Loss
10781	STM-4 LOF, OOF or LOP
10782	STM-4, STM-4 B1 BIP errors detected
10792	STM-4, STM-4 B2 BIP errors detected
10801	STM-1 LOF, OOF or LOP
10803	STM-1 Power level low [1310]
10804	STM-1 Power level high [1310]
10805	STM-1 LOF, OOF or LOP
10807	STM-1 Power level low [1550]
10808	STM-1 Power level high [1550]
10811	STM-4 LOF, OOF or LOP
10813	STM-4 Power level low [1310]
10814	STM-4 Power level high [1310]
10815	STM-4 LOF, OOF or LOP
10817	STM-4 Power level low [1550]
10818	STM-4 Power level high [1550]
10821	STM-1 Signal Loss
10823	STM-1 Frequency low
10824	STM-1 Frequency high
10825	STM-1 Signal Loss
10827	STM-1 Frequency low
10828	STM-1 Frequency high
10831	STM-4 Signal Loss
10833	STM-4 Frequency low
10834	STM-4 Frequency high
10835	STM-4 Signal Loss
10837	STM-4 Frequency low
10838	STM-4 Frequency high
10841	STM-4 LOF
10843	STM-4 MS B2 BIP Errors low
10844	STM-4 MS B2 BIP Errors high
10845	STM-4 LOF
10847	STM-4 MS B2 BIP Errors low
10848	STM-4 MS B2 BIP Errors high

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10853	STM-4 A1A2 Errors low
10854	STM-4 A1A2 Errors high
10855	STM-4 RS B1 Errors low
10856	STM-4 RS B1 Errors high
10857	STM-4 MS-REI Errors low
10858	STM-4 MS-REI Errors high
10861	STM-4 LOF
10862	STM-4 OOF
10865	STM-4 LOF
10866	STM-4 OOF
10871	STM-4 LOF
10872	STM-4 No Loss of Signal
10873	STM-4 Loss of Signal
10876	STM-4 No Loss of Signal
10877	STM-4 Loss of Signal
10881	STM-4 LOF
10882	STM-4 No Loss of Signal
10883	STM-4 Loss of Signal
10886	STM-4 No Loss of Signal
10887	STM-4 Loss of Signal
10891	STM-4c POH J1 incorrect
10895	STM-4c POH J1 incorrect
10901	STM-4c 2^23 Pattern Loss
10903	STM-4c 2^23 Bit Errors low
10904	STM-4c 2^23 Bit Errors high
10905	STM-4c 2^23 Pattern Loss
10907	STM-4c 2^23 Bit Errors low
10908	STM-4c 2^23 Bit Errors high
10911	STM-4c 2^15 Pattern Loss
10913	STM-4c 2^15 Bit Errors low
10914	STM-4c 2^15 Bit Errors high
10915	STM-4c 2^15 Pattern Loss
10917	STM-4c 2^15 Bit Errors low
10918	STM-4c 2^15 Bit Errors high
10921	STM-4c Word Pattern Loss

Optical (USN) Tests UKT, [USN]	
No.	**Description**
10923	STM-4c Word Bit Errors low
10924	STM-4c Word Bit Errors high
10925	STM-4c Word Pattern Loss
10927	STM-4c Word Bit Errors low
10928	STM-4c Word Bit Errors high
10931	STM-4c 2^9 Pattern Loss
10933	STM-4c 2^9 Bit Errors low
10934	STM-4c 2^9 Bit Errors high
10935	STM-4c 2^9 Pattern Loss
10937	STM-4c 2^9 Bit Errors low
10938	STM-4c 2^9 Bit Errors high
10941	STM-4c LOF Detected
10942	STM-4c LOP Detected
10943	STM-4c B1 BIP Errors Detected
10944	STM-4c B2 BIP Errors Detected
10945	STM-4c B3 BIP Errors Detected
10953	STM-4c +100 ppm VC Offset - low
10954	STM-4c +100 ppm VC Offset - high
10955	STM-4c -100 ppm VC Offset - low
10956	STM-4c -100 ppm VC Offset - high
10961	STM-4 STM#3 Pattern Sync Loss
10962	STM-4 STM#3 Bit Errors Detected
10965	STM-4 STM#3 Pattern Sync Loss
10966	STM-4 STM#3 Bit Errors Detected
10971	STM-4 STM#1 Pattern Sync Loss"
10972	STM-4 STM#1 Bit Errors <> 1
10973	STM-4 STM#2 Pattern Sync Loss"
10974	STM-4 STM#2 Bit Errors <> 1
10975	STM-4 STM#4 Pattern Sync Loss"
10976	STM-4 STM#4 Bit Errors <> 1

12016 to 12999

Some firmware revs use 12xxx instead of 15xxx for ATM Self Test Fail Numbers.

For Self Test Fail Numbers between 12016 and 12999, use the equivalents for 15016 to 15999 in the Table starting on page 5-64.

Jitter Tests UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	
No.	**Description**
14102	JITTER GEN 2 Mb/s PRBS23 10 UI 5 kHz - no PDH errors
14111	JITTER GEN SDH 10 UI 2 kHz - SDH errors
14121	JITTER GEN SDH 10 UI 5 kHz - SDH errors
14133	JITTER Rx 140 Mb/s PRBS23 - Peak-to-peak too low
14134	JITTER Rx 140 Mb/s PRBS23 - Peak-to-peak too high
14138	JITTER Rx 140 Mb/s - jitter not locked
14139	JITTER Rx 140 Mb/s - VCO not settled
14143	JITTER Rx 140 Mb/s All-zeroes - Peak-to-peak too low
14144	JITTER Rx 140 Mb/s All-zeroes - Peak-to-peak too high
14145	JITTER Rx 140 Mb/s All-zeroes - RMS too low
14146	JITTER Rx 140 Mb/s All-zeroes - RMS too high
14148	JITTER Rx 140 Mb/s - jitter not locked
14153	JITTER Rx 140 Mb/s 1000 - Peak-to-peak too low
14154	JITTER Rx 140 Mb/s 1000 - Peak-to-peak too high
14158	JITTER Rx 140 Mb/s - jitter not locked
14163	JITTER Rx 140 Mb/s All-ones - Peak-to-peak too low
14164	JITTER Rx 140 Mb/s All-ones - Peak-to-peak too high
14168	JITTER Rx 140 Mb/s - jitter not locked
14173	JITTER Rx 34 Mb/s PRBS23 - Peak-to-peak too low
14174	JITTER Rx 34 Mb/s PRBS23 - Peak-to-peak too high
14178	JITTER Rx 34 Mb/s - jitter not locked
14179	JITTER Rx 34 Mb/s - VCO not settled
14183	JITTER Rx 34 Mb/s All-zeroes - Peak-to-peak too low
14184	JITTER Rx 34 Mb/s All-zeroes - Peak-to-peak too high
14185	JITTER Rx 34 Mb/s All-zeroes - RMS too low
14186	JITTER Rx 34 Mb/s All-zeroes - RMS too high
14188	JITTER Rx 34 Mb/s - jitter not locked
14193	JITTER Rx 34 Mb/s 1000 - Peak-to-peak too low
14194	JITTER Rx 34 Mb/s 1000 - Peak-to-peak too high
14198	JITTER Rx 34 Mb/s - jitter not locked
14203	JITTER Rx 34 Mb/s All-ones - Peak-to-peak too low
14204	JITTER Rx 34 Mb/s All-ones - Peak-to-peak too high
14208	JITTER Rx 34 Mb/s - jitter not locked
14213	JITTER Rx 8 Mb/s PRBS23 - Peak-to-peak too low
14214	JITTER Rx 8 Mb/s PRBS23 - Peak-to-peak too high

Jitter Tests UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	
No.	**Description**
14218	JITTER Rx 8 Mb/s - jitter not locked
14219	JITTER Rx 8 Mb/s - VCO not settled
14223	JITTER Rx 8 Mb/s All-zeroes - Peak-to-peak too low
14224	JITTER Rx 8 Mb/s All-zeroes - Peak-to-peak too high
14225	JITTER Rx 8 Mb/s All-zeroes - RMS too low
14226	JITTER Rx 8 Mb/s All-zeroes - RMS too high
14233	JITTER Rx 8 Mb/s 1000 - Peak-to-peak too low
14234	JITTER Rx 8 Mb/s 1000 - Peak-to-peak too high
14243	JITTER Rx 8 Mb/s All-ones - Peak-to-peak too low
14244	JITTER Rx 8 Mb/s All-ones - Peak-to-peak too high
14253	JITTER Rx 2 Mb/s PRBS23 - Peak-to-peak too low
14254	JITTER Rx 2 Mb/s PRBS23 - Peak-to-peak too high
14258	JITTER Rx 2 Mb/s - jitter not locked
14259	JITTER Rx 2 Mb/s - VCO not settled
14263	JITTER Rx 2 Mb/s All-zeroes - Peak-to-peak too low
14264	JITTER Rx 2 Mb/s All-zeroes - Peak-to-peak too high
14265	JITTER Rx 2 Mb/s All-zeroes - RMS too low
14266	JITTER Rx 2 Mb/s All-zeroes - RMS too high
14268	JITTER Rx 140 Mb/s - jitter not locked
14273	JITTER Rx 2 Mb/s 1000 - Peak-to-peak too low
14274	JITTER Rx 2 Mb/s 1000 - Peak-to-peak too high
14278	JITTER Rx 140 Mb/s - jitter not locked
14283	JITTER Rx 2 Mb/s All-ones - Peak-to-peak too low
14284	JITTER Rx 2 Mb/s All-ones - Peak-to-peak too high
14288	JITTER Rx 140 Mb/s - jitter not locked
14293	JITTER GEN+Rx 140 Mb/s All-0's Jit Off - Result too low
14294	JITTER GEN+Rx 140 Mb/s All-0's Jit Off - Result too high
14298	JITTER Gen+Rx 140 Mb/s - jitter not locked
14299	JITTER Gen+Rx 140 Mb/s - VCO not settled
14303	JITTER GEN+Rx 140 Mb/s All-0's 10 UI 100 Hz - Result too low
14304	JITTER GEN+Rx 140 Mb/s All-0's 10 UI 100 Hz - Result too high
14308	JITTER Gen+Rx 140 Mb/s - jitter not locked
14313	JITTER GEN+Rx 140 Mb/s All-0's 1 UI 10 kHz - Result too low
14314	JITTER GEN+Rx 140 Mb/s All-0's 1 UI 10 kHz - Result too high
14315	JITTER GEN+Rx 140 Mb/s All-0's 1 UI 10 kHz - RMS too low

Jitter Tests UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	
No.	**Description**
14316	JITTER GEN+Rx 140 Mb/s All-0's 1 UI 10 kHz - RMS too high
14318	JITTER Gen+Rx 140 Mb/s - jitter not locked
14323	JITTER GEN+Rx 140 Mb/s All-0's 0.6 UI 3 MHz - Result too low
14324	JITTER GEN+Rx 140 Mb/s All-0's 0.6 UI 3 MHz - Result too high
14328	JITTER Gen+Rx 140 Mb/s - jitter not locked
14333	JITTER GEN+Rx 34 Mb/s All-1's Jit Off - Result too low
14334	JITTER GEN+Rx 34 Mb/s All-1's Jit Off - Result too high
14338	JITTER Gen+Rx 34 Mb/s - jitter not locked
14339	JITTER Gen+Rx 34 Mb/s - VCO not settled
14343	JITTER GEN+Rx 34 Mb/s All-1's 10 UI 100 Hz - Result too low
14344	JITTER GEN+Rx 34 Mb/s All-1's 10 UI 100 Hz - Result too high
14348	JITTER Gen+Rx 34 Mb/s - jitter not locked
14353	JITTER GEN+Rx 34 Mb/s All-1's 1 UI 200 kHz - Result too low
14354	JITTER GEN+Rx 34 Mb/s All-1's 1 UI 200 kHz - Result too high
14355	JITTER GEN+Rx 34 Mb/s All-1's 1 UI 200 kHz - RMS too low
14356	JITTER GEN+Rx 34 Mb/s All-1's 1 UI 200 kHz - RMS too high
14358	JITTER Gen+Rx 34 Mb/s - jitter not locked
14363	JITTER GEN+Rx 34 Mb/s All-1's 0.6 UI 500 kHz - Result too low
14364	JITTER GEN+Rx 34 Mb/s All-1's 0.6 UI 500 kHz - Result too high
14368	JITTER Gen+Rx 34 Mb/s - jitter not locked
14373	JITTER GEN+Rx 8 Mb/s All-1's jit-off - Result too low
14374	JITTER GEN+Rx 8 Mb/s All-1's jit-off - Result too high
14378	JITTER Gen+Rx 8 Mb/s - jitter not locked
14379	JITTER Gen+Rx 8 Mb/s - VCO not settled
14383	JITTER GEN+Rx 8 Mb/s All-1's 10 UI 100 Hz - Result too low
14384	JITTER GEN+Rx 8 Mb/s All-1's 10 UI 100 Hz - Result too high
14388	JITTER Gen+Rx 8 Mb/s - jitter not locked
14393	JITTER GEN+Rx 8 Mb/s All-1's 1 UI 100 kHz - Result too low
14394	JITTER GEN+Rx 8 Mb/s All-1's 1 UI 100 kHz - Result too high
14395	JITTER GEN+Rx 8 Mb/s All-1's 1 UI 100 kHz - RMS too low
14396	JITTER GEN+Rx 8 Mb/s All-1's 1 UI 100 kHz - RMS too high
14398	JITTER Gen+Rx 8 Mb/s - jitter not locked
14403	JITTER GEN+Rx 8 Mb/s All-1's 0.6 UI 300 kHz - Result too low
14404	JITTER GEN+Rx 8 Mb/s All-1's 0.6 UI 300 kHz - Result too high
14408	JITTER Gen+Rx 8 Mb/s - jitter not locked

Jitter Tests UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	
No.	**Description**
14413	JITTER GEN+Rx 2 Mb/s All-1's jit-off - Result too low
14414	JITTER GEN+Rx 2 Mb/s All-1's jit-off - Result too high
14418	JITTER Gen+Rx 2 Mb/s - jitter not locked
14419	JITTER Gen+Rx 2 Mb/s - VCO not settled
14423	JITTER GEN+Rx 2 Mb/s All-1's 10 UI 100 Hz - Result too low
14424	JITTER GEN+Rx 2 Mb/s All-1's 10 UI 100 Hz - Result too high
14428	JITTER Gen+Rx 2 Mb/s - jitter not locked
14433	JITTER GEN+Rx 2 Mb/s All-1's 1 UI 25 kHz - Result too low
14434	JITTER GEN+Rx 2 Mb/s All-1's 1 UI 25 kHz - Result too high
14435	JITTER GEN+Rx 2 Mb/s All-1's 1 UI 25 kHz - RMS too low
14436	JITTER GEN+Rx 2 Mb/s All-1's 1 UI 25 kHz - RMS too high
14438	JITTER Gen+Rx 2 Mb/s - jitter not locked
14443	JITTER GEN+Rx 2 Mb/s All-1's 0.6 UI 80 kHz - Result too low
14444	JITTER GEN+Rx 2 Mb/s All-1's 0.6 UI 80 kHz - Result too high
14448	JITTER Gen+Rx 2 Mb/s - jitter not locked
14453	JITTER GEN+RX 2 Mb/s All-1's 1.0 UI 1 kHz - Result too low
14454	JITTER GEN+RX 2 Mb/s All-1's 1.0 UI 1 kHz - Result too high
14458	JITTER GEN+RX 2 Mb/s - jitter not locked
14463	JITTER GEN+RX 8 Mb/s All-1's 1.0 UI 1 kHz - Result too low
14464	JITTER GEN+RX 8 Mb/s All-1's 1.0 UI 1 kHz - Result too high
14468	JITTER GEN+RX 8 Mb/s - jitter not locked
14473	JITTER GEN+RX 34 Mb/s All-1's 1.0 UI 1 kHz - Result too low
14474	JITTER GEN+RX 34 Mb/s All-1's 1.0 UI 1 kHz - Result too high
14478	JITTER GEN+RX 34 Mb/s - jitter not locked
14483	JITTER GEN+RX 140 Mb/s All-1's 1.0 UI 1 kHz - Result too low
14484	JITTER GEN+RX 140 Mb/s All-1's 1.0 UI 1 kHz - Result too high
14488	JITTER GEN+RX 140 Mb/s - jitter not locked
14493	JITTER STM-1E RX 1.6 UI PRBS23 - Result too low
14494	JITTER STM-1E RX 1.6 UI PRBS23 - Result too high
14495	JITTER STM-1E RX 1.6 UI PRBS23 - RMS too low
14496	JITTER STM-1E RX 1.6 UI PRBS23 - RMS too high
14497	JITTER STM-1E RX 1.6 UI PRBS23 - STM LOS
14498	JITTER STM-1E RX 1.6 UI PRBS23 - Jitter not locked
14499	JITTER STM-1E RX 1.6 UI PRBS23 - VCO not settled
14503	JITTER STM-1E RX 1.6 UI All-0's - Result too low

Jitter Tests UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	
No.	**Description**
14504	JITTER STM-1E RX 1.6 UI All 0's - Result too high
14507	JITTER STM-1E RX 1.6 UI All 0's - STM LOS
14508	JITTER STM-1E RX 1.6 UI All 0's - Jitter not locked
14513	JITTER STM-1E RX 1.6 UI All-1's - Result too low
14514	JITTER STM-1E RX 1.6 UI All 1's - Result too high
14517	JITTER STM-1E RX 1.6 UI All 1's - STM LOS
14518	JITTER STM-1E RX 1.6 UI All 1's - Jitter not locked
14523	JITTER STM-1E RX 16 UI PRBS23 - Result too low
14524	JITTER STM-1E RX 16 UI PRBS23 - Result too high
14527	JITTER STM-1E RX 16 UI PRBS23 - STM LOS
14528	JITTER STM-1E RX 16 UI PRBS23 - Jitter not locked
14533	JITTER STM-1E RX 16 UI All-0's - Result too low
14534	JITTER STM-1E RX 16 UI All 0's - Result too high
14537	JITTER STM-1E RX 16 UI All 0's - STM LOS
14538	JITTER STM-1E RX 16 UI All 0's - Jitter not locked
14543	JITTER STM-1E RX 16 UI All-1's - Result too low
14544	JITTER STM-1E RX 16 UI All 1's - Result too high
14547	JITTER STM-1E RX 16 UI All 1's - STM LOS
14548	JITTER STM-1E RX 16 UI All 1's - Jitter not locked
14553	JITTER TX & STM-1E RX TX: OFF - Result too low
14554	JITTER TX & STM-1E RX TX: OFF - Result too high
14557	JITTER TX & STM-1E RX TX: OFF - STM LOS
14558	JITTER TX & STM-1E RX TX: OFF - Jitter not locked
14563	JITTER TX & STM-1E RX 5 UI 100 Hz - Result too low
14564	JITTER TX & STM-1E RX 5 UI 100 Hz - Result too high
14567	JITTER TX & STM-1E RX 5 UI 100 Hz - STM LOS
14568	JITTER TX & STM-1E RX 5 UI 100 Hz - Jitter not locked
14573	JITTER TX & STM-1E RX 5 UI 1 kHz - Result too low
14574	JITTER TX & STM-1E RX 5 UI 1 kHz - Result too high
14577	JITTER TX & STM-1E RX 5 UI 1 kHz - STM LOS
14578	JITTER TX & STM-1E RX 5 UI 1 kHz - Jitter not locked
14583	JITTER TX & STM-1E RX 1 UI 10 kHz - Result too low
14584	JITTER TX & STM-1E RX 1 UI 10 kHz - Result too high
14587	JITTER TX & STM-1E RX 1 UI 10 kHz - STM LOS
14588	JITTER TX & STM-1E RX 1 UI 10 kHz - Jitter not locked

Jitter Tests UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	
No.	**Description**
14593	JITTER TX & STM-1E RX 1 UI 100 kHz - Result too low
14594	JITTER TX & STM-1E RX 1 UI 100 kHz - Result too high
14595	JITTER TX & STM-1E RX 1 UI 100 kHz - RMS too low
14596	JITTER TX & STM-1E RX 1 UI 100 kHz - RMS too high
14597	JITTER TX & STM-1E RX 1 UI 100 kHz - STM LOS
14598	JITTER TX & STM-1E RX 1 UI 100 kHz - Jitter not locked
14603	JITTER TX & STM-1E RX 0.5 UI 1 MHz - Result too low
14604	JITTER TX & STM-1E RX 0.5 UI 1 MHz - Result too high
14607	JITTER TX & STM-1E RX 0.5 UI 1 MHz - STM LOS
14608	JITTER TX & STM-1E RX 0.5 UI 1 MHz - Jitter not locked
14613	JITTER TX & STM-1E RX Hits: 1.0 UI 1 kHz - Result too low
14614	JITTER TX & STM-1E RX Hits: 1.0 UI 1 kHz - Result too high
14617	JITTER TX & STM-1E RX Hits: 1.0 UI 1 kHz - STM LOS
14618	JITTER TX & STM-1E RX Hits: 1.0 UI 1 kHz - Jitter not locked
14623	JITTER STM-1O RX 1.6 UI PRBS23 - Result too low
14624	JITTER STM-1O RX 1.6 UI PRBS23 - Result too high
14625	JITTER STM-1O RX 1.6 UI PRBS23 - RMS too low
14626	JITTER STM-1O RX 1.6 UI PRBS23 - RMS too high
14627	JITTER STM-1O RX 1.6 UI PRBS23 - STM LOL
14628	JITTER STM-1O RX 1.6 UI PRBS23 - Jitter not locked
14629	JITTER STM-1O RX 1.6 UI PRBS23 - VCO not settled
14633	JITTER STM-1O RX 1.6 UI All-0's - Result too low
14634	JITTER STM-1O RX 1.6 UI All 0's - Result too high
14637	JITTER STM-1O RX 1.6 UI All 0's - STM LOL
14638	JITTER STM-1O RX 1.6 UI All 0's - Jitter not locked
14643	JITTER STM-1O RX 1.6 UI All-1's - Result too low
14644	JITTER STM-1O RX 1.6 UI All 1's - Result too high
14647	JITTER STM-1O RX 1.6 UI All 1's - STM LOL
14648	JITTER STM-1O RX 1.6 UI All 1's - Jitter not locked
14653	JITTER STM-1O RX 16 UI PRBS23 - Result too low
14654	JITTER STM-1O RX 16 UI PRBS23 - Result too high
14657	JITTER STM-1O RX 16 UI PRBS23 - STM LOL
14658	JITTER STM-1O RX 16 UI PRBS23 - Jitter not locked
14663	JITTER STM-1O RX 16 UI All-0's - Result too low
14664	JITTER STM-1O RX 16 UI All 0's - Result too high

Jitter Tests UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	
No.	**Description**
14667	JITTER STM-1O RX 16 UI All 0's - STM LOL
14668	JITTER STM-1O RX 16 UI All 0's - Jitter not locked
14673	JITTER STM-1O RX 16 UI All-1's - Result too low
14674	JITTER STM-1O RX 16 UI All 1's - Result too high
14677	JITTER STM-1O RX 16 UI All 1's - STM LOL
14678	JITTER STM-1O RX 16 UI All 1's - Jitter not locked
14683	JITTER TX & STM-1O RX TX: OFF - Result too low
14684	JITTER TX & STM-1O RX TX: OFF - Result too high
14687	JITTER TX & STM-1O RX TX: OFF - STM LOL
14688	JITTER TX & STM-1O RX TX: OFF - Jitter not locked
14693	JITTER TX & STM-1O RX 5 UI 100 Hz - Result too low
14694	JITTER TX & STM-1O RX 5 UI 100 Hz - Result too high
14697	JITTER TX & STM-1O RX 5 UI 100 Hz - STM LOL
14698	JITTER TX & STM-1O RX 5 UI 100 Hz - Jitter not locked
14703	JITTER TX & STM-1O RX 5 UI 1 kHz - Result too low
14704	JITTER TX & STM-1O RX 5 UI 1 kHz - Result too high
14707	JITTER TX & STM-1O RX 5 UI 1 kHz - STM LOL
14708	JITTER TX & STM-1O RX 5 UI 1 kHz - Jitter not locked
14713	JITTER TX & STM-1O RX 1 UI 10 kHz - Result too low
14714	JITTER TX & STM-1O RX 1 UI 10 kHz - Result too high
14717	JITTER TX & STM-1O RX 1 UI 10 kHz - STM LOL
14718	JITTER TX & STM-1O RX 1 UI 10 kHz - Jitter not locked
14723	JITTER TX & STM-1O RX 1 UI 100 kHz - Result too low
14724	JITTER TX & STM-1O RX 1 UI 100 kHz - Result too high
14725	JITTER TX & STM-1O RX 1 UI 100 kHz - RMS too low
14726	JITTER TX & STM-1O RX 1 UI 100 kHz - RMS too high
14727	JITTER TX & STM-1O RX 1 UI 100 kHz - STM LOL
14728	JITTER TX & STM-1O RX 1 UI 100 kHz - Jitter not locked
14733	JITTER TX & STM-1O RX 0.5 UI 1 MHz - Result too low
14734	JITTER TX & STM-1O RX 0.5 UI 1 MHz - Result too high
14737	JITTER TX & STM-1O RX 0.5 UI 1 MHz - STM LOL
14738	JITTER TX & STM-1O RX 0.5 UI 1 MHz - Jitter not locked
14743	JITTER TX & STM-1O RX Hits: 1.0 UI 1 kHz - Result too low
14744	JITTER TX & STM-1O RX Hits: 1.0 UI 1 kHz - Result too high
14747	JITTER TX & STM-1O RX Hits: 1.0 UI 1 kHz - STM LOL

Jitter Tests UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	
No.	**Description**
14748	JITTER TX & STM-1O RX Hits: 1.0 UI 1 kHz - Jitter not locked
14753	JITTER STM-4O RX 1.6 UI PRBS23 - Result too low
14754	JITTER STM-4O RX 1.6 UI PRBS23 - Result too high
14755	JITTER STM-4O RX 1.6 UI PRBS23 - RMS too low
14756	JITTER STM-4O RX 1.6 UI PRBS23 - RMS too high
14757	JITTER STM-4O RX 1.6 UI PRBS23 - STM LOL
14758	JITTER STM-4O RX 1.6 UI PRBS23 - Jitter not locked
14759	JITTER STM-4O RX 1.6 UI PRBS23 - VCO not settled
14763	JITTER STM-4O RX 1.6 UI All-0's - Result too low
14764	JITTER STM-4O RX 1.6 UI All 0's - Result too high
14767	JITTER STM-4O RX 1.6 UI All 0's - STM LOL
14768	JITTER STM-4O RX 1.6 UI All 0's - Jitter not locked
14773	JITTER STM-4O RX 1.6 UI All-1's - Result too low
14774	JITTER STM-4O RX 1.6 UI All 1's - Result too high
14777	JITTER STM-4O RX 1.6 UI All 1's - STM LOL
14778	JITTER STM-4O RX 1.6 UI All 1's - Jitter not locked
14783	JITTER STM-4O RX 16 UI PRBS23 - Result too low
14784	JITTER STM-4O RX 16 UI PRBS23 - Result too high
14787	JITTER STM-4O RX 16 UI PRBS23 - STM LOL
14788	JITTER STM-4O RX 16 UI PRBS23 - Jitter not locked
14793	JITTER STM-4O RX 16 UI All-0's - Result too low
14794	JITTER STM-4O RX 16 UI All 0's - Result too high
14797	JITTER STM-4O RX 16 UI All 0's - STM LOL
14798	JITTER STM-4O RX 16 UI All 0's - Jitter not locked
14803	JITTER STM-4O RX 16 UI All-1's - Result too low
14804	JITTER STM-4O RX 16 UI All 1's - Result too high
14807	JITTER STM-4O RX 16 UI All 1's - STM LOL
14808	JITTER STM-4O RX 16 UI All 1's - Jitter not locked
14813	JITTER TX & STM-4O RX TX: OFF - Result too low
14814	JITTER TX & STM-4O RX TX: OFF - Result too high
14817	JITTER TX & STM-4O RX TX: OFF - STM LOL
14818	JITTER TX & STM-4O RX TX: OFF - Jitter not locked
14823	JITTER TX & STM-4O RX 5 UI 100 Hz - Result too low
14824	JITTER TX & STM-4O RX 5 UI 100 Hz - Result too high
14827	JITTER TX & STM-4O RX 5 UI 100 Hz - STM LOL

Jitter Tests UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	
No.	**Description**
14828	JITTER TX & STM-4O RX 5 UI 100 Hz - Jitter not locked
14833	JITTER TX & STM-4O RX 5 UI 1 kHz - Result too low
14834	JITTER TX & STM-4O RX 5 UI 1 kHz - Result too high
14837	JITTER TX & STM-4O RX 5 UI 1 kHz - STM LOL
14838	JITTER TX & STM-4O RX 5 UI 1 kHz - Jitter not locked
14843	JITTER TX & STM-4O RX 1 UI 10 kHz - Result too low
14844	JITTER TX & STM-4O RX 1 UI 10 kHz - Result too high
14847	JITTER TX & STM-4O RX 1 UI 10 kHz - STM LOL
14848	JITTER TX & STM-4O RX 1 UI 10 kHz - Jitter not locked
14853	JITTER TX & STM-4O RX 1 UI 100 kHz - Result too low
14854	JITTER TX & STM-4O RX 1 UI 100 kHz - Result too high
14855	JITTER TX & STM-4O RX 1 UI 100 kHz - RMS too low
14856	JITTER TX & STM-4O RX 1 UI 100 kHz - RMS too high
14857	JITTER TX & STM-4O RX 1 UI 100 kHz - STM LOL
14858	JITTER TX & STM-4O RX 1 UI 100 kHz - Jitter not locked
14863	JITTER TX & STM-4O RX 0.5 UI 1 MHz - Result too low
14864	JITTER TX & STM-4O RX 0.5 UI 1 MHz - Result too high
14867	JITTER TX & STM-4O RX 0.5 UI 1 MHz - STM LOL
14868	JITTER TX & STM-4O RX 0.5 UI 1 MHz - Jitter not locked
14873	JITTER TX & STM-4O RX Hits: 1.0 UI 1 kHz - Result too low
14874	JITTER TX & STM-4O RX Hits: 1.0 UI 1 kHz - Result too high
14877	JITTER TX & STM-4O RX Hits: 1.0 UI 1 kHz - STM LOL
14878	JITTER TX & STM-4O RX Hits: 1.0 UI 1 kHz - Jitter not locked
14881	JITTER GEN 2 Mb/s PRBS23 80 UI 100 Hz - PDH errors
14889	JITTER GEN 2 Mb/s - VCO not settled
14893	JITTER Gen+Rx 2 Mb/s All-1's 13 UI 100 Hz - Result too low
14894	JITTER Gen+Rx 2 Mb/s All-1's 13 UI 100 Hz - Result too high
14898	JITTER Gen+Rx 2 Mb/s - jitter not locked
14899	JITTER Gen+Rx 2 Mb/s - VCO not settled
14902	JITTER Gen+Rx 2 Mb/s All-1's 20 UI 100 Hz - Over-range not generated
14908	JITTER Gen+Rx 2 Mb/s - jitter not locked
14909	JITTER Gen+Rx 2 Mb/s - VCO not settled
14911	JITTER GEN SDH 50 UI 100 Hz - SDH errors
14923	JITTER TX & STM-1E RX 13 UI 100 Hz - Result too low
14924	JITTER TX & STM-1E RX 13 UI 100 Hz - Result too high

Jitter Tests UHK, UHN, A1M, A1N, A1P [A1Q, A1R, A1S] A3K, 140, A3L, A3V, A3N	
No.	**Description**
14926	JITTER TX & STM-1E RX 13 UI 100 Hz - STM LOS
14928	JITTER TX & STM-1E RX 13 UI 100 Hz - Jitter not locked
14933	JITTER TX & STM-1O RX 13 UI 100 Hz - Result too low
14934	JITTER TX & STM-1O RX 13 UI 100 Hz - Result too high
14936	JITTER TX & STM-1O RX 13 UI 100 Hz - STM LOS
14938	JITTER TX & STM-1O RX 13 UI 100 Hz - Jitter not locked
14943	JITTER TX & STM-4O RX 12 UI 100 Hz - Result too low
14944	JITTER TX & STM-4O RX 12 UI 100 Hz - Result too high
14946	JITTER TX & STM-4O RX 12 UI 100 Hz - STM LOS
14948	JITTER TX & STM-4O RX 12 UI 100 Hz - Jitter not locked

ATM Tests UKN, [USE]	
No.	**Description**
15016	ATM 34 Mb/s - Pattern Loss not detected
15017	ATM 34 Mb/s - Pattern Loss detected
15026	ATM 34 Mb/s - Cell Sync Loss not detected
15027	ATM 34 Mb/s - Cell Sync Loss detected
15036	ATM 34 Mb/s - Selected Cell Not Received not detected
15037	ATM 34 Mb/s - Selected Cell Not Received detected
15046	ATM 34 Mb/s - Congestion Experienced not detected
15047	ATM 34 Mb/s - Congestion Experienced detected
15056	ATM 140 Mb/s - VP-AIS not detected
15057	ATM 140 Mb/s - VP-AIS detected
15066	ATM 140 Mb/s - VP-RDI not detected
15067	ATM 140 Mb/s - VP-RDI detected
15076	ATM 140 Mb/s - VP-LOC not detected
15077	ATM 140 Mb/s - VP-LOC detected
15086	ATM 140 Mb/s - VC-AIS not detected
15087	ATM 140 Mb/s - VC-AIS detected
15096	ATM 2 Mb/s - VC-RDI not detected
15097	ATM 2 Mb/s - VC-RDI detected
15106	ATM 2 Mb/s - VC-LOC not detected
15107	ATM 2 Mb/s - VC-LOC detected
15116	ATM 2 Mb/s - Test Cell Loss not detected
15117	ATM 2 Mb/s - Test Cell Loss detected

ATM Tests UKN, [USE]	
No.	**Description**
15124	ATM 2 Mb/s - Loss of Frame not detected
15125	ATM 2 Mb/s - Loss of Frame detected
15126	ATM 34 Mb/s - Loss of Frame not detected
15127	ATM 34 Mb/s - Loss of Frame detected
15128	ATM 140 Mb/s - Loss of Frame not detected
15129	ATM 140 Mb/s - Loss of Frame detected
15134	ATM 2 Mb/s - RAI not detected
15135	ATM 2 Mb/s - RAI detected
15136	ATM 34 Mb/s - RDI not detected
15137	ATM 34 Mb/s - RDI detected
15138	ATM 140 Mb/s - RDI not detected
15139	ATM 140 Mb/s - RDI detected
15144	ATM 2 Mb/s - AIS not detected
15145	ATM 2 Mb/s - AIS detected
15146	ATM 34 Mb/s - AIS not detected
15147	ATM 34 Mb/s - AIS detected
15148	ATM 140 Mb/s - AIS not detected
15149	ATM 140 Mb/s - AIS detected
15150	ATM 34 Mb/s - F/G rate 80000Cell/sec - Signal Loss
15151	ATM 34 Mb/s - F/G rate 80000Cell/sec - Loss of Cell Synchronization
15152	ATM 34 Mb/s - F/G rate 80000Cell/sec - Pattern Loss
15153	ATM 34 Mb/s - F/G rate 80000Cell/sec - Received Cell Count = Result Low
15154	ATM 34 Mb/s - F/G rate 80000Cell/sec - Received Cell Count = Result High
15155	ATM 34 Mb/s - F/G rate 80000Cell/sec - Selected Cell Not Received detected
15156	ATM 34 Mb/s - F/G rate 80000Cell/sec - Received Cell Count = Result Invalid
15160	ATM 34 Mb/s - F/G rate 40000Cell/sec - Signal Loss
15161	ATM 34 Mb/s - F/G rate 40000Cell/sec - Loss of Cell Synchronization
15162	ATM 34 Mb/s - F/G rate 40000Cell/sec - Pattern Loss
15163	ATM 34 Mb/s - F/G rate 40000Cell/sec - Received Cell Count = Result Low
15164	ATM 34 Mb/s - F/G rate 40000Cell/sec - Received Cell Count = Result High
15165	ATM 34 Mb/s - F/G rate 40000Cell/sec - Selected Cell Not Received detected
15166	ATM 34 Mb/s - F/G rate 40000Cell/sec - Received Cell Count = Result Invalid
15170	ATM 34 Mb/s - F/G rate 100Cell/sec - Signal Loss
15171	ATM 34 Mb/s - F/G rate 100Cell/sec - Loss of Cell Synchronization
15172	ATM 34 Mb/s - F/G rate 100Cell/sec - Pattern Loss

ATM Tests UKN, [USE]	
No.	**Description**
15173	ATM 34 Mb/s - F/G rate 100Cell/sec - Received Cell Count = Result Low
15174	ATM 34 Mb/s - F/G rate 100Cell/sec - Received Cell Count = Result High
15175	ATM 34 Mb/s - F/G rate 100Cell/sec - Selected Cell Not Received detected
15176	ATM 34 Mb/s - F/G rate 100Cell/sec - Received Cell Count = Result Invalid
15180	ATM 34 Mb/s - F/G rate 24000Cell/sec - Signal Loss
15181	ATM 34 Mb/s - F/G rate 24000Cell/sec - Loss of Cell Synchronization
15182	ATM 34 Mb/s - F/G rate 24000Cell/sec - Pattern Loss
15183	ATM 34 Mb/s - F/G rate 24000Cell/sec - Received Cell Count = Result Low
15184	ATM 34 Mb/s - F/G rate 24000Cell/sec - Received Cell Count = Result High
15185	ATM 34 Mb/s - F/G rate 24000Cell/sec - Selected Cell Not Received detected
15186	ATM 34 Mb/s - F/G rate 24000Cell/sec - Received Cell Count = Result Invalid
15190	ATM 34 Mb/s - #1 B/G rate 70% - Signal Loss
15191	ATM 34 Mb/s - #1 B/G rate 70% - Loss of Cell Synchronization
15192	ATM 34 Mb/s - #1 B/G rate 70% - Pattern Loss
15193	ATM 34 Mb/s - #1 B/G rate 70% - Received Cell Count = Result Low
15194	ATM 34 Mb/s - #1 B/G rate 70% - Received Cell Count = Result High
15195	ATM 34 Mb/s - #1 B/G rate 70% - Selected Cell Not Received detected
15196	ATM 34 Mb/s - #1 B/G rate 70% - Received Cell Count = Result Invalid
15200	ATM 34 Mb/s - #1 B/G rate 25% - Signal Loss
15201	ATM 34 Mb/s - #1 B/G rate 25% - Loss of Cell Synchronization
15202	ATM 34 Mb/s - #1 B/G rate 25% - Pattern Loss
15203	ATM 34 Mb/s - #1 B/G rate 25% - Received Cell Count = Result Low
15204	ATM 34 Mb/s - #1 B/G rate 25% - Received Cell Count = Result High
15205	ATM 34 Mb/s - #1 B/G rate 25% - Selected Cell Not Received detected
15206	ATM 34 Mb/s - #1 B/G rate 25% - Received Cell Count = Result Invalid
15210	ATM 34 Mb/s - #2 B/G rate 45% - Signal Loss
15211	ATM 34 Mb/s - #2 B/G rate 45% - Loss of Cell Synchronization
15212	ATM 34 Mb/s - #2 B/G rate 45% - Pattern Loss
15213	ATM 34 Mb/s - #2 B/G rate 45% - Received Cell Count = Result Low
15214	ATM 34 Mb/s - #2 B/G rate 45% - Received Cell Count = Result High
15215	ATM 34 Mb/s - #2 B/G rate 45% - Selected Cell Not Received detected
15216	ATM 34 Mb/s - #2 B/G rate 45% - Received Cell Count = Result Invalid
15220	ATM 34 Mb/s - #2 B/G rate 20% - Signal Loss
15221	ATM 34 Mb/s - #2 B/G rate 20% - Loss of Cell Synchronization
15222	ATM 34 Mb/s - #2 B/G rate 20% - Pattern Loss

ATM Tests UKN, [USE]	
No.	**Description**
15223	ATM 34 Mb/s - #2 B/G rate 20% - Received Cell Count = Result Low
15224	ATM 34 Mb/s - #2 B/G rate 20% - Received Cell Count = Result High
15225	ATM 34 Mb/s - #2 B/G rate 20% - Selected Cell Not Received detected
15226	ATM 34 Mb/s - #2 B/G rate 20% - Received Cell Count = Result Invalid
15230	ATM 34 Mb/s - #3 B/G rate 25% - Signal Loss
15231	ATM 34 Mb/s - #3 B/G rate 25% - Loss of Cell Synchronization
15232	ATM 34 Mb/s - #3 B/G rate 25% - Pattern Loss
15233	ATM 34 Mb/s - #3 B/G rate 25% - Received Cell Count = Result Low
15234	ATM 34 Mb/s - #3 B/G rate 25% - Received Cell Count = Result High
15235	ATM 34 Mb/s - #3 B/G rate 25% - Selected Cell Not Received detected
15236	ATM 34 Mb/s - #3 B/G rate 25% - Received Cell Count = Result Invalid
15240	ATM 34 Mb/s - #3 B/G rate 15% - Signal Loss
15241	ATM 34 Mb/s - #3 B/G rate 15% - Loss of Cell Synchronization
15242	ATM 34 Mb/s - #3 B/G rate 15% - Pattern Loss
15243	ATM 34 Mb/s - #3 B/G rate 15% - Received Cell Count = Result Low
15244	ATM 34 Mb/s - #3 B/G rate 15% - Received Cell Count = Result High
15245	ATM 34 Mb/s - #3 B/G rate 15% - Selected Cell Not Received detected
15246	ATM 34 Mb/s - #3 B/G rate 15% - Received Cell Count = Result Invalid
15250	ATM 34 Mb/s - Fill (Idle) 10% - Signal Loss
15251	ATM 34 Mb/s - Fill (Idle) 10% - Loss of Cell Synchronization
15252	ATM 34 Mb/s - Fill (Idle) 10% - Pattern Loss
15253	ATM 34 Mb/s - Fill (Idle) 10% - Received Cell Count = Result Low
15254	ATM 34 Mb/s - Fill (Idle) 10% - Received Cell Count = Result High
15255	ATM 34 Mb/s - Fill (Idle) 10% - Selected Cell Not Received detected
15256	ATM 34 Mb/s - Fill (Idle) 10% - Received Cell Count = Result Invalid
15260	ATM 34 Mb/s - Periodic 2000Cell/sec - Signal Loss
15261	ATM 34 Mb/s - Periodic 2000Cell/sec - Loss of Cell Synchronization
15262	ATM 34 Mb/s - Periodic 2000Cell/sec - Pattern Loss
15263	ATM 34 Mb/s - Periodic 2000Cell/sec - Received Cell Count = Result Low
15264	ATM 34 Mb/s - Periodic 2000Cell/sec - Received Cell Count = Result High
15265	ATM 34 Mb/s - Periodic 2000Cell/sec - Selected Cell Not Received detected
15266	ATM 34 Mb/s - Periodic 2000Cell/sec - Received Cell Count = Result Invalid
15270	ATM 34 Mb/s - Burst 2000Cell/sec - Signal Loss
15271	ATM 34 Mb/s - Burst 2000Cell/sec - Loss of Cell Synchronization
15272	ATM 34 Mb/s - Burst 2000Cell/sec - Pattern Loss

ATM Tests UKN, [USE]	
No.	**Description**
15273	ATM 34 Mb/s - Burst 2000Cell/sec - Received Cell Count = Result Low
15274	ATM 34 Mb/s - Burst 2000Cell/sec - Received Cell Count = Result High
15275	ATM 34 Mb/s - Burst 2000Cell/sec - Selected Cell Not Received not detected
15276	ATM 34 Mb/s - Burst 2000Cell/sec - Received Cell Count = Result Invalid
15280	ATM 34 Mb/s - Periodic+Burst - Signal Loss
15281	ATM 34 Mb/s - Periodic+Burst - Loss of Cell Synchronization
15282	ATM 34 Mb/s - Periodic+Burst - Pattern Loss
15283	ATM 34 Mb/s - Periodic+Burst - Received Cell Count = Result Low
15284	ATM 34 Mb/s - Periodic+Burst - Received Cell Count = Result High
15285	ATM 34 Mb/s - Periodic+Burst - Selected Cell Not Received detected
15286	ATM 34 Mb/s - Periodic+Burst - Received Cell Count = Result Invalid
15290	ATM 2 Mb/s - CRC4 error add = Signal Loss
15291	ATM 2 Mb/s - CRC4 error add = Loss of Cell Synchronization
15292	ATM 2 Mb/s - CRC4 error add = Pattern Loss
15293	ATM 2 Mb/s - CRC4 error add = OFF Result Low
15294	ATM 2 Mb/s - CRC4 error add = OFF Result High
15295	ATM 2 Mb/s - CRC4 error add = Selected Cell Not Received detected
15296	ATM 2 Mb/s - CRC4 error add = OFF Result Invalid
15297	ATM 2 Mb/s - CRC4 error add = SINGLE Result Low
15298	ATM 2 Mb/s - CRC4 error add = SINGLE Result High
15299	ATM 2 Mb/s - CRC4 error add = SINGLE Result Invalid
15300	ATM 2 Mb/s - REBE error add = Signal Loss
15301	ATM 2 Mb/s - REBE error add = Loss of Cell Synchronization
15302	ATM 2 Mb/s - REBE error add = Pattern Loss
15303	ATM 2 Mb/s - REBE error add = OFF Result Low
15304	ATM 2 Mb/s - REBE error add = OFF Result High
15305	ATM 2 Mb/s - REBE error add = Selected Cell Not Received detected
15306	ATM 2 Mb/s - REBE error add = OFF Result Invalid
15307	ATM 2 Mb/s - REBE error add = SINGLE Result Low
15308	ATM 2 Mb/s - REBE error add = SINGLE Result High
15309	ATM 2 Mb/s - REBE error add = SINGLE Result Invalid
15310	ATM 34 Mb/s - EM BIP error add = Signal Loss
15311	ATM 34 Mb/s - EM BIP error add = Loss of Cell Synchronization
15312	ATM 34 Mb/s - EM BIP error add = Pattern Loss
15313	ATM 34 Mb/s - EM BIP error add = OFF Result Low

ATM Tests UKN, [USE]	
No.	**Description**
15314	ATM 34 Mb/s - EM BIP error add = OFF Result High
15315	ATM 34 Mb/s - EM BIP error add = Selected Cell Not Received detected
15316	ATM 34 Mb/s - EM BIP error add = OFF Result Invalid
15317	ATM 34 Mb/s - EM BIP error add = SINGLE Result Low
15318	ATM 34 Mb/s - EM BIP error add = SINGLE Result High
15319	ATM 34 Mb/s - EM BIP error add = SINGLE Result Invalid
15320	ATM 140 Mb/s - EM BIP error add = Signal Loss
15321	ATM 140 Mb/s - EM BIP error add = Loss of Cell Synchronization
15322	ATM 140 Mb/s - EM BIP error add = Pattern Loss
15323	ATM 140 Mb/s - EM BIP error add = OFF Result Low
15324	ATM 140 Mb/s - EM BIP error add = OFF Result High
15325	ATM 140 Mb/s - EM BIP error add = Selected Cell Not Received detected
15326	ATM 140 Mb/s - EM BIP error add = OFF Result Invalid
15327	ATM 140 Mb/s - EM BIP error add = SINGLE Result Low
15328	ATM 140 Mb/s - EM BIP error add = SINGLE Result High
15329	ATM 140 Mb/s - EM BIP error add = SINGLE Result Invalid
15330	ATM 34 Mb/s - REI error add = Signal Loss
15331	ATM 34 Mb/s - REI error add = Loss of Cell Synchronization
15332	ATM 34 Mb/s - REI error add = Pattern Loss
15333	ATM 34 Mb/s - REI error add = OFF Result Low
15334	ATM 34 Mb/s - REI error add = OFF Result High
15335	ATM 34 Mb/s - REI error add = Selected Cell Not Received detected
15336	ATM 34 Mb/s - REI error add = OFF Result Invalid
15337	ATM 34 Mb/s - REI error add = ON Result Low
15338	ATM 34 Mb/s - REI error add = ON Result High
15339	ATM 34 Mb/s - REI error add = ON Result Invalid
15340	ATM 140 Mb/s - REI error add = Signal Loss
15341	ATM 140 Mb/s - REI error add = Loss of Cell Synchronization
15342	ATM 140 Mb/s - REI error add = Pattern Loss
15343	ATM 140 Mb/s - REI error add = OFF Result Low
15344	ATM 140 Mb/s - REI error add = OFF Result High
15345	ATM 140 Mb/s - REI error add = Selected Cell Not Received detected
15346	ATM 140 Mb/s - REI error add = OFF Result Invalid
15347	ATM 140 Mb/s - REI error add = ON Result Low
15348	ATM 140 Mb/s - REI error add = ON Result High

ATM Tests UKN, [USE]	
No.	**Description**
15349	ATM 140 Mb/s - REI error add = ON Result Invalid
15350	ATM 34 Mb/s - SINGLE HEC error add = Signal Loss
15351	ATM 34 Mb/s - SINGLE HEC error add = Loss of Cell Synchronization
15352	ATM 34 Mb/s - SINGLE HEC error add = Pattern Loss
15353	ATM 34 Mb/s - SINGLE HEC error add = OFF Result Low
15354	ATM 34 Mb/s - SINGLE HEC error add = OFF Result High
15355	ATM 34 Mb/s - SINGLE HEC error add = Selected Cell Not Received detected
15356	ATM 34 Mb/s - SINGLE HEC error add = OFF Result Invalid
15357	ATM 34 Mb/s - SINGLE HEC error add = SINGLE Result Low
15358	ATM 34 Mb/s - SINGLE HEC error add = SINGLE Result High
15359	ATM 34 Mb/s - SINGLE HEC error add = SINGLE Result Invalid
15360	ATM 34 Mb/s - SINGLE HEC error add = Signal Loss
15361	ATM 34 Mb/s - SINGLE HEC error add = Loss of Cell Synchronization
15362	ATM 34 Mb/s - SINGLE HEC error add = Pattern Loss
15363	ATM 34 Mb/s - SINGLE HEC error add = SINGLE (INV HEC) Result Low
15364	ATM 34 Mb/s - SINGLE HEC error add = SINGLE (INV HEC) Result High
15365	ATM 34 Mb/s - SINGLE HEC error add = Selected Cell Not Received detected
15366	ATM 34 Mb/s - SINGLE HEC error add = SINGLE (INV HEC) Result Invalid
15367	ATM 34 Mb/s - SINGLE HEC error add = 1..0E-3 Result Low
15368	ATM 34 Mb/s - SINGLE HEC error add = 1..0E-3 Result High
15369	ATM 34 Mb/s - SINGLE HEC error add = 1..0E-3 Result Invalid
15370	ATM 34 Mb/s - SINGLE HEC error add = Signal Loss
15371	ATM 34 Mb/s - SINGLE HEC error add = Loss of Cell Synchronization
15372	ATM 34 Mb/s - SINGLE HEC error add = Pattern Loss
15373	ATM 34 Mb/s - SINGLE HEC error add = BURST (COR HEC) Result Low
15374	ATM 34 Mb/s - SINGLE HEC error add = BURST (COR HEC) Result High
15375	ATM 34 Mb/s - SINGLE HEC error add = Selected Cell Not Received detected
15376	ATM 34 Mb/s - SINGLE HEC error add = BURST (COR HEC) Result Invalid
15377	ATM 34 Mb/s - SINGLE HEC error add = BURST (INV HEC) Result Low
15378	ATM 34 Mb/s - SINGLE HEC error add = BURST (INV HEC) Result High
15379	ATM 34 Mb/s - SINGLE HEC error add = BURST (INV HEC) Result Invalid
15380	ATM 34 Mb/s - DOUBLE HEC error add = Signal Loss
15381	ATM 34 Mb/s - DOUBLE HEC error add = Loss of Cell Synchronization
15382	ATM 34 Mb/s - DOUBLE HEC error add = Pattern Loss
15383	ATM 34 Mb/s - DOUBLE HEC error add = OFF Result Low

ATM Tests UKN, [USE]	
No.	**Description**
15384	ATM 34 Mb/s - DOUBLE HEC error add = OFF Result High
15385	ATM 34 Mb/s - DOUBLE HEC error add = Selected Cell Not Received detected
15386	ATM 34 Mb/s - DOUBLE HEC error add = OFF Result Invalid
15387	ATM 34 Mb/s - DOUBLE HEC error add = SINGLE Result Low
15388	ATM 34 Mb/s - DOUBLE HEC error add = SINGLE Result High
15389	ATM 34 Mb/s - DOUBLE HEC error add = SINGLE Result Invalid
15390	ATM 34 Mb/s - DOUBLE HEC error add = Signal Loss
15391	ATM 34 Mb/s - DOUBLE HEC error add = Loss of Cell Synchronization
15392	ATM 34 Mb/s - DOUBLE HEC error add = Pattern Loss
15393	ATM 34 Mb/s - DOUBLE HEC error add = SINGLE (COR HEC) Result Low
15394	ATM 34 Mb/s - DOUBLE HEC error add = SINGLE (COR HEC) Result High
15395	ATM 34 Mb/s - DOUBLE HEC error add = Selected Cell Not Received detected
15396	ATM 34 Mb/s - DOUBLE HEC error add = SINGLE (COR HEC) Result Invalid
15397	ATM 34 Mb/s - DOUBLE HEC error add = 1..0E-3 Result Low
15398	ATM 34 Mb/s - DOUBLE HEC error add = 1..0E-3 Result High
15399	ATM 34 Mb/s - DOUBLE HEC error add = 1..0E-3 Result Invalid
15400	ATM 34 Mb/s - DOUBLE HEC error add = Signal Loss
15401	ATM 34 Mb/s - DOUBLE HEC error add = Loss of Cell Synchronization
15402	ATM 34 Mb/s - DOUBLE HEC error add = Pattern Loss
15403	ATM 34 Mb/s - DOUBLE HEC error add = BURST (COR HEC) Result Low
15404	ATM 34 Mb/s - DOUBLE HEC error add = BURST (COR HEC) Result High
15405	ATM 34 Mb/s - DOUBLE HEC error add = Selected Cell Not Received detected
15406	ATM 34 Mb/s - DOUBLE HEC error add = BURST (COR HEC) Result Invalid
15407	ATM 34 Mb/s - DOUBLE HEC error add = BURST (INV HEC) Result Low
15408	ATM 34 Mb/s - DOUBLE HEC error add = BURST (INV HEC) Result High
15409	ATM 34 Mb/s - DOUBLE HEC error add = BURST (INV HEC) Result Invalid
15410	ATM 34 Mb/s - BIT error add = Signal Loss
15411	ATM 34 Mb/s - BIT error add = Loss of Cell Synchronization
15412	ATM 34 Mb/s - BIT error add = Pattern Loss
15413	ATM 34 Mb/s - BIT error add = OFF Result Low
15414	ATM 34 Mb/s - BIT error add = OFF Result High
15415	ATM 34 Mb/s - BIT error add = Selected Cell Not Received detected
15416	ATM 34 Mb/s - BIT error add = OFF Result Invalid
15417	ATM 34 Mb/s - BIT error add = SINGLE Result Low
15418	ATM 34 Mb/s - BIT error add = SINGLE Result High

ATM Tests UKN, [USE]	
No.	**Description**
15419	ATM 34 Mb/s - BIT error add = SINGLE Result Invalid
15420	ATM 34 Mb/s - BIT error add = Signal Loss
15421	ATM 34 Mb/s - BIT error add = Loss of Cell Synchronization
15422	ATM 34 Mb/s - BIT error add = Pattern Loss
15423	ATM 34 Mb/s - BIT error add = SINGLE (Err Cell Cnt) Result Low
15424	ATM 34 Mb/s - BIT error add = SINGLE (Err Cell Cnt) Result High
15425	ATM 34 Mb/s - BIT error add = Selected Cell Not Received detected
15426	ATM 34 Mb/s - BIT error add = SINGLE (Err Cell Cnt) Result Invalid
15427	ATM 34 Mb/s - BIT error add = 1..0E-3 Result Low
15428	ATM 34 Mb/s - BIT error add = 1..0E-3 Result High
15429	ATM 34 Mb/s - BIT error add = 1..0E-3 Result Invalid
15430	ATM 140 Mb/s - F/G GFC = 10 - Signal Loss
15431	ATM 140 Mb/s - F/G GFC = 10 - Loss of Cell Synchronization
15433	ATM 140 Mb/s - F/G GFC = 10 Received Cell Count = Result Low
15434	ATM 140 Mb/s - F/G GFC = 10 Received Cell Count = Result High
15435	ATM 140 Mb/s - F/G GFC = 10 - Selected Cell Not Received detected
15436	ATM 140 Mb/s - F/G GFC = 10 Received Cell Count = Result Invalid
15440	ATM 140 Mb/s - F/G VPI = 85 - Signal Loss
15441	ATM 140 Mb/s - F/G VPI = 85 - Loss of Cell Synchronization
15443	ATM 140 Mb/s - F/G VPI = 85 Received Cell Count = Result Low
15444	ATM 140 Mb/s - F/G VPI = 85 Received Cell Count = Result High
15445	ATM 140 Mb/s - F/G VPI = 85 - Selected Cell Not Received detected
15446	ATM 140 Mb/s - F/G VPI = 85 Received Cell Count = Result Invalid
15450	ATM 140 Mb/s - F/G VPI = 2730 - Signal Loss
15451	ATM 140 Mb/s - F/G VPI = 2730 - Loss of Cell Synchronization
15453	ATM 140 Mb/s - F/G VPI = 2730 Received Cell Count = Result Low
15454	ATM 140 Mb/s - F/G VPI = 2730 Received Cell Count = Result High
15455	ATM 140 Mb/s - F/G VPI = 2730 - Selected Cell Not Received detected
15456	ATM 140 Mb/s - F/G VPI = 2730 Received Cell Count = Result Invalid
15460	ATM 140 Mb/s - F/G VCI = 21845 - Signal Loss
15461	ATM 140 Mb/s - F/G VCI = 21845 - Loss of Cell Synchronization
15463	ATM 140 Mb/s - F/G VCI = 21845 Received Cell Count = Result Low
15464	ATM 140 Mb/s - F/G VCI = 21845 Received Cell Count = Result High
15465	ATM 140 Mb/s - F/G VCI = 21845 - Selected Cell Not Received detected
15466	ATM 140 Mb/s - F/G VCI = 21845 Received Cell Count = Result Invalid

ATM Tests UKN, [USE]	
No.	**Description**
15470	ATM 140 Mb/s - F/G PTI = 000 - Signal Loss
15471	ATM 140 Mb/s - F/G PTI = 000 - Loss of Cell Synchronization
15473	ATM 140 Mb/s - F/G PTI = 000 Received Cell Count = Result Low
15474	ATM 140 Mb/s - F/G PTI = 000 Received Cell Count = Result High
15475	ATM 140 Mb/s - F/G PTI = 000 - Selected Cell Not Received detected
15476	ATM 140 Mb/s - F/G PTI = 000 Received Cell Count = Result Invalid
15480	ATM 140 Mb/s - F/G PTI = 010 - Signal Loss
15481	ATM 140 Mb/s - F/G PTI = 010 - Loss of Cell Synchronization
15483	ATM 140 Mb/s - F/G PTI = 010 Received Cell Count = Result Low
15484	ATM 140 Mb/s - F/G PTI = 010 Received Cell Count = Result High
15485	ATM 140 Mb/s - F/G PTI = 010 - Selected Cell Not Received detected
15486	ATM 140 Mb/s - F/G PTI = 010 Received Cell Count = Result Invalid
15490	ATM 140 Mb/s - F/G CLP = 0 - Signal Loss
15491	ATM 140 Mb/s - F/G CLP = 0 - Loss of Cell Synchronization
15493	ATM 140 Mb/s - F/G CLP = 0 Received Cell Count = Result Low
15494	ATM 140 Mb/s - F/G CLP = 0 Received Cell Count = Result High
15495	ATM 140 Mb/s - F/G CLP = 0 - Selected Cell Not Received detected
15496	ATM 140 Mb/s - F/G CLP = 0 Received Cell Count = Result Invalid
15500	ATM 140 Mb/s - F/G CLP = 1 - Signal Loss
15501	ATM 140 Mb/s - F/G CLP = 1 - Loss of Cell Synchronization
15503	ATM 140 Mb/s - F/G CLP = 1 Received Cell Count = Result Low
15504	ATM 140 Mb/s - F/G CLP = 1 Received Cell Count = Result High
15505	ATM 140 Mb/s - F/G CLP = 1 - Selected Cell Not Received detected
15506	ATM 140 Mb/s - F/G CLP = 1 Received Cell Count = Result Invalid
15510	ATM 140 Mb/s - RX GFC = X - Signal Loss
15511	ATM 140 Mb/s - RX GFC = X - Loss of Cell Synchronization
15513	ATM 140 Mb/s - RX GFC = X Received Cell Count = Result Low
15514	ATM 140 Mb/s - RX GFC = X Received Cell Count = Result High
15515	ATM 140 Mb/s - RX GFC = X - Selected Cell Not Received detected
15516	ATM 140 Mb/s - RX GFC = X Received Cell Count = Result Invalid
15520	ATM 140 Mb/s - RX GFC = 2 - Signal Loss
15521	ATM 140 Mb/s - RX GFC = 2 - Loss of Cell Synchronization
15523	ATM 140 Mb/s - RX GFC = 2 Received Cell Count = Result Low
15524	ATM 140 Mb/s - RX GFC = 2 Received Cell Count = Result High
15525	ATM 140 Mb/s - RX GFC = 2 - Selected Cell Not Received detected

ATM Tests UKN, [USE]	
No.	**Description**
15526	ATM 140 Mb/s - RX GFC = 2 Received Cell Count = Result Invalid
15530	ATM 140 Mb/s - RX VPI = X - Signal Loss
15531	ATM 140 Mb/s - RX VPI = X - Loss of Cell Synchronization
15533	ATM 140 Mb/s - RX VPI = X Received Cell Count = Result Low
15534	ATM 140 Mb/s - RX VPI = X Received Cell Count = Result High
15535	ATM 140 Mb/s - RX VPI = X - Selected Cell Not Received detected
15536	ATM 140 Mb/s - RX VPI = X Received Cell Count = Result Invalid
15540	ATM 140 Mb/s - RX VPI = 0 - Signal Loss
15541	ATM 140 Mb/s - RX VPI = 0 - Loss of Cell Synchronization
15543	ATM 140 Mb/s - RX VPI = 0 Received Cell Count = Result Low
15544	ATM 140 Mb/s - RX VPI = 0 Received Cell Count = Result High
15545	ATM 140 Mb/s - RX VPI = 0 - Selected Cell Not Received detected
15546	ATM 140 Mb/s - RX VPI = 0 Received Cell Count = Result Invalid
15550	ATM 140 Mb/s - RX VPI = 85 - Signal Loss
15551	ATM 140 Mb/s - RX VPI = 85 - Loss of Cell Synchronization
15553	ATM 140 Mb/s - RX VPI = 85 Received Cell Count = Result Low
15554	ATM 140 Mb/s - RX VPI = 85 Received Cell Count = Result High
15555	ATM 140 Mb/s - RX VPI = 85 - Selected Cell Not Received detected
15556	ATM 140 Mb/s - RX VPI = 85 Received Cell Count = Result Invalid
15560	ATM 140 Mb/s - RX VCI = X - Signal Loss
15561	ATM 140 Mb/s - RX VCI = X - Loss of Cell Synchronization
15563	ATM 140 Mb/s - RX VCI = X Received Cell Count = Result Low
15564	ATM 140 Mb/s - RX VCI = X Received Cell Count = Result High
15565	ATM 140 Mb/s - RX VCI = X - Selected Cell Not Received detected
15566	ATM 140 Mb/s - RX VCI = X Received Cell Count = Result Invalid
15570	ATM 140 Mb/s - RX VCI = 33 - Signal Loss
15571	ATM 140 Mb/s - RX VCI = 33 - Loss of Cell Synchronization
15573	ATM 140 Mb/s - RX VCI = 33 Received Cell Count = Result Low
15574	ATM 140 Mb/s - RX VCI = 33 Received Cell Count = Result High
15575	ATM 140 Mb/s - RX VCI = 33 - Selected Cell Not Received detected
15576	ATM 140 Mb/s - RX VCI = 33 Received Cell Count = Result Invalid
15580	ATM 140 Mb/s - RX PTI = XXX - Signal Loss
15581	ATM 140 Mb/s - RX PTI = XXX - Loss of Cell Synchronization
15583	ATM 140 Mb/s - RX PTI = XXX Received Cell Count = Result Low
15584	ATM 140 Mb/s - RX PTI = XXX Received Cell Count = Result High

ATM Tests UKN, [USE]	
No.	**Description**
15585	ATM 140 Mb/s - RX PTI = XXX - Selected Cell Not Received detected
15586	ATM 140 Mb/s - RX PTI = XXX Received Cell Count = Result Invalid
15590	ATM 140 Mb/s - RX PTI = 0XX - Signal Loss
15591	ATM 140 Mb/s - RX PTI = 0XX - Loss of Cell Synchronization
15593	ATM 140 Mb/s - RX PTI = 0XX Received Cell Count = Result Low
15594	ATM 140 Mb/s - RX PTI = 0XX Received Cell Count = Result High
15595	ATM 140 Mb/s - RX PTI = 0XX - Selected Cell Not Received detected
15596	ATM 140 Mb/s - RX PTI = 0XX Received Cell Count = Result Invalid
15600	ATM 140 Mb/s - RX PTI = X1X - Signal Loss
15601	ATM 140 Mb/s - RX PTI = X1X - Loss of Cell Synchronization
15603	ATM 140 Mb/s - RX PTI = X1X Received Cell Count = Result Low
15604	ATM 140 Mb/s - RX PTI = X1X Received Cell Count = Result High
15605	ATM 140 Mb/s - RX PTI = X1X - Selected Cell Not Received detected
15606	ATM 140 Mb/s - RX PTI = X1X Received Cell Count = Result Invalid
15610	ATM 140 Mb/s - RX PTI = XX0 - Signal Loss
15611	ATM 140 Mb/s - RX PTI = XX0 - Loss of Cell Synchronization
15613	ATM 140 Mb/s - RX PTI = XX0 Received Cell Count = Result Low
15614	ATM 140 Mb/s - RX PTI = XX0 Received Cell Count = Result High
15615	ATM 140 Mb/s - RX PTI = XX0 - Selected Cell Not Received detected
15616	ATM 140 Mb/s - RX PTI = XX0 Received Cell Count = Result Invalid
15620	ATM 140 Mb/s - RX CLP = X - Signal Loss
15621	ATM 140 Mb/s - RX CLP = X - Loss of Cell Synchronization
15623	ATM 140 Mb/s - RX CLP = X Received Cell Count = Result Low
15624	ATM 140 Mb/s - RX CLP = X Received Cell Count = Result High
15625	ATM 140 Mb/s - RX CLP = X - Selected Cell Not Received detected
15626	ATM 140 Mb/s - RX CLP = X Received Cell Count = Result Invalid
15630	ATM 140 Mb/s - RX CLP = 0 - Signal Loss
15631	ATM 140 Mb/s - RX CLP = 0 - Loss of Cell Synchronization
15633	ATM 140 Mb/s - RX CLP = 0 Received Cell Count = Result Low
15634	ATM 140 Mb/s - RX CLP = 0 Received Cell Count = Result High
15635	ATM 140 Mb/s - RX CLP = 0 - Selected Cell Not Received detected
15636	ATM 140 Mb/s - RX CLP = 0 Received Cell Count = Result Invalid
15640	ATM 140 Mb/s - RX CLP = 1 - Signal Loss
15641	ATM 140 Mb/s - RX CLP = 1 - Loss of Cell Synchronization
15643	ATM 140 Mb/s - RX CLP = 1 Received Cell Count = Result Low

ATM Tests UKN, [USE]	
No.	**Description**
15644	ATM 140 Mb/s - RX CLP = 1 Received Cell Count = Result High
15645	ATM 140 Mb/s - RX CLP = 1 - Selected Cell Not Received detected
15646	ATM 140 Mb/s - RX CLP = 1 Received Cell Count = Result Invalid
15650	ATM 34 Mb/s - Cross Cell 2^15-1 - Signal Loss
15651	ATM 34 Mb/s - Cross Cell 2^15-1 - Loss of Cell Synchronization
15652	ATM 34 Mb/s - Cross Cell 2^15-1 - Pattern Loss
15654	ATM 34 Mb/s - Cross Cell 2^15-1 - Pattern Errors Present
15655	ATM 34 Mb/s - Cross Cell 2^15-1 - Selected Cell Not Received detected
15656	ATM 34 Mb/s - Cross Cell 2^15-1 - Result Invalid
15660	ATM 34 Mb/s - Cross Cell 2^23-1 - Signal Loss
15661	ATM 34 Mb/s - Cross Cell 2^23-1 - Loss of Cell Synchronization
15662	ATM 34 Mb/s - Cross Cell 2^23-1 - Pattern Loss
15664	ATM 34 Mb/s - Cross Cell 2^23-1 - Pattern Errors Present
15665	ATM 34 Mb/s - Cross Cell 2^23-1 - Selected Cell Not Received detected
15666	ATM 34 Mb/s - Cross Cell 2^23-1 - Result Invalid
15670	ATM 34 Mb/s - Single Cell 2^9-1 - Signal Loss
15671	ATM 34 Mb/s - Single Cell 2^9-1 - Loss of Cell Synchronization
15672	ATM 34 Mb/s - Single Cell 2^9-1 - Pattern Loss
15674	ATM 34 Mb/s - Single Cell 2^9-1 - Pattern Errors Present
15675	ATM 34 Mb/s - Single Cell 2^9-1 - Selected Cell Not Received detected
15676	ATM 34 Mb/s - Single Cell 2^9-1 - Result Invalid
15680	ATM 140 Mb/s - User Word 00000000 - Signal Loss
15681	ATM 140 Mb/s - User Word 00000000 - Loss of Cell Synchronization
15682	ATM 140 Mb/s - User Word 00000000 - Pattern Loss
15684	ATM 140 Mb/s - User Word 00000000 - Pattern Errors Present
15685	ATM 140 Mb/s - User Word 00000000 - Selected Cell Not Received detected
15686	ATM 140 Mb/s - User Word 00000000 - Result Invalid
15690	ATM 140 Mb/s - User Word 11111111 - Signal Loss
15691	ATM 140 Mb/s - User Word 11111111 - Loss of Cell Synchronization
15692	ATM 140 Mb/s - User Word 11111111 - Pattern Loss
15694	ATM 140 Mb/s - User Word 11111111 - Pattern Errors Present
15695	ATM 140 Mb/s - User Word 11111111 - Selected Cell Not Received detected
15696	ATM 140 Mb/s - User Word 11111111 - Result Invalid
15700	ATM 2 Mb/s - User Word 01010101 - Signal Loss
15701	ATM 2 Mb/s - User Word 01010101 - Loss of Cell Synchronization

ATM Tests UKN, [USE]	
No.	**Description**
15702	ATM 2 Mb/s - User Word 01010101 - Pattern Loss
15704	ATM 2 Mb/s - User Word 01010101 - Pattern Errors Present
15705	ATM 2 Mb/s - User Word 01010101 - Selected Cell Not Received detected
15706	ATM 2 Mb/s - User Word 01010101 - Result Invalid
15710	ATM 2 Mb/s - Test Cell - Signal Loss
15711	ATM 2 Mb/s - Test Cell - Loss of Cell Synchronization
15712	ATM 2 Mb/s - Test Cell - Pattern Loss
15714	ATM 2 Mb/s - Test Cell - Pattern Errors Present
15715	ATM 2 Mb/s - Test Cell - Selected Cell Not Received detected
15716	ATM 2 Mb/s - Test Cell - Result Invalid
15720	ATM 34 Mb/s - Single Header error add - Signal Loss
15721	ATM 34 Mb/s - Single Header error add - Loss of Cell Synchronization
15722	ATM 34 Mb/s - Single Header error add - Pattern Loss
15723	ATM 34 Mb/s - Single Header error add - Cell Loss Count = Result Low
15724	ATM 34 Mb/s - Single Header error add - Cell Loss Count = Result High
15725	ATM 34 Mb/s - Single Header error add - Selected Cell Not Received detected
15726	ATM 34 Mb/s - Single Header error add - Cell Loss Count = Result Invalid
15730	ATM 34 Mb/s - Double Header error add - Signal Loss
15731	ATM 34 Mb/s - Double Header error add - Loss of Cell Synchronization
15732	ATM 34 Mb/s - Double Header error add - Pattern Loss
15733	ATM 34 Mb/s - Double Header error add - Cell Loss Count = Result Low
15734	ATM 34 Mb/s - Double Header error add - Cell Loss Count = Result High
15735	ATM 34 Mb/s - Double Header error add - Selected Cell Not Received detected
15736	ATM 34 Mb/s - Double Header error add - Cell Loss Count = Result Invalid
15740	ATM 34 Mb/s - 100msec Double Header error add - Signal Loss
15741	ATM 34 Mb/s - 100msec Double Header error add - Loss of Cell Synchronization
15742	ATM 34 Mb/s - 100msec Double Header error add - Pattern Loss
15743	ATM 34 Mb/s - 100msec Double Header error add - Cell Loss Count = Result Low
15744	ATM 34 Mb/s - 100msec Double Header error add -Cell Loss Count = Result High
15745	ATM 34 Mb/s - 100msec Double Header error add - Selected Cell Not Received detected
15746	ATM 34 Mb/s - 100msec Double Header error add -Cell Loss Count = Result Invalid
15750	ATM 34 Mb/s - Type A - Signal Loss
15751	ATM 34 Mb/s - Type A - Loss of Cell Synchronization
15752	ATM 34 Mb/s - Type A - Pattern Loss
15753	ATM 34 Mb/s - Type A - Misinserted Cell Count = Result Low

ATM Tests UKN, [USE]	
No.	**Description**
15754	ATM 34 Mb/s - Type A - Misinserted Cell Count = Result High
15755	ATM 34 Mb/s - Type A - Selected Cell Not Received detected
15756	ATM 34 Mb/s - Type A - Misinserted Cell Count = Result Invalid
15757	ATM 34 Mb/s - Type A - Errored Cell Count = Result Low
15758	ATM 34 Mb/s - Type A - Errored Cell Count = Result High
15759	ATM 34 Mb/s - Type A - Errored Cell Count = Result Invalid
15760	ATM 34 Mb/s - Type B - Signal Loss
15761	ATM 34 Mb/s - Type B - Loss of Cell Synchronization
15762	ATM 34 Mb/s - Type B - Pattern Loss
15763	ATM 34 Mb/s - Type B - Misinserted Cell Count = Result Low
15764	ATM 34 Mb/s - Type B - Misinserted Cell Count = Result High
15765	ATM 34 Mb/s - Type B - Selected Cell Not Received detected
15766	ATM 34 Mb/s - Type B - Misinserted Cell Count = Result Invalid
15767	ATM 34 Mb/s - Type B - Errored Cell Count = Result Low
15768	ATM 34 Mb/s - Type B - Errored Cell Count = Result High
15769	ATM 34 Mb/s - Type B - Errored Cell Count = Result Invalid
15770	ATM 34 Mb/s - Type C - Signal Loss
15771	ATM 34 Mb/s - Type C - Loss of Cell Synchronization
15772	ATM 34 Mb/s - Type C - Pattern Loss
15773	ATM 34 Mb/s - Type C - Misinserted Cell Count = Result Low
15774	ATM 34 Mb/s - Type C - Misinserted Cell Count = Result High
15775	ATM 34 Mb/s - Type C - Selected Cell Not Received detected
15776	ATM 34 Mb/s - Type C - Misinserted Cell Count = Result Invalid
15777	ATM 34 Mb/s - Type C - Errored Cell Count = Result Low
15778	ATM 34 Mb/s - Type C - Errored Cell Count = Result High
15779	ATM 34 Mb/s - Type C - Errored Cell Count = Result Invalid
15780	ATM 34 Mb/s - Mean Cell Transfer delay = Signal Loss
15781	ATM 34 Mb/s - Mean Cell Transfer delay = Loss of Cell Synchronization
15782	ATM 34 Mb/s - Mean Cell Transfer delay = Pattern Loss
15783	ATM 34 Mb/s - Mean Cell Transfer delay = 0 - Result Low
15784	ATM 34 Mb/s - Mean Cell Transfer delay = 0 - Result High
15785	ATM 34 Mb/s - Mean Cell Transfer delay = Selected Cell Not Received detected
15786	ATM 34 Mb/s - Mean Cell Transfer delay = 0 - Result Invalid
15787	ATM 34 Mb/s - Mean Cell Transfer delay = 307 - Result Low
15788	ATM 34 Mb/s - Mean Cell Transfer delay = 307 - Result High

ATM Tests UKN, [USE]	
No.	**Description**
15789	ATM 34 Mb/s - Mean Cell Transfer delay = 307 - Result Invalid
15790	ATM 34 Mb/s - Gated Mean Cell Transfer delay = Signal Loss
15791	ATM 34 Mb/s - Gated Mean Cell Transfer delay = Loss of Cell Synchronization
15792	ATM 34 Mb/s - Gated Mean Cell Transfer delay = Pattern Loss
15793	ATM 34 Mb/s - Gated Mean Cell Transfer delay = 0 - Result Low
15794	ATM 34 Mb/s - Gated Mean Cell Transfer delay = 0 - Result High
15795	ATM 34 Mb/s -Gated Mean Cell Transfer delay =Selected Cell Not Received detected
15796	ATM 34 Mb/s - Gated Mean Cell Transfer delay = 0 - Result Invalid
15797	ATM 34 Mb/s - Gated Mean Cell Transfer delay = 307 - Result Low
15798	ATM 34 Mb/s - Gated Mean Cell Transfer delay = 307 - Result High
15799	ATM 34 Mb/s - Gated Mean Cell Transfer delay = 307 - Result Invalid
15800	ATM 34 Mb/s - Max Cell Transfer delay = Signal Loss
15801	ATM 34 Mb/s - Max Cell Transfer delay = Loss of Cell Synchronization
15802	ATM 34 Mb/s - Max Cell Transfer delay = Pattern Loss
15803	ATM 34 Mb/s - Max Cell Transfer delay = 0 - Result Low
15804	ATM 34 Mb/s - Max Cell Transfer delay = 0 - Result High
15805	ATM 34 Mb/s - Max Cell Transfer delay = Selected Cell Not Received detected
15806	ATM 34 Mb/s - Max Cell Transfer delay = 0 - Result Invalid
15807	ATM 34 Mb/s - Max Cell Transfer delay = 307 - Result Low
15808	ATM 34 Mb/s - Max Cell Transfer delay = 307 - Result High
15809	ATM 34 Mb/s - Max Cell Transfer delay = 307 - Result Invalid
15810	ATM 34 Mb/s - Pk-to-Pk Cell Transfer delay = Signal Loss
15811	ATM 34 Mb/s - Pk-to-Pk Cell Transfer delay = Loss of Cell Synchronization
15812	ATM 34 Mb/s - Pk-to-Pk Cell Transfer delay = Pattern Loss
15813	ATM 34 Mb/s - Pk-to-Pk Cell Transfer delay = 0 - Result Low
15814	ATM 34 Mb/s - Pk-to-Pk Cell Transfer delay = 0 - Result High
15815	ATM 34 Mb/s - Pk-to-Pk Cell Transfer delay = Selected Cell Not Received detected
15816	ATM 34 Mb/s - Pk-to-Pk Cell Transfer delay = 0 - Result Invalid
15817	ATM 34 Mb/s - Pk-to-Pk Cell Transfer delay = 625 - Result Low
15818	ATM 34 Mb/s - Pk-to-Pk Cell Transfer delay = 625 - Result High
15819	ATM 34 Mb/s - Pk-to-Pk Cell Transfer delay = 625 - Result Invalid
15820	ATM 34 Mb/s - Bit Error Add = OFF (Err Cell)- Signal Loss
15821	ATM 34 Mb/s - Bit Error Add = OFF (Err Cell)- Loss of Cell Synchronization
15822	ATM 34 Mb/s - Bit Error Add = OFF (Err Cell)- Pattern Loss
15823	ATM 34 Mb/s - Bit Error Add = OFF (Err Cell)- Result Low

ATM Tests UKN, [USE]	
No.	**Description**
15824	ATM 34 Mb/s - Bit Error Add = OFF (Err Cell)- Result High
15825	ATM 34 Mb/s - Bit Error Add = OFF (Err Cell)- Selected Cell Not Received detected
15826	ATM 34 Mb/s - Bit Error Add = OFF (Err Cell)- Result Invalid
15830	ATM 34 Mb/s - Bit Error Add = SINGLE (Err Cell)- Signal Loss
15831	ATM 34 Mb/s - Bit Error Add = SINGLE (Err Cell)- Loss of Cell Synchronization
15832	ATM 34 Mb/s - Bit Error Add = SINGLE (Err Cell)- Pattern Loss
15833	ATM 34 Mb/s - Bit Error Add = SINGLE (Err Cell)- Result Low
15834	ATM 34 Mb/s - Bit Error Add = SINGLE (Err Cell)- Result High
15835	ATM 34 Mb/s - Bit Error Add = SINGLE (Err Cell)- Selected Cell Not Received detected
15836	ATM 34 Mb/s - Bit Error Add = SINGLE (Err Cell)- Result Invalid
15840	ATM 34 Mb/s - Bit Error Add = 1.0E-3 (Err Cell)- Signal Loss
15841	ATM 34 Mb/s - Bit Error Add = 1.0E-3 (Err Cell)- Loss of Cell Synchronization
15842	ATM 34 Mb/s - Bit Error Add = 1.0E-3 (Err Cell)- Pattern Loss
15843	ATM 34 Mb/s - Bit Error Add = 1.0E-3 (Err Cell)- Result Low
15844	ATM 34 Mb/s - Bit Error Add = 1.0E-3 (Err Cell)- Result High
15845	ATM 34 Mb/s - Bit Error Add = 1.0E-3 (Err Cell)- Selected Cell Not Received detected
15846	ATM 34 Mb/s - Bit Error Add = 1.0E-3 (Err Cell)- Result Invalid
15850	ATM 34 Mb/s = NCCount - Type A - Signal Loss
15851	ATM 34 Mb/s = NCCount - Type A - Loss of Cell Synchronization
15852	ATM 34 Mb/s = NCCount - Type A - Pattern Loss
15853	ATM 34 Mb/s = NCCount - Type A - Result Low
15854	ATM 34 Mb/s = NCCount - Type A - Result High
15855	ATM 34 Mb/s = NCCount - Type A - Selected Cell Not Received detected
15856	ATM 34 Mb/s = NCCount - Type A - Result Invalid
15860	ATM 34 Mb/s = NCCount - Signal Loss
15861	ATM 34 Mb/s = NCCount - Loss of Cell Synchronization
15862	ATM 34 Mb/s = NCCount - Pattern Loss
15863	ATM 34 Mb/s = NCCount - Type B - Result Low
15864	ATM 34 Mb/s = NCCount - Type B - Result High
15865	ATM 34 Mb/s = NCCount - Selected Cell Not Received detected
15866	ATM 34 Mb/s = NCCount - Type B - Result Invalid
15867	ATM 34 Mb/s = NCCount - Type C - Result Low
15868	ATM 34 Mb/s = NCCount - Type C - Result High
15869	ATM 34 Mb/s = NCCount - Type C - Result Invalid
15870	ATM 34 Mb/s - PCR 20000Cell/sec - Signal Loss

ATM Tests UKN, [USE]	
No.	**Description**
15871	ATM 34 Mb/s - PCR 20000Cell/sec - Loss of Cell Synchronization
15872	ATM 34 Mb/s - PCR 20000Cell/sec - Pattern Loss
15873	ATM 34 Mb/s - PCR 20000Cell/sec - Result Low
15874	ATM 34 Mb/s - PCR 20000Cell/sec - Result High
15875	ATM 34 Mb/s - PCR 20000Cell/sec - Selected Cell Not Received detected
15876	ATM 34 Mb/s - PCR 20000Cell/sec - Result Invalid
15880	ATM 34 Mb/s - PCR 60000Cell/sec - Signal Loss
15881	ATM 34 Mb/s - PCR 60000Cell/sec - Loss of Cell Synchronization
15882	ATM 34 Mb/s - PCR 60000Cell/sec - Pattern Loss
15883	ATM 34 Mb/s - PCR 60000Cell/sec - Result Low
15884	ATM 34 Mb/s - PCR 60000Cell/sec - Result High
15885	ATM 34 Mb/s - PCR 60000Cell/sec - Selected Cell Not Received detected
15886	ATM 34 Mb/s - PCR 60000Cell/sec - Result Invalid
15890	ATM - Trail Trace - Signal Loss
15891	ATM - Trail Trace - Loss of Cell Synchronization
15892	ATM - Trail Trace - Pattern Loss
15895	ATM - Trail Trace - Selected Cell Not Received detected
15896	ATM 34 Mb/s - TEST Trail Trace - String not correct
15897	ATM 140 Mb/s - TEST Trail Trace - String not correct
15898	ATM 34 Mb/s - USER Trail Trace - String not correct
15899	ATM 140 Mb/s - USER Trail Trace - String not correct
15906	ATM 34 Mb/s - LPM - F4 Segment - Loss of Perf Management Not Detected
15907	ATM 34 Mb/s - LPM - F4 Segment - Loss of Perf Management Detected
15916	ATM 34 Mb/s - LPM - F4 End-to-End - Loss of Perf Management Not Detected
15917	ATM 34 Mb/s - LPM - F4 End-to-End - Loss of Perf Management Detected
15926	ATM 34 Mb/s - LPM - F5 Segment - Loss of Perf Management Not Detected
15927	ATM 34 Mb/s - LPM - F5 Segment - Loss of Perf Management Detected
15936	ATM 34 Mb/s - LPM - F5 End-to-End - Loss of Perf Management Not Detected
15937	ATM 34 Mb/s - LPM - F5 End-to-End - Loss of Perf Management Detected
15940	ATM 34 Mb/s - POAM F4 Seg BEDC errors - Signal Loss
15941	ATM 34 Mb/s - POAM F4 Seg BEDC errors - Loss of Cell Synchronization
15942	ATM 34 Mb/s - POAM F4 Seg BEDC errors - Pattern Loss
15943	ATM 34 Mb/s - POAM F4 Seg BEDC errors (0)- Received Cell Count = Result Low
15944	ATM 34 Mb/s - POAM F4 Seg BEDC errors (0) - Received Cell Count = Result High

ATM Tests UKN, [USE]	
No.	**Description**
15945	ATM 34 Mb/s - POAM F4 Seg BEDC errors - Selected Cell Not Received detected
15946	ATM 34 Mb/s - POAM F4 Seg BEDC errors (0) - Received Cell Count = Result Invalid
15947	ATM 34 Mb/s - POAM F4 Seg BEDC errors (3) - Received Cell Count = Result Low
15948	ATM 34 Mb/s - POAM F4 Seg BEDC errors (3) - Received Cell Count = Result High
15949	ATM 34 Mb/s - POAM F4 Seg BEDC errors (3) - Received Cell Count = Result Invalid
15950	ATM 34 Mb/s - POAM F4 End BEDC errors - Signal Loss
15951	ATM 34 Mb/s - POAM F4 End BEDC errors - Loss of Cell Synchronization
15952	ATM 34 Mb/s - POAM F4 End BEDC errors - Pattern Loss
15953	ATM 34 Mb/s - POAM F4 End BEDC errors (0) - Received Cell Count = Result Low
15954	ATM 34 Mb/s - POAM F4 End BEDC errors (0) - Received Cell Count = Result High
15955	ATM 34 Mb/s - POAM F4 End BEDC errors - Selected Cell Not Received detected
15956	ATM 34 Mb/s - POAM F4 End BEDC errors (0) - Received Cell Count = Result Invalid
15957	ATM 34 Mb/s - POAM F4 End BEDC errors (3) - Received Cell Count = Result Low
15958	ATM 34 Mb/s - POAM F4 End BEDC errors (3) - Received Cell Count = Result High
15959	ATM 34 Mb/s - POAM F4 End BEDC errors (3) -Received Cell Count = Result Invalid
15960	ATM 34 Mb/s - POAM F5 Seg BEDC errors - Signal Loss
15961	ATM 34 Mb/s - POAM F5 Seg BEDC errors - Loss of Cell Synchronization
15962	ATM 34 Mb/s - POAM F5 Seg BEDC errors - Pattern Loss
15963	ATM 34 Mb/s - POAM F5 Seg BEDC errors (0) - Received Cell Count = Result Low
15964	ATM 34 Mb/s - POAM F5 Seg BEDC errors (0) - Received Cell Count = Result High
15965	ATM 34 Mb/s - POAM F5 Seg BEDC errors - Selected Cell Not Received detected
15966	ATM 34 Mb/s - POAM F5 Seg BEDC errors (0) - Received Cell Count = Result Invalid
15967	ATM 34 Mb/s - POAM F5 Seg BEDC errors (3) - Received Cell Count = Result Low
15968	ATM 34 Mb/s - POAM F5 Seg BEDC errors (3) - Received Cell Count = Result High
15969	ATM 34 Mb/s - POAM F5 Seg BEDC errors (3) - Received Cell Count = Result Invalid
15970	ATM 34 Mb/s - POAM F5 End BEDC errors - Signal Loss
15971	ATM 34 Mb/s - POAM F5 End BEDC errors - Loss of Cell Synchronization
15972	ATM 34 Mb/s - POAM F5 End BEDC errors - Pattern Loss
15973	ATM 34 Mb/s - POAM F5 End BEDC errors (0) - Received Cell Count = Result Low
15974	ATM 34 Mb/s - POAM F5 End BEDC errors (0) - Received Cell Count = Result High
15975	ATM 34 Mb/s - POAM F5 End BEDC errors - Selected Cell Not Received detected
15976	ATM 34 Mb/s - POAM F5 End BEDC errors (0) - Received Cell Count = Result Invalid
15977	ATM 34 Mb/s - POAM F5 End BEDC errors (3) - Received Cell Count = Result Low

ATM Tests UKN, [USE]	
No.	**Description**
15978	ATM 34 Mb/s - POAM F5 End BEDC errors (3) - Received Cell Count = Result High
15979	ATM 34 Mb/s - POAM F5 End BEDC errors (3) - Received Cell Count = Result Invalid
15980	ATM 34 Mb/s - POAM Cell loss errors - Signal Loss
15981	ATM 34 Mb/s - POAM Cell loss errors - Loss of Cell Synchronization
15982	ATM 34 Mb/s - POAM Cell loss errors - Pattern Loss
15983	ATM 34 Mb/s - POAM Cell loss errors - Result Low
15984	ATM 34 Mb/s - POAM Cell loss errors - Result High
15985	ATM 34 Mb/s - POAM Cell loss errors - Selected Cell Not Received detected
15986	ATM 34 Mb/s - POAM Cell loss errors - Result Invalid
15987	ATM 34 Mb/s - BEDC errors - Result Low
15988	ATM 34 Mb/s - BEDC errors - Result High
15989	ATM 34 Mb/s - BEDC errors - Result Invalid
15990	ATM 34 Mb/s - POAM Cell misinsertion errors - Signal Loss
15991	ATM 34 Mb/s - POAM Cell misinsertion errors - Loss of Cell Synchronization
15992	ATM 34 Mb/s - POAM Cell misinsertion errors - Pattern Loss
15993	ATM 34 Mb/s - POAM Cell misinsertion errors - Result Low
15994	ATM 34 Mb/s - POAM Cell misinsertion errors - Result High
15995	ATM 34 Mb/s - POAM Cell misinsertion errors - Selected Cell Not Received detected
15996	ATM 34 Mb/s - POAM Cell misinsertion errors - Result Invalid
15997	ATM 34 Mb/s - BEDC errors - Result Low
15998	ATM 34 Mb/s - BEDC errors - Result High
15999	ATM 34 Mb/s - BEDC errors - Result Invalid

No.	**Description**
16200	Locked during jitter mask sweep and auto tolerance

SPDH Tests 110	
No.	**Description**
18003	SPDH DS3 - FAS error add = 1.0E-3 Result low
18004	SPDH DS3 - FAS error add = 1.0E-3 Result high
18006	SPDH DS3 - FAS error add = 1.0E-3 Result Invalid
18013	SPDH DS3 - BIT error add = OFF Result low
18014	SPDH DS3 - BIT error add = OFF Result high
18016	SPDH DS3 - BIT error add = OFF Result Invalid
18023	SPDH DS3 - BIT error add = SINGLE Result low
18024	SPDH DS3 - BIT error add = SINGLE Result high
18026	SPDH DS3 - BIT error add = SINGLE Result Invalid
18033	SPDH DS3 - BIT error add = 1.0E-3 Result low
18034	SPDH DS3 - BIT error add = 1.0E-3 Result high
18036	SPDH DS3 - BIT error add = 1.0E-3 Result Invalid
18043	SPDH DS1 - FAS (D4) error add = OFF Result low
18044	SPDH DS1 - FAS (D4) error add = OFF Result high
18046	SPDH DS1 - FAS (D4) error add = OFF Result Invalid
18053	SPDH DS1 - FAS (D4) error add = SINGLE Result low
18054	SPDH DS1 - FAS (D4) error add = SINGLE Result high
18056	SPDH DS1 - FAS (D4) error add = SINGLE Result Invalid
18063	SPDH DS1 - FAS (D4) error add = 1.0E-3 Result low
18064	SPDH DS1 - FAS (D4) error add = 1.0E-3 Result high
18066	SPDH DS1 - FAS (D4) error add = 1.0E-3 Result Invalid
18073	SPDH DS1 - BIT error add = OFF Result low
18074	SPDH DS1 - BIT error add = OFF Result high
18076	SPDH DS1 - BIT error add = OFF Result Invalid
18083	SPDH DS1 - BIT error add = SINGLE Result low
18084	SPDH DS1 - BIT error add = SINGLE Result high
18086	SPDH DS1 - BIT error add = SINGLE Result Invalid
18093	SPDH DS1 - BIT error add = 1.0E-3 Result low
18094	SPDH DS1 - BIT error add = 1.0E-3 Result high
18096	SPDH DS1 - BIT error add = 1.0E-3 Result Invalid
18103	SPDH DS1 - FAS (SLC96) error add = OFF Result low
18104	SPDH DS1 - FAS (SLC96) error add = OFF Result high
18106	SPDH DS1 - FAS (SLC96) error add = OFF Result Invalid
18113	SPDH DS1 - FAS (SLC96) error add = SINGLE Result low
18114	SPDH DS1 - FAS (SLC96) error add = SINGLE Result high

SPDH Tests 110	
No.	**Description**
18116	SPDH DS1 - FAS (SLC96) error add = SINGLE Result Invalid
18123	SPDH DS1 - FAS (SLC96) error add = 1.0E-3 Result low
18124	SPDH DS1 - FAS (SLC96) error add = 1.0E-3 Result high
18126	SPDH DS1 - FAS (SLC96) error add = 1.0E-3 Result Invalid
18137	SPDH DS3 Unframed - Loss Of Frame Detected
18146	SPDH DS3 M23 - Loss Of Frame Not Detected
18147	SPDH DS3 M23 - Loss Of Frame Detected
18156	SPDH DS3 C-BIT - Loss Of Frame Not Detected
18157	SPDH DS3 C-BIT - Loss Of Frame Detected
18167	SPDH DS1 Unframed - Loss Of Frame Detected
18176	SPDH DS1 D4 - Loss Of Frame Not Detected
18177	SPDH DS1 D4 - Loss Of Frame Detected
18186	SPDH DS1 ESF - Loss Of Frame Not Detected
18187	SPDH DS1 ESF - Loss Of Frame Detected
18196	SPDH DS1 SLC96 - Loss Of Frame Not Detected
18197	SPDH DS1 SLC96 - Loss Of Frame Detected
18206	SPDH DS1 DROP from DS3 - Loss Of Frame Not Detected
18207	SPDH DS1 DROP from DS3 - Loss Of Frame Detected
18211	SPDH DS3 struct 64 kb/s - Pattern Loss
18214	SPDH DS3 struct 64 kb/s - Pattern Errors Present
18221	SPDH DS3 struct Nx64 kb/s (odd channels) - Pattern Loss
18224	SPDH DS3 struct Nx64 kb/s (odd channels) - Pattern Errors Present
18231	SPDH DS3 struct DS1 - Pattern Loss
18234	SPDH DS3 struct DS1 - Pattern Errors Present
18241	SPDH DS3 struct 56 kb/s - Pattern Loss
18244	SPDH DS3 struct 56 kb/s - Pattern Errors Present
18251	SPDH DS3 struct Nx56 kb/s (odd channels) - Pattern Loss
18254	SPDH DS3 struct Nx56 kb/s (odd channels) - Pattern Errors Present
18261	SPDH DS3 struct Nx56 kb/s (even channels) - Pattern Loss
18264	SPDH DS3 struct Nx56 kb/s (even channels) - Pattern Errors Present
18271	SPDH DS1 struct 64 kb/s - Pattern Loss
18274	SPDH DS1 struct 64 kb/s - Pattern Errors Present
18281	SPDH DS1 struct Nx64 kb/s (odd channels) - Pattern Loss
18284	SPDH DS1 struct Nx64 kb/s (odd channels) - Pattern Errors Present
18291	SPDH DS1 struct 56 kb/s - Pattern Loss

SPDH Tests 110	
No.	**Description**
18294	SPDH DS1 struct 56 kb/s - Pattern Errors Present
18301	SPDH DS1 struct Nx56 kb/s (even channels) - Pattern Loss
18304	SPDH DS1 struct Nx56 kb/s (even channels) - Pattern Errors Present
18311	SPDH DS3 Unframed - PRBS(9) INV Pattern Loss
18314	SPDH DS3 Unframed - PRBS(9) INV Pattern Errors Present
18321	SPDH DS3 Unframed - PRBS(20) NON-INV Pattern Loss
18324	SPDH DS3 Unframed - PRBS(20) NON-INV Pattern Errors Present
18331	SPDH DS3 Unframed - PRBS(15) INV Pattern Loss
18334	SPDH DS3 Unframed - PRBS(15) INV Pattern Errors Present
18341	SPDH DS3 Unframed - PRBS(23) NON-INV Pattern Loss
18344	SPDH DS3 Unframed - PRBS(23) NON-INV Pattern Errors Present
18351	SPDH DS3 Unframed - User Word Pattern Loss
18354	SPDH DS3 Unframed - User Word Pattern Errors Present
18361	SPDH DS1 Unframed - PRBS(9) NON-INV Pattern Loss
18364	SPDH DS1 Unframed - PRBS(9) NON-INV Pattern Errors Present
18371	SPDH DS1 Unframed - PRBS(11) INV Pattern Loss
18374	SPDH DS1 Unframed - PRBS(11) INV Pattern Errors Present
18381	SPDH DS1 Unframed - QRSS Pattern Loss
18384	SPDH DS1 Unframed - QRSS Pattern Errors Present
18391	SPDH DS1 Unframed - PRBS(23) INV Pattern Loss
18394	SPDH DS1 Unframed - PRBS(23) INV Pattern Errors Present
18401	SPDH DS1 Unframed - User Word Pattern Loss
18404	SPDH DS1 Unframed - User Word Pattern Errors Present
18411	SPDH DS3 struct DS1 insert/drop - Insert Port Not Settled
18414	SPDH DS3 struct DS1 insert/drop - Drop Port Not Settled
18421	SPDH DS3 struct 56 kb/s delay = 0s - Result Invalid
18422	SPDH DS3 struct 56 kb/s delay = 0s - Timeout
18423	SPDH DS3 struct 56 kb/s delay = 0s - Result low
18424	SPDH DS3 struct 56 kb/s delay = 0s - Result high
18431	SPDH DS3 struct 56 kb/s delay = 2s - Result Invalid
18432	SPDH DS3 struct 56 kb/s delay = 2s - Timeout
18433	SPDH DS3 struct 56 kb/s delay = 2s - Result low
18434	SPDH DS3 struct 56 kb/s delay = 2s - Result high
18441	SPDH DS1 struct 56 kb/s delay = 0s - Result Invalid
18442	SPDH DS1 struct 56 kb/s delay = 0s - Timeout

SPDH Tests 110	
No.	**Description**
18443	SPDH DS1 struct 56 kb/s delay = 0s - Result low
18444	SPDH DS1 struct 56 kb/s delay = 0s - Result high
18451	SPDH DS1 struct 56 kb/s delay = 2s - Result Invalid
18452	SPDH DS1 struct 56 kb/s delay = 2s - Timeout
18453	SPDH DS1 struct 56 kb/s delay = 2s - Result low
18454	SPDH DS1 struct 56 kb/s delay = 2s - Result high

SDH Tests A1T, [A1U], A3R	
No.	**Description**
22001	"STM-1 TU-12 DS-1 F/G Patt: Unframed shows PSL
22002	"STM-1 TU-12 DS-1 B/G Patt: Expected D4 framing shows PSL
22011	"STM-1 TU-12 DS-1 F/G Patt: Expected ESF framing shows PSL
22012	"STM-1 TU-12 DS-1 B/G Patt: Expected D4 framing shows PSL
22021	"STM-1 AU-4 Pattern Sync Loss
22025	"STM-1 AU-4 Service Disruption : Short Burst <> 0 ms
22026	"STM-1 AU-4 Service Disruption : Long Burst <> 0 ms
22027	"STM-1 AU-4 Service Disruption : Last Burst <> 0 ms
22031	"STM-1 AU-4 Pattern Sync Loss
22035	"STM-1 AU-4 Service Disruption : Short Burst <> 0 ms
22036	"STM-1 AU-4 Service Disruption : Long Burst not OVERRANGE
22037	"STM-1 AU-4 Service Disruption : Last Burst not OVERRANGE
22041	"STM-1 AU-4 Pattern Sync Loss
22045	"STM-1 AU-4 Service Disruption : Short Burst <0 ms or >2000 ms
22046	"STM-1 AU-4 Service Disruption : Long Burst <> Short Burst
22047	"STM-1 AU-4 Service Disruption : Last Burst <> Short Burst
22051	"STM-0 Signal Loss
22061	"STM-0 Pattern Sync Loss
22064	"STM-0 Bit Errors
22071	"STM-0 Signal Loss
22081	"STM-0 AU-3 Pattern Sync loss (TX Pulse HI, RX HI)
22084	"STM-0 AU-3 Bit Errors (TX Pulse = HI, RX Pulse = HI)
22091	"STM-0 AU-3 Pattern Sync loss (TX Pulse LO, RX LO)
22094	"STM-0 AU-3 Bit Errors (TX Pulse = LO, RX Pulse = LO)
22101	"STM-0 AU-3 Pattern Sync loss (TX Pulse XCON, RX HI)
22104	"STM-0 AU-3 Bit Errors (TX Pulse = XCON, RX Pulse = HI)

SDH Tests A1T, [A1U], A3R	
No.	**Description**
22111	"STM-0 Signal Loss
22113	"STM-0 No offset - Frequency low
22114	"STM-0 No offset - Frequency high
22121	"STM-0 AU-3 Bulk TX, AU-3 Unfrm RX: Fail to get PSL
22122	"STM-0 AU-3 Bulk: Pattern Sync Loss
22131	"STM-0 TU-2 TX, AU-3 Unfrm RX : Fail to get PSL
22132	"STM-0 TU-2: Pattern Sync Loss
22141	"STM-0 DS-1 Unfrmd TX, AU-3 Unfrm RX: Fail to get PSL
22142	"STM-0 DS-1 Unfrmd: Pattern Sync Loss
22151	"STM-0 Frame or Pointer Sync Loss
22153	"STM-0 B1 BIP Errors low
22154	"STM-0 B1 BIP Errors high
22161	"STM-0 Frame or Pointer Sync Loss
22163	"STM-0 B2 BIP Errors low
22164	"STM-0 B2 BIP Errors high
22171	"STM-0 Frame or Pointer Sync Loss
22173	"STM-0 B3 BIP Errors low
22174	"STM-0 B3 BIP Errors high
22181	"STM-0 Frame or Pointer Sync Loss
22183	"STM-0 (M1) MS-REI Errors low
22184	"STM-0 (M1) MS-REI Errors high
22191	"STM-0 Frame or Pointer Sync Loss
22193	"STM-0 (Z5) AU-3 HP-IEC Errors low
22194	"STM-0 (Z5) AU-3 HP-IEC Errors high
22201	"STM-0 34M +100 ppm Pattern Sync loss
22203	"STM-0 34M +100 ppm Bit Errors low
22204	"STM-0 34M +100 ppm Bit Errors high
22211	"STM-0 34M -100 ppm Pattern Sync loss
22213	"STM-0 34M -100 ppm Bit Errors low
22214	"STM-0 34M -100 ppm Bit Errors high
22221	"STM-0 DS-3 +100 ppm Pattern Sync loss
22223	"STM-0 DS-3 +100 ppm Bit Errors low
22224	"STM-0 DS-3 +100 ppm Bit Errors high
22231	"STM-0 C-3 Bulk -100 ppm Pattern Sync loss
22233	"STM-0 C-3 Bulk -100 ppm Bit Errors low

SDH Tests A1T, [A1U], A3R	
No.	**Description**
22234	"STM-0 C-3 Bulk -100 ppm Bit Errors high
22251	STM-1 TU11 Async, Frame or Pointer Sync Loss
22264	STM-1 TU11 Async, B1 BIP Errors
22274	STM-1 TU11 Async, B2 BIP Errors
22284	STM-1 TU11 Async, B3 BIP Errors
22294	STM-1 TU11 Async, HP-REI Errors
22304	STM-1 TU11 Async, VC-11 V5 BIP Errors
22314	STM-1 TU11 Async, VC-11 V5 LP-REI Errors
22321	STM-1 Frame or Pointer Sync Loss
22323	STM-1 VC-11 V5 BIP Error Rate Low
22324	STM-1 VC-11 V5 BIP Error Rate High
22331	STM-1 Frame or Pointer Sync Loss
22333	STM-1 VC-11 V5 LP-REI Error Rate Low
22334	STM-1 VC-11 V5 LP-REI Error Rate High
22341	STM-1 TU11 Async, Pattern Sync Loss
22343	STM-1 TU11 Async, Bit Errors Low
22344	STM-1 TU11 Async, Bit Errors High
22351	STM-1 TU11 Background Pattern same as Test Pattern
22361	STM-1 TU11 Background Pattern Failure
22371	STM-1 TU11 Freq Off Ptr Mvts: Frame Sync Loss
22381	STM-1 TU11 Freq Off Ptr Mvts: Pointer Sync Loss
22394	STM-1 TU11 Freq Off Ptr Mvts: B1 BIP Errors
22404	STM-1 TU11 Freq Off Ptr Mvts: B2 BIP Errors
22414	STM-1 TU11 Freq Off Ptr Mvts: B3 BIP Errors
22424	STM-1 TU11 Freq Off Ptr Mvts: TU BIP Errors
22433	STM-1 TU11 Freq Off Ptr Mvts: +100 ppm, Imp VC Offset Low
22434	STM-1 TU11 Freq Off Ptr Mvts: +100 ppm, Imp VC Offset High
22443	STM-1 TU11 Freq Off Ptr Mvts: -100 ppm, Imp VC Offset Low
22444	STM-1 TU11 Freq Off Ptr Mvts: -100 ppm, Imp VC Offset High
22455	STM-1 Mixed TU3/TU11 TUG3#2 Background TU-11 shows TU-AIS
22456	STM-1 Mixed TU3/TU11 TUG3#2 Background TU-11 shows LP-RDI
22457	STM-1 Mixed TU3/TU11 TUG3#2 Background TU-11 shows TU-LOP
22461	STM-1 Mixed TU3/TU11 TUG3#1 Foreground TU-3 shows PSL
22471	STM-1 Mixed TU3/TU11 TUG3#3 Background TU-3 shows PSL
22485	STM-1 Mixed TU3/TU11 TUG3#1 Background TU-3 shows TU-AIS

SDH Tests A1T, [A1U], A3R	
No.	**Description**
22486	STM-1 Mixed TU3/TU11 TUG3#1 Background TU-3 shows LP-RDI
22487	STM-1 Mixed TU3/TU11 TUG3#1 Background TU-3 shows TU-LOP
22491	STM-1 Mixed TU3/TU11 TUG3#2 Foreground TU-11 shows PSL
22501	STM-1 Mixed TU3/TU11 TUG3#3 Background TU-11 shows PSL
22511	STM-1 TU-11 DS-1 F/G Patt: Unframed shows PSL
22512	STM-1 TU-11 DS-1 B/G Patt: Expected D4 framing shows PSL
22521	STM-1 TU-11 DS-1 F/G Patt: Expected ESF framing shows PSL
22522	STM-1 TU-11 DS-1 B/G Patt: Expected D4 framing shows PSL
22531	STM-1 AU-3 J1 message failure
22541	STM-1 TU-2 Pattern Sync loss
22543	STM-1 TU-2 Bit Errors low
22544	STM-1 TU-2 Bit Errors high
22551	STM-1 TU-12 Fl Byte Sync, Pattern Sync loss
22553	STM-1 TU-12 Fl Byte Sync, Bit Errors low
22554	STM-1 TU-12 Fl Byte Sync, Bit Errors high
22561	STM-1 TU-11 Pattern Sync loss
22563	STM-1 TU-11 Bit Errors low
22564	STM-1 TU-11 Bit Errors high
22571	STM-1 AU-3 34 Mb/s PRBS 23 Pattern Sync Loss
22573	STM-1 AU-3 34 Mb/s PRBS 23 Bit Errors Low
22574	STM-1 AU-3 34 Mb/s PRBS 23 Bit Errors High
22581	STM-1 AU-3 TU-2 Bulk PRBS 15 Pattern Sync Loss
22583	STM-1 AU-3 TU-2 Bulk PRBS 15 Bit Errors Low
22584	STM-1 AU-3 TU-2 Bulk PRBS 15 Bit Errors High
22591	STM-1 AU-3 TU-12 Fl Byte Word Pattern Sync Loss
22593	STM-1 AU-3 TU-12 Fl Byte Word Bit Errors Low
22594	STM-1 AU-3 TU-12 Fl Byte Word Bit Errors High
22601	STM-1 AU-3 TU-11 Async PRBS 9 Pattern Sync Loss
22603	STM-1 AU-3 TU-11 Async PRBS 9 Bit Errors Low
22604	STM-1 AU-3 TU-11 Async PRBS 9 Bit Errors High

Service Sheet G3 - Colour Display

Introduction

This Service Sheet should be used when troubleshooting faults associated with the instrument display after performing the preliminary troubleshooting described in General Service Sheet G-1.

Troubleshooting aims to isolate the fault to either the Display/Keypad Assembly, A3 Motherboard, A2 Front Panel Interface Assembly or the CPU Assembly.

Troubleshooting

1 If the display is blank after switch on, suspect the ribbon cable from A3 or A3 itself.

2 If the data displayed is in error garbled, suspect the display assembly or the CPU.

The Colour Display is an OEM Modular Assembly which contains no user-replaceable parts. If faulty it must be replaced. An Exchange Part is available-Refer to the Replaceable Parts Section and the Dismantling and Re-assembly procedures in this manual.

Service Sheet G4 - Power Supply

Introduction

This Service Sheet covers troubleshooting of the Line input through to the output of the Power Supply Module. The main sections are:

- Line Input, Filter and Protection
- Power Supply Module
- Fan and Low Voltage Supplies

If a problem is suspected on any of the above circuitry after performing the preliminary troubleshooting described in General Service Sheet G-1, then use the flowchart below to help isolate the fault.

WARNING **Take extra care when working on Power Supply Circuitry as hazardous voltages are present regardless of the ON/OFF switch setting.**

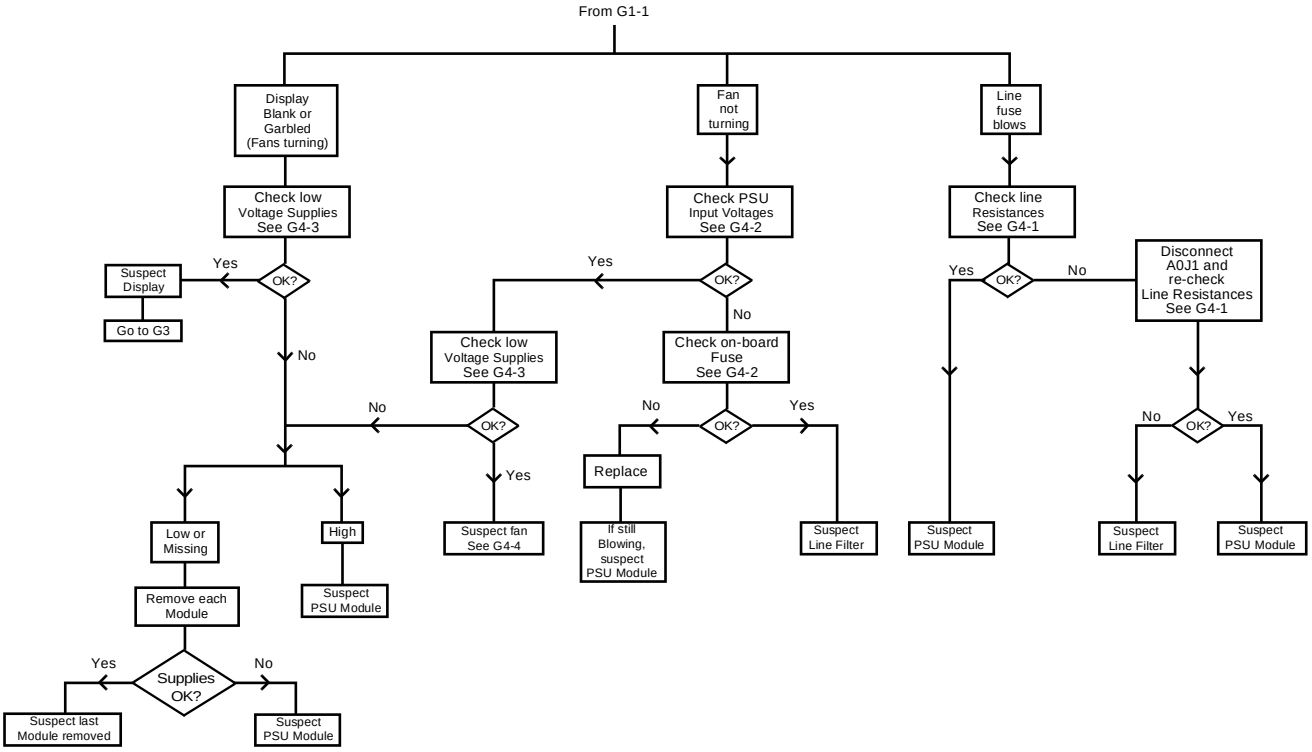


Figure 5-5 Power Supply Troubleshooting

Line (Mains) Fuse Blown

Carry out the following checks to isolate the cause of a continuously blowing Line Fuse.

Procedure	Troubleshooting
If F1 (Line fuse) is blown, remove the power cord and replace the line fuse. With the Instrument ON / OFF switch set to ON, check the following resistances using a DVM. Line to Ground: Open-Circuit. Neutral to Ground: Open-Circuit. Line to Neutral (L to N) : > 400 kΩ (after approximately 2 seconds).	If one or more of the resistance checks is low - Disconnect A0J1 and repeat the resistance checks. Resistances now OK - suspect the PSU Assembly. Resistance still low - suspect the Line Filter Assembly.

Power Supply Module Input Check

Carry out the following checks to ensure that the Power Supply Module is receiving the correct input supply voltage.

Procedure	Troubleshooting
Switch off the instrument and remove the power cord. Connect an AC Voltmeter across A0R40. Reconnect the power cord and switch on. Check for a voltage of 110 Volts or 240 Volts depending on the line supply in use.	Voltage OK-go to Low-voltage Supplies Check. Voltage low-check the on-board fuse. If not blown, suspect the Line Filter assembly. If the on-board fuse is blown replace then re-check the supply voltage as in step 1. If the fuse continues to blow, suspect the PSU Module.

Low-Voltage Supplies Check

Carry out the following checks to see if the internal instrument supplies are within their operating range.

Fans and Supplies

Carry out the following checks if the barrel fan is inoperative.

Procedure	Troubleshooting
1. Locate the low voltage test points on the motherboard. These are accessible through the left-side of the unit with the covers removed. Check the following voltages using a DVM. Ground one DVM lead on the chassis. **TEST POINT** **DC VOLTAGE** **PFD** +4.8 V +12 V +12 V +5 V +5 V **GND** 0 V -5.2 V -5.2 V -12 V -12 V -4.5 V -4.5 V	All Voltages O.K.-Power Supplies seem good. Any Voltage high-suspect PSU Assembly. Any Voltage low-remove each module in turn as described in the Dismantling and Re-assembly procedures. Re-measure the voltages after each module is removed. One or more voltage low with all modules removed -suspect the PSU Assembly or the Motherboard. Voltages OK if any module removed-suspect the last module removed-confirm as follows: Refit all modules except the “faulty” module Measure the voltages as before. If voltages now OK, the “faulty” module is faulty If voltages still low, suspect the PSU Assembly. (may be unable to supply enough current).

Procedure	Troubleshooting
1. Unplug the fan connector from its motherboard socket and measure the voltage across this socket. Typically **J2 Pins** **DC VOLTAGE** Across JI5 +12 V Barrel Fan	Voltage bad-Suspect the PSU Assembly or the Motherboard

Service Sheet G5 - Processor (CPU)

NOTE **If a processor is to be repaired or replaced, you must follow the correct procedure. Refer to Service Note 37717C-03 in Appendix B for information on how to do this.**

Introduction

This Service Sheet should be used when troubleshooting faults associated with the instrument Main Processor after performing the troubleshooting described in General Service Sheet G-1.

Troubleshooting aims to isolate the fault to either the CPU Assembly or the interfaces.

If a Fatal Error code and message are displayed and cannot be cleared by cycling power, re-initialize the NVM (see below), then if the Fatal Error is still present, use Fatal Error Table to decide the location of the fault.

If the CPU Selftest or Diagnostic Test fails, then use Disk Drive CPU Test Table to troubleshoot the fail code.

Upgrading the Firmware

NOTE The internal clock Time and Data will need to be set after upgrading the firmware. See Service Note 37717C-01A.

Refer to the Replaceable Parts Section and order the appropriate set of disks.

1 Power on the instrument and check for a valid display.

2 Press OTHER key, then MORE softkey then select the cal function.

3 Select CALIBRATION PASSWORD and using the DECREASE DIGIT and INCREASE DIGIT softkeys set the password to [1243].

4 Select CALIBRATION ITEM: [FIRMWARE UPGRADE].

5 Fit Disk 1 (from the set of disks) into the disk drive slot with the disk label facing towards the instrument Front Panel.

NOTE The Disk-Drive slot is at the right-side of the instrument, forward of the line ON/OFF switch.

6 Answer each question displayed on the screen using the appropriate keys. When you have answered all the questions, the instrument will commence downloading data from Disk 1. This process will take from 5-10 minutes.

NOTE Select <**Program**> when asked if you want to verify the disks. Verification is **not** required.

When data transfer from Disk 1 is complete, the display will show:

Inset next disk & press any key.

Use <single error key> to abort update.

7 Repeat steps 5 to 7 with the other disks supplied in the set.

When data transfer from the last disk is complete, the display will show:

To use new code press any key.

Use <single error key> to abort update.

8 Press the TRANSMIT key to initialize the instrument.

9 After initialization, press the TRANSMIT key again to restart the instrument.

The firmware upgrade is now complete.

CAUTION Resetting the NVM RAMS will also remove all user-defined stored settings and measurement results data. If this data is required by the customer, it will be downloaded to another storage device or tabulated for future re-entry into the instrument NVM.

NOTE The internal clock Time and Data will need to be set after NVM initiation.
See Service Note 37717C-01B.

Procedure

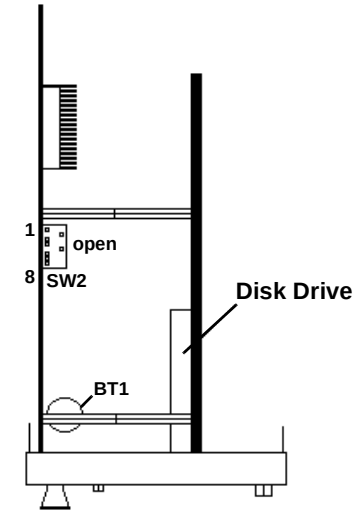
1 Switch off the instrument and disconnect the power cord.

2 Remove the rear panel feet.

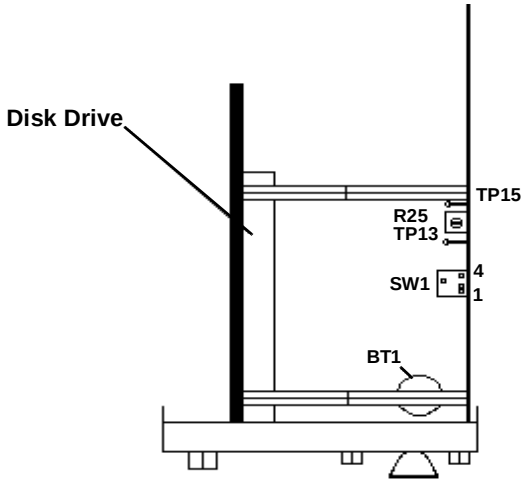
3 If Optical Modules are fitted, unscrew the optical shield from each input and output connector.

4 Withdraw the outer cabinet sleeve back and out of the instrument.

5 Looking down on the instrument, locate the 8-bit DIL switch SW2 on the CPU module (this is the module nearest the rear of the instrument). This switch is visible through a slot in the instrument metalwork.

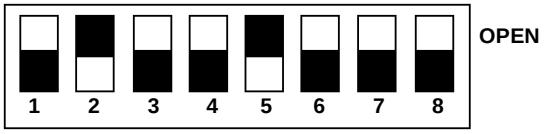


CPU Disk Module (top view)

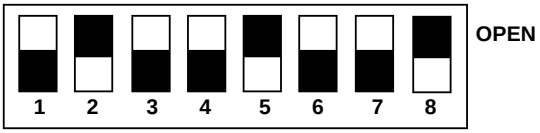


CPU Disk Module (bottom view)

The switch will be set as follows:



1 With the instrument OFF change the settings on the switch as below:



2 Power on the instrument and check for a COLD START message on the display.

3 Hit any key to restart the instrument.

4 Switch the instrument OFF and return the DIL Switch to the original settings (see above).

5 Power on the instrument and check to see if the fault condition has been removed.

6 Replace the instrument metal work as a reversal of the above procedure.

7 Obtain a pass on all instrument Selftests.

8 The instrument is now ready for use.

Replacing the Disk Drive

1. Place the CPU on the bench.
2. Remove the Disk-Drive RFI shield by unscrewing the four posidrive screws which secure it to the board standoffs.
3. The RFI shield can now be lifted off once the HP-IB ribbon cable (A28J3) is unplugged.
4. Remove the Disk-Drive by unscrewing the nut which secures it to the rear of the CPU Front Panel.
5. The Disk-drive can now be lifted off and placed to one side in an anti-static bag after unplugging A28J7.

NOTE Before replacing the Disk-Drive it is prudent to check the battery voltage (BT1) to see if it needs to be replaced.

6. Fit new Disk-Drive by performing a reversal of the removal procedure.

Checking and Replacing the Non-Volatile-Memory (NVM) Battery.

The NVM battery is a non-rechargeable item so will need to be replaced when the voltage falls below the minimum required to maintain memory content. The typical life of this battery should be between 3 and 5 years depending on instrument use.

To decide if this battery requires replacement, power the instrument OFF then ON. If DEFAULT settings are assumed (see Appendix A) and the front panel displays a NVM message, then it is likely that the NVM battery requires replacement. Confirm this by measuring the voltage as described in the following procedure.

Procedure

1. Remove the Processor Module as described in the Module Removal and Replacement Procedure. (this is the module nearest the rear of the instrument).
2. Locate the NVM battery. This is marked BT1 and is located behind the Disk Drive on the CPU Module. Remove the 4 screws which holds the Disk Drive in place, and slip the assembly back to allow access to the battery BT1.
3. Check the NVM battery voltage using a DVM. It should be between 3.4 V and 3.8 V. If it is less than 3.4 V it should be replaced.
4. Remove the NVM Battery by carefully unsoldering the leads.

WARNING **Explosion may result if the terminals of this Lithium Battery are short-circuited.**

Always follow HP guidelines when disposing of lithium batteries. Never incinerate or puncture.

CAUTION All customer defined Stored Settings/Panels will be lost when the NVM Battery is removed. The instrument will adopt DEFAULT SETTINGS and perform COLD START when power is re-applied. Refer to the Operating Manual for more details.

NOTE The internal clock Time and Data will need to be set after NUM initiation. See Service Note 37717C-01B.

5 Solder a new NVM Battery into the CPU Assembly (see Replaceable Parts List for the battery part number).

6 Once the new battery is fitted, replace the processor module and all other modules in the correct sequence.

7 Power on the instrument and change the Transmitter Output Signal Rate to 2 Mb/s.

8 Switch off the instrument.

9 Switch on the instrument and check there is no COLD START message and the Transmitter Output Signal Rate is still set to 2 Mb/s.

10 Replace the outer cabinet sleeve, optical module shields and the rear panel feet-this is a reversal of the removal procedure.

Fatal Errors

Table 5-1 Fatal Error Table

No.	Description	No.	Description
1	"Error in EEPROM id"	2	"Error in function parameter"
3	"Error in ASIC read/write"	4	"Coldstart forced by user"
5	"Meas system overruns sampling period"	6	"Meas system loop time excessive"
7	"Corrupted LCA data"	8	"LCAs failed to initialize"
9	"LCA not getting prog command"	10	"LCA not holding prog low"
11	"LCA short program cycle"	12	"LCA program failed"
13	"POH ram timeout"	14	"Error in comms to ODL uP"
15	"ODL Dpram failed"	16	"Error in ODL code checksum"
17	"Error in ODL uP boot"	18	"Error in ODL-no ASIC clock"
19	"TU ASIC write fail"	20	"CMOS GA busy reading Tx Clk count"
21	"switch_in_vcxo: invalid VCXO index"	22	"switch_in_vcxo: VCXO not loaded"
23	"turn_on_vcxo: VCXO not loaded"	24	"turn_off_vcxo: VCXO not loaded"
25	"invalid ECL input"	26	"ppm out of range"
27	"VCXO unsTable when moving"	28	"VCXO unsTable when steady"
29	"VCXO control DAC out of range"	30	"UPDH: LCA(no program)"
31	"UPDH: LCA(prog. line not held low)"	32	"UPDH: LCA(short program)"
33	"UPDH: LCA(program fail)"	34	"ATM Tx ram timeout"
199	"Meas system overruns sampling period"	220	"Too many lines in port address Table"
221	"Too many images for image Table"	222	"Too few images, hence RAM wasted"
223	"Error in port address Table"	224	"Update address not in image Table"
225	"Unidentified opcode (func bio_update)"	226	"Reference/access to word at odd address"
		300	"Unable to create exchange control block"

Table 5-1 Fatal Error Table

No.	Description	No.	Description
301	"pSOS primitive REQ_X failed"	302	"pSOS primitive SEND_X failed"
303	"pSOS primitive ATTACH_X failed"	304	"pSOS primitive LIBER_X failed"
305	"Attempted to Join a region twice"	306	Attempted to Leave an unowned region"
307	Bad process number in Create_process"	308	"Unable to create process"
309	"Bad process number in Create_process"	310	"Unable to suspend process"
311	"Unable to resume process"	312	"Unable to change priority"
313	"Process user stack underflow"	314	"Process user stack overflow"
315	"Process spvsr stack underflow"	316	"Process spvsr stack overflow"
317	"System supervisor stack overflow"	318	"Unable to delete process"
319	"Semaphore exceeds max value"	320	"Unsynchronized display access"
322	"Unsynchronized logging access"	323	"Attempted join breaks order rules" 321 ,"ACRTC command error"
350	"Root process exits"	400	"Logging queue excessed"
401	"Logging queue underrun"	407	"Error in 'log_starts'"
408	"Error in 'log_Table'"	409	"Unknown CALL(A) code"
410	"Error in graph command string"	411	"Cannot run the plot x value backwards!"
412	"Unknown token on logging output queue!"	420	"Unknown graph y axis type"
421	"Word register number out of range"	422	"Word register command, syntax error"
423	"Unknown graph x axis type"	450	"Unable to create SCPI status handler"
451	"Unable to create SCPI device driver"	452	"Unable to create SCPI macro handler"
453	"SCPI parser terminated"	500	"Real time clock failed"
501	"Internal Printer failure"	600	"Unrecognized cmd received from 8031"
601	"Attempted to send unknown cmd to 8031"	602	"Protocol failure"
603	"Bad response from 8031"	604	"MPIF ready timeout"
605	"MPIF key protocol failure"	606	"MPIF PB0 protocol failure"
607	"MPIF PB1 protocol failure"	608	"MPIF RST protocol failure"
609	"MPIF CMD protocol failure"	610	"MPIF STX protocol failure"
611	"MPIF MCT protocol failure"	700	"ROM ID mismatch"
701	"ROM 1 number incorrect" }	702	"ROM 2 number incorrect" }
703	"ROM datecodes disagree" }	704	"No Power-fail interrupt at power-down" }
705	"RAM content corrupt during power-down" }	706	"RAM failed read/write test" }
707	"Firmware changed?" }	708	"Unknown SA test selected"
709	"Unable to correct EEPROM location"	710	"Timed out waiting for EEPROM"

Table 5-1 Fatal Error Table

No.	Description	No.	Description
711	"Unable to initialise EEPROM"	712	"Saved EEPROM address illegal"
713	"Unable to clear EEPROM pfail flag"	750	"BUS ERROR exception"
751	"Address error"	752	"Illegal instruction"
753	"Divide-by-zero"	754	"CHK instruction trap"
755	"TRAPV instruction trap"	756	"Privilege violation"
757	"Trace trap"	758	"Line 101X Emulator trap"
759	"Uninitialized vector"	760	"Spurious interrupt"
761	"Unknown floating-point trap"	762	"Floating-point precision loss"
763	"Inexact floating-point result"	764	"Floating-point divide-by-0"
765	"Floating-point underflow"	766	"Floating-point overflow"
767	"Floating-point operator error"	768	"Floating-point NaN signalled"
770	"Spurious DUART interrupt"	780	"No DTACK from EEPROM"
781	"No DTACK from DPRAM"	782	"No DTACK from DUART"
783	"No DTACK from Real-time clock"	784	"No DTACK from HPIB"
785	"No DTACK from CRT controller"	786	"No DTACK from option switch"
787	"No DTACK from timer ack"	788	"No DTACK from RAM @ FEXXXX"
789	"No DTACK from RAM @ FFXXXX"	800	"Subtest-return value out of range" }
801	"Subtest-nonexistent CARE parameter" }	802	"Subtest-CARE message no. layer error" }
850	"SMG result queue full"	851	"SMG result queue empty"
852	"SMG command queue full"	853	"SMG command queue empty"
854	"Unknown SMG command"	855	"Illegal SMG sample period selected"
861	"Unable to create SCPI Printer driver"	862	Illegal free var type"
863	"Xpanel mask out of range"	864	"No evoke fn to call"
890	"sel var stacking queue size has been exceeded"		

Table 5-2 Disk-Drive CPU Tests

Sub Test Number	Test Description	Fail Codes	Action
1	FEPROM	1,010	Check firmware revision is valid
2	SRAM	1020-1024	Suspect CPU assembly
4	RS232 Port	1040-1047	Check RS232 Loopback is fitted
5	HPIB Port	1,052	Suspect CPU assembly
6	Real Time Clock	1060-1061	Suspect CPU assembly
7	Parallel Port	1,070	Check firmware revision is A.00.99 and above, if not firmware update needed.
8	(F.P.) Printer	1080-1083	Perform Printer troubleshooting
10	Disk-Drive I/F	1110-1104	Check formatted disk is inserted, otherwise suspect disk drive
11	LAN I/F	1110-1113	Check firmware revision is A.00.99 and above, if not firmware update is needed

CPU Tests

Detail Description

Subtest 1 - FEPROM test

This subtest checks the processor card FEPROM area, **this test is executed regardless of the equipment options and current setup**.

The unit under test is set to the default state and then tested as follows, the test is interruptible by power fail.

A CRC check over the VxWorks FEPROM code area is performed.

Note no CRC check of the data area is performed, a CRC check over the main code may be added at a later date.

Subtest 2 - SRAM test

This subtest checks the processor card ISS SRAM area, **this test is executed regardless of the equipment options and current setup**.

The unit under test is set to the default state and then tested as follows, the test is not interruptible by power fail. This test does not test all of the SRAM area present on the processor board.

ISS area check : from the start address until the end address each long word is tested by saving the original data, writing and reading each of the defined test words, restoring the original test data.

Test pattern

MS-Word	LS-Word	Save original data write and read test
0000	0000	data in sequence as specified, then
FFFF	FFFF	restore original data.
5555	5555	
AAAA	AAAA	

Address line check : once the SRAM data area has been successfully tested a SRAM address line test is performed.

Subtest 4 - User RS232C serial Port

This subtest checks the processor card 'user' RS232C interface. **The test is only executed if option A3B or A3D is fitted and RS232C is not selected for VRM, DNA or REMOTE port.**

The unit under test is set to the default state and then tested as follows, the test is interruptible by power fail. If the equipment is operating under the control of Virtual Remote this test is not performed.

A loop back is fitted to the serial port and the RS232C interface is tested as follows, during the test the VxWorks high level driver Tx/Rx is switched off.

DTR/RTS are looped back to RI,DCD/DSR, CTS for this test

Tx/Rx Check : The UART Tx/Rx is configured as follows, the test message is transmitted and the received message is checked.

Baud rate = 9600, stop bits = 1, parity = none and data bits = 8, UART software 'Interrupt' mode.

Subtest 5 - HPIB Port

This subtest checks the processor card HPIB interface. **The test is only executed if option A3B or A3D is fitted and HPIB is not selected for REMOTE port.**

The unit under test is set to the default state and then tested as follows, the test is interruptible by power fail. If the SCPI interface is in use this test is not performed.

Tx-Rx transmit check : the text string "The quick brown fox jumps over the lazy dog" is transmitted one character at a time, after each character is transmitted the state of the output lines is read in order to ensure that the character has been written.

Subtest 6 - Real Time Clock test

This subtest checks the processor card real time clock, **this test is executed regardless of the equipment options and current setup**.

The unit under test is set to the default state and then tested as follows, the test is not interruptible by power fail.

Register read/write check : the current time is saved and then the clock is set to 23:59:59 on the 31/12/99 and the time is read back to ensure the internal registers have been correctly written.

Register 'roll over' check : a time of greater than 1 second is allowed to pass and then the clock is checked to ensure that the time and date has 'rolled over' to 00:00:00 on 1/1/20.

Subtest 7 - Parallel Port

This subtest checks the processor card Parallel interface, **this test is never executed during normal selftest**, it is executed during 'Hidden Screen' factory selftest.

The unit under test is set to the default state and then tested as follows, the test is interruptible by power fail.

The following test string is transmitted twice to the device connected to the Parallel port:

"abc_def ghi_jkl mno_pqr stu_vwx_yz !@#$%^&*()_+="

Note : attached device must be ready and able to accept the data being transmitted or error 1070 will occur.

Subtest 10 - Floppy Disk Interface

This subtest checks the processor card floppy Disk interface and drive, **this test is executed regardless of the equipment options and current setup**.

The unit under test is set to the default state and then tested as follows, the test is not interruptible by power fail.

Disk check : selftest will first check that a floppy Disk is inserted into the drive.

Write File : a test file is written to the disk.

Read File : the test file is read from the Disk.

Check file data : the read data is compared to the write data.

Read File : the test file is read from the disk.

Check file data : the read data is compared to the write data.

NOTE If Disk-Drive is faulty use the procedure on Page 5-100 to replace the Disk-drive.

Replacing the CPU Assembly

Refer to Service Note 37717-07 for the correct procedure to replace a faulty CPU Assembly.

Subtest 11 - LAN 10Base - T Interface

This subtest checks the processor card LAN interface if fitted. **The test is only executed if option A3B is fitted and LAN is not selected for DNA port.**

The unit under test is set to the default state and then tested as follows, the test is interruptible by power fail.

Results of the 'Power on' LAN selftest functions are requested from the LAN controller functions.

Service Sheet G6 - Front Panel LEDS

Introduction

This Service Sheet should be used when troubleshooting faults on the Front Panel Leds after performing the troubleshooting described in General Service Sheet G-1. A fault on this assembly will normally be indicated as a Front Panel Leds Diagnostic test failure.

Running Front Panel LEDS Diagnostic Test

1. Display the Other Test Features Page by simultaneously pressing [SINGLE] and the 4th softkey from the left below the Front Panel display.
2. To start testing, select LED TEST. The test will automatically light each LED in sequence, so the operator must look for an unlit LED during this sequence. The sequence is continuously repeated.
3. To stop the test, press ABORT TEST softkey. The test will stop at the end of the current sequence and the display will return to the Other Test Features page.
4. Press EXIT softkey to return to normal operation.

Front Panel LEDS Troubleshooting

The procedure depends on whether the failure is one LED or more than one (multiple) LEDs.

Only one LED failing

Procedure	Troubleshooting
1. Connect the Oscilloscope between the cathode (marked with a square pad) of the LED which is not lighting, and ground.	
2. Run the LED test Sequence as described above. The cathode should be at +5 volts when the LED is unlit and pulse low when the LED is expected to be lit.	Voltage and Pulses as expected-suspect the LED itself-it may be replaced (part number is in Replaceable Parts section). Voltage and Pulses incorrect-suspect A1 Assembly.

Multiple LEDS failing

Suspect the A1 Assembly.

Service Sheet G7 - Front Panel Membrane Keyboard

Introduction

This Service Sheet should be used when troubleshooting faults on the Front Panel Membrane Keyboard after performing the troubleshooting described in General Service Sheet G-1.

A fault on this assembly will normally be indicated as a Keyboard Diagnostic test failure when running this test.

Running the Keyboard Diagnostic Test

1. Display the Keyboard Test Page by simultaneously pressing [SINGLE] and the 3rd softkey from the left below the Front Panel display.
2. Press each front panel key once to check operation. When the key is pressed, the display will show the key function in the Last Key Pressed field, so the operator must look for an incorrect description in this field.
3. To stop the test, press the same key twice. The instrument will return to normal operation.

Keyboard Operation

The Front Panel keyboard membrane is arranged in a 7 Column by 5 Row matrix. When a key is pressed, a circuit connection is made between the appropriate Column and Row lines.

When the keyboard is not being used, the Main CPU pulses the Column lines to TTL lows approximately every 7 ms. The Row lines normally sit high and are read by the Main CPU approximately every 7 ms. When a key is pressed, a low is passed through the key connection from the Column line to the appropriate Row line.

The change in row line status gives the Main CPU Row line identification, and initiates a verification procedure to identify the Column line associated with the pressed key. Column lines are driven low in turn and the appropriate Column line data is returned the CPU via the corresponding Row line thus identifying the Column.

Keyboard Troubleshooting

Procedure	**Troubleshooting**
1. One key only failing.	Suspect the Membrane Keypad or A1 Assembly (see Note below).
2. Multiple keys failing.	Suspect A2.

NOTE The Membrane Keypad can be replaced only as an integral part of the Front Panel Assembly. It must be ordered for replacement using only the part number designated for Front Panel Keyboard Display Assembly given in the Replaceable Parts Section of this Manual.

Service Sheet G8 - Printer

Before checking the Printer, go to the OPTIONS page on the 37717C and ensure option UKX is enabled. There are no serviceable parts inside the lid Printer. If the Printer is suspected to be faulty, it must be replaced as a unit (part number 37717-60095).

1. With the HP 37717C powered down, connect the UKX Printer (ensure a roll of paper is fitted) and power up the HP 37717C.
2. Press the OTHER key then the PRINTER softkey.
3. Select the PRINTER field on the display and set to internal.
4. Select the PRINTING field in the display and set to ON.
5. Lift the tabs at either end of the Printer mechanism cover and note the three LEDS on the left hand side of the Printer mechanism.
6. The left most and rightmost LEDs should be ON (the center LED may be on or off or flashing).
7. If the leftmost LED is flashing this may be due to Print head overheating due to a paper jam. Clear the jam and the print head and proceed to step 5.
8. With the internal Printer selected on the HP 37717C, LOG ON DEMAND may be set to SCREEN DUMP. Pressing PRINT NOW will cause the screen contents to be printed.
9. If the head has been cleaned and no printout appears then suspect the Printer.

Service Sheet G9 - Unstructured PDH Module

Introduction

This Service Sheet should be used when troubleshooting faults associated with the instrument Unstructured PDH Module after performing the troubleshooting described in General Service Sheet G-1. A faulty PDH Module will normally be indicated as a PDH Selftest failure when running the instrument selftest.

Troubleshooting PDH Selftest failure

The following troubleshooting aims to isolate the fault to either the PDH Transmit Board Assembly or the PDH Receive Board Assembly. When the faulty board assembly has been located it should be replaced using the Replacement Procedures (section G15 in this Manual). The correct part to order will be found in the Replaceable Parts section in this Manual.

NOTE Board Assemblies in this module contain on-board protection fuses. Before replacing a defective board assembly, test all on-board fuses using an ohmmeter. If any fuse is blown it may be replaced using the part number from the Replaceable Parts Section in this Manual. After replacement, rerun the selftest to verify repair. On-board fuses are identified as in-line, two-wire, through-hole types normally colored green and approximately 7 mm x 2 mm diameter. The rating is stamped on the fuse body.

Troubleshooting Procedure

If the PDH Selftest fails, use the following procedure and accompanying selftest information to troubleshoot the fail code.

1. Check that the PDH 75Ω Tx and Rx ports are looped using a suiTable BNC/BNC cable.
2. Check that the PDH 120Ω Tx and Rx ports are looped using a suiTable 3-pin Siemens/3-pin Siemens cable.
3. **If the Failcode indicates No Signal**, check the PDH Transmitter output at the appropriate bit rate on an oscilloscope (a procedure is given in the Performance Tests section of the Calibration Manual).
   If the PDH Transmitter output signal is OK, then suspect the PDH Receiver Assembly.
   If the PDH Transmitter output signal is NOT OK, then suspect the PDH Transmitter Assembly.
4. **If the failcode indicates No Pattern Sync,** perform the Recovered Clock adjustment at the failing bit rate (see Adjustments Section of this Manual) and re-run the selftest.
5. If the selftest still fails, setup another HP 37717C or equivalent Unstructured PDH Transmitter to the same Transmit Parameters as were frozen at selftest failure (see G2) and connect the PDH transmitter of this instrument to the PDH Receiver of the faulty unit.
6. Setup the Receiver parameters of the faulty unit to be the same as those in the subtest which fails (see the descriptions which follow).
7. Check to see if the **No Pattern Sync** indication is still present.
8. If the **No Pattern Sync** indication is still present, suspect the PDH Receiver Assembly.
9. If the **No Pattern Sync** indication is no longer present, suspect the PDH Transmitter Assembly.
10. **If the failcode indicates Incorrect Errors Counted** perform the Recovered Clock

adjustment at the failing bit rate (see Adjustments Section of this Manual) and re-run the selftest.

11 If the selftest still fails, setup another HP 37717C or equivalent Unstructured PDH Transmitter to the same Transmit Parameters as were frozen at selftest failure (see G4) and connect the PDH transmitter of this instrument to the PDH Receiver of the faulty unit.

12 Setup the Receiver parameters of the faulty unit to be the same as those in the subtest which fails (see the descriptions which follow).

13 Start and run an error measurement for the required time.

14 Check the Error Count on the HP 37717C Results page when the measurement ends:
If the Error Result is high or low, suspect the PDH Receiver Assembly.
If the Error Result is now OK, suspect the PDH Transmitter Assembly.

PDH Tests

Subtest Number Range	Test Name	Number of Subtests
1-10	Unbal 75Ω	10
11-12	Bal 120Ω	2
13-23	Data Rate	11
24-26	Error inject	3
27-31	Clock recovery	5
32-36	FAS	5

Subtests 1 to 10 : Patterns Test

The Receiver is first checked to have a signal present, then Pattern Sync is checked. For each of the settings below the bit error count is measured, and checked to be zero.

Subtests 11 to 12 : Balanced Interface Tests

First check Receiver signal present, then sync, then count bit errors. Count should be zero.

Subtests 13 to 23: Data rate tests (Receiver frequency measurement)

For each of the Transmitter frequency settings, the receiver is used to measure absolute frequency. Any selftest failure is reported as per normal with a corresponding error number. Receiver frequency limits are calculated as, the nominal frequency (including any Tx offset) ±3 ppm. In all cases the test pattern used is PRBS(23) and results are given in Hz.

Subtests 24 to 26 : Error Inject Tests

The receiver is used to measure bit errors over a 5 second gating period for each of the settings listed. In the case of subtest 2, 5 single errors are injected during gating.

Subtests 27 to 31 : Clock Recovery Tests

For each of the following receiver rates the free running clock recovery frequency is measured and compared against corresponding limits. Each measurement is taken as an offset in ppm from the standard rate. Test failure results in generation of an error code in the normal way.

Subtests 32 to 36 : FAS Tests

Setup

- In-Service
- Ternary
- Internal Clock
- No Clock Offset
- Unbalanced
- External Loopback

Subtest 32

Write value (0xFF) to FAS register and check it is read back correctly. Clear bus with a write to dummy address between writing to and reading from the FAS register.

Error code 2326

Subtest 33

Set Tx pattern to look like FAS word and check that at 2 Mb/s the LCA does not lock. The LCA should only lock if it gets FAS, NFAS, FAS-this cannot be setup by the user word at 2 Mb/s.

Error codes

No Signal 2330

LCA Not Locked 2335

Subtests 34-36

Check that the LCA can lock onto a FAS word.

Wait 2 seconds then recheck that no further errors, slips or loss of sync have occurred.

Check that the LCA will not lock onto a non-FAS word.

Service Sheet G10 - Structured PDH Modules and ATM

Introduction

Separate Transmit and Receive Modules are used to provide Structured PDH functionality.

This Service Sheet should be used when troubleshooting faults associated with either of these modules after performing the troubleshooting described in General Service Sheet G-1. A faulty Structured PDH Module will normally be indicated as a SPDH Selftest failure when running the instrument selftest.

Troubleshooting SPDH Selftest failure

The following troubleshooting aims to isolate the fault to either the A17 Transmit Board on the SPDH Transmitter Module or the A16 Receive Board Assembly on the SPDH Receiver Module. Once the faulty board assembly has been located it should be replaced using the Replacement Procedures section in this manual. The correct part to order will be found in the Replaceable Parts section in this manual.

NOTE Board Assemblies in this module contain on-board protection fuses. Before replacing a defective board assembly, test all on-board fuses using an ohmmeter. If any fuse is blown it may be replaced using the part number from the Replaceable Parts Section in this manual. After replacement, rerun the selftest to verify repair. The on-board fuses are identified as in-line, two-wire, through-hole types normally colored green and approximately 7 mm x 2 mm diameter. The rating is stamped on the fuse body.

Troubleshooting Procedure

If the SPDH Selftest fails, use the following procedure and accompanying selftest information to troubleshoot the fail code.

1. Connect the SPDH 75Ω Tx and Rx ports are looped using a suiTable BNC/BNC cable.
2. Check that the SPDH 120Ω Tx and Rx ports are looped using a suiTable 3-pin Siemens to 3-pin Siemens cable. Connect the MUX to the DEMUX port if applicable.
3. If the Failcode indicates No Signal then check the SPDH Transmitter output at the appropriate bit rate on an Oscilloscope (a procedure is given in the Performance Tests section of the Calibration Manual).
   If the SPDH Transmitter output signal is OK, then suspect the SPDH Receiver Assembly.
   If the SPDH Transmitter output signal is NOT OK, then suspect the SPDH Transmitter Assembly.
4. If the failcode indicates No Pattern Sync, perform the Recovered Clock adjustment at the failing bit rate (see Adjustments Section of this Manual) and re-run the selftest.
5. If the selftest still fails, setup another HP 37714/17A/B or equivalent structured PDH Transmitter to the same Transmit Parameters as were frozen at selftest failure (see G2) and connect the SPDH transmitter of this instrument to the SPDH Receiver of the faulty unit.
6. Setup the Receiver parameters of the faulty unit to be the same as those in the subtest which fails (see the descriptions which follow).

7 Check to see if the No Pattern Sync indication is still present.
If No Pattern Sync indication is still present, suspect the SPDH Receiver Assembly.
If No Pattern Sync indication is no longer present, suspect the SPDH Transmitter Assembly.

8 If the failcode indicates Incorrect Errors Counted perform the Recovered Clock adjustment at the failing bit rate (see Adjustments Section of this Manual) and re-run the selftest.

9 If the selftest still fails, setup another HP 37714/17A/B or equivalent structured PDH Transmitter to the same Transmit Parameters as were frozen at selftest failure (see G2) and connect the SPDH transmitter of this instrument to the SPDH Receiver of the faulty unit.

10 Setup the Receiver parameters of the faulty unit to be the same as those in the subtest which fails (see the descriptions which follow).

11 Start and run an error measurement for the required time.

12 Check the Error Count on the HP 37717C Results page when the measurement ends:
If the Error Result is high or low, suspect the SPDH Receiver Assembly.
If the Error Result is now OK, suspect the SPDH Transmitter Assembly.

SPDH Test

Subtest Number Range	Test Name	Number Of Subtests	Test Time (Seconds)
1-7	Line Code (Unbalanced 75Ω)	7	23
8-9	Line Code (Balanced 120Ω)	2	6
10-21	Frequency Offset	12	245
22-36	Error Add	15	16
37-44	Framing	8	8
45-53	Structured Payloads	9	20
54-63	Patterns	10	17
64	Drop and Insert	1	10
65-72	Round Trip Delay	8	18
83-86	Line Code (Unb 75Ω)	4	
87-88	Line Code (110Ω)	2	
89-94	Frequency Offset	6	
95-112	Error Add	18	
113-120	Framing	8	
121-130	Structured Payloads	10	
131-140	Patterns	10	
141	Drop/Insert	1	
142-145	Round Trip Delay	4	

Overall Connections

- TX Unbalanced Data To RX Unbalanced Data
- TX balanced Data To RX balanced Data
- TX Insert 2 Mb/s Data to RX Drop 2 Mb/s Data.

Estimated Overall Test Time: 375 seconds (6.25 minutes)

The test method attempts to minimize test time by not insisting that the transmitter VCXO has settled. If the test results pass prior to the VCXO settling, then the test completes (passed) and the next test begins. A test fails when a length of time passes within which the VCXO ought to have settled and the test results are still in a failed state.

NOTE 140M and 8M tests are not run when 110 PDH Module is fitted.

Line Code (Unbalanced 75Ω)

All line rate and line code settings are configured and the receiver is checked for zero errors. The Loss Of Signal and Pattern Sync Loss alarms are measured and then pattern errors are measured for each of the test points. Both alarms must be off and the pattern errors must be zero otherwise an error will be reported. The instrument is gated for 2 seconds at each test point.

Line Code (balanced 120Ω)

All line codes are selected for a sample of two line rates and the receiver is checked for zero errors. The Loss Of Signal and Pattern Sync Loss alarms are measured and then pattern errors are measured for each of the test points. Both alarms must be off and the pattern errors must be zero otherwise an error will be reported. The instrument is gated for 2 seconds at each test point

Frequency Offset

For each line rate the transmitter is configured for 0, +100 and -100 ppm offset and the receiver is used to measure the actual frequency. The measured frequency must be accurate to ± 3 ppm. The measurement is only made when the transmitter VCXO has settled. In all subtests the pattern is configured to PRBS23 (INV).

Error Add

All error types (Code, FAS and BIT) are checked in two modes: framed 34M; and 34M structured to 2M PCM30. The error add is set to OFF, SINGLE and 1.0E-3 rate for each setting and the receiver gates for 3 seconds and the error count is measured. The pattern is fixed at PRBS23 (INV) and the line code at HDB3.

Framing

The ability to frame to and lose frame is checked at 140M and 2M. All multiframe types are also checked at the 2M rate. The error code for LOF/LOM is reported if LOF/LOM is asserted when expecting a framed signal. It is also reported if LOF/LOM is not asserted when applying an unframed signal to a framed receiver. In drop 2 Mb/s mode the LOF/LOM alarms are checked and should be off.

Structured Payloads

Pattern sync and pattern errors are checked for each test point using the default pattern. The instrument is gated for 2 seconds at each test point.

Patterns

Pattern sync and pattern errors are checked for each test point. The signal is unframed in all test points. The instrument is gated for 2 seconds at each test point.

Drop/Insert

A 2 Mb/s signal is inserted into channel 1 of an 8M transmit signal. The receiver is configured to drop channel 2 (a transmit background channel) and the drop port is connect to the insert port. The transmit justifier is forced to apply a fixed stuffing ratio. The insert and drop port settled status bits are monitored and errors reported as follows.

Round Trip Delay

The TX and RX are set to 64 kb/s mode and simulated delays of 0 sec and 2 sec are introduced and measured. This is repeated for all setup delay paths.

Binary Interface Tests

NOTE Only run when UH3 PDH Binary Interface Module is fitted.

Setup

Binary TX Clock Out to Binary RX Clock In.
Binary TX Data Out to Binary RX Data In.

Subtests 73-82 For each test the bit count is measured and checked that it is within the test limits.

Line Code (Unbalanced 75Ω)

NOTE Only run when option 110 PDH Module is fitted.

All line rate and line code settings are configured and the receiver is checked for zero errors. The Loss of Signal and Pattern Sync Loss alarms are measured and then pattern errors are measured for each of the test points. Both alarms must be off and the pattern errors must be zero otherwise an error will be reported. The instrument is gated for 2 seconds at each test point

ATM Tests

Subtest Number Range	Test Name	Number Of Subtests	Test Time (Seconds)
1 to 14	Alarms	14	185
15 to 25	Bandwidth	11	95
26 to 28	Distribution	3	25
29 to 42	Error Add	20	210
43 to 64	Headers	24	130
65 to 71	Payloads	7	60
72 to 88	Test Cell	15	165
89	Trail Trace	1	45
90 to 99	Perf. Man. OAM	4	110

Overall Connections

- TX Unbalanced Data To RX Unbalanced Data.
- TX balanced Data To RX balanced Data.
- TX Insert 2 Mb/s Data to RX Drop 2 Mb/s Data.

Estimated Overall Test Time: 1025 seconds (17 mins 5 seconds)

The tests run in this section are identical to those run as test 15 in some firmware revisions. When the tests are run as Test 15, the error codes are displayed as 15xxx rather than 12xxx.

Alarms

The instrument is set up to a 2M signal with F/G bandwidth set to 4,528 cells/sec (100%). All the F/G Header selection is set to 0 in UNI mode (except VCI equals 32) and a payload selection of 2^15-1 Cross Cell. Each of the alarms is tested for its active and non-active state and the appropriate error condition is reported. Alarms are not a transmit function in this module. The instrument changes Tx and Rx rates for every test except for physical layer alarm tests which are tested at 2M, 34M and 140M. The instrument is gated for 3 seconds at each test point.

LOC alarms are activated by setting the Tx cell stream to 100 cells/s on periodic burst mode (burst size of 2000 cells) giving one second of FG followed by 19 seconds of idle cells. After 4 seconds the LOC alarm is tested to have been activated. The appropriate CC stream is then activated and the alarm is tested to have been deactivated.

Bandwidth

Bandwidth can be measured via the received cell rate count. The F/G and 3 B/G headers are set up to be the same, i.e. all values set to 0 except for the GFC values which are set to 1,2,3 and 4 consecutively. These values have been chosen since the fill will be set to Idle which has a GFC value of 0. These values will be used at the receiver to set the filter to select F/G or B/G cell streams. Signal is fixed at 34M with a F/G payload of User Word 55H and background payloads of 01H, 02H and 03H respectively. Fill cells are set to Idle (default). Distribution is set to Periodic. The instrument is gated for 3 seconds at each test point and the receive cell count value checked.

Distribution

The instrument is set up to default settings of 34M and a payload of Cross-Cell 2^15-1 PRBS. Distribution choice only applies to the F/G selection (B/G are always Periodic). B/G bandwidths are set to 0% and the Fill cells set to Idle (identifiable by Header values set to all zeros except for CLP which is set to 1). F/G header is set to default values and a Bandwidth of 2,000 cells/sec. For the Periodic test the alarm SCNR should not be active however in the Burst test this alarm should be active. When testing Periodic with extra burst SCNR alarm should be inactive and the received cell count checked. The measurement is gated for 3 seconds at each test point.

Error Add

The instrument is set up to signal 34M, F/G bandwidth is 100% with all header values set to default and payload of Single 2^9 PRBS. Some of the received error counts are not matched with a corresponding generation on the transmit side. Where appropriate the error add is set to OFF, ON, SINGLE and 1.0E-3 rate. When injecting a single Single Header error the Non-Corrected HEC count is checked to be 0, and similarly when a single Double Header error is injected the Corrected HEC count is checked to be 0. When a single bit error is injected the errored cell count is checked to be equal to the number of errors injected. The receiver is gated for 3 seconds and the error count is measured.

Headers

The ability to set up different values of Header field for F/G and B/G streams is tested using the receive filter mechanism to select the stream for test. Each of the streams has a set bandwidth so that cell count can be used to ensure correct identification.
(F/G = 24000cell/s (30%), #1 B/G = 25%, #2 B/G = 20%, #3 B/G = 15%, Fill = 10%). All tests are done with Cross-Cell PRBS 2^23-1 for 140M signal. The test is really split into two parts. In the first part the F/G is tested over a range of the values with the background set to fixed values. Both UNI/NNI modes are tested for VPI values. In the second part the filter mechanism is tested in the receiver using don't care states. Before each test point the headers are set to their default values as in the following Table. The instrument is gated for 2 seconds at each test point.

Table 5-3 Header Default Settings Configuration

Stream	GFC	VPI (UNI)	VCI	PTI	CLP	Cell/sec	Tolerance
F/G	10	0	32	000	0	97811	1
#1 B/G	2	0	33	010	1	81127	3/sec
#2 B/G	3	85	33	010	1	65080	3/sec
#3 B/G	4	0	21845	010	1	49033	3/sec
Fill(Idle)	0	0	0	000	1	32986	10/sec

Payloads

The F/G stream is set to fill the whole of the 34 M signal. Each of the F/G Payload selections are checked. The Header pattern is set to the default values. Pattern sync and pattern errors are checked for each test point. Although pattern errors can not be used for the Test Cell (result is not valid), so here the errored test cell count is checked to be 0. The instrument is gated for 2 seconds at each test point.

Test Cell

There are several tests included here but they are all pertinent to only the Test Cell payload and so have been grouped together. The F/G stream is set to fill the whole of the 34M signal and the Test Cell selected.

1. Cell Loss: This is tested by applying header errors and checking the measured Cell Loss count. The instrument is gated for 3 seconds at each test point.
2. Misinserted Cells: There are three conditions to test for, each test point is gated for 3 seconds:
   a. A misinserted cell that doesn't look like a test cell Misinserted Cell count to increment (60000 ±6) and Errored Cell count to increment (60000 ±6). This is achieved by adding a BG stream with the same header value as the FG.
   b. A misinserted cell that looks like a test cell will cause Misinserted Cell count to increment (3±1) and no increment to the Errored Cell count (0 ±0).
   c. An error in the test cell sequence number but not the CRC will cause the Misinserted Cell count (0 ±0) and Errored cell count to not increment (0 ±0).
3. Cell Transfer Delay: The gated mean cell transfer delay and mean cell transfer delay is tested to be 0 +2 in the normal condition and 307 ±31 usec in the test condition. The maximum cell transfer delay and the peak-to-peak 2-pt CDV are tested to be 0 +2 in the normal condition and 625 ±31 usec in the test condition.
4. Errored Cell count: This is incremented when the EDC's are incorrect which can be forced by applying bit errors. The receiver is gated for 3 seconds for this test.
5. Non-conforming cell count: This is the number of cells exceeding the set CDV PCR and tolerance parameters. Non-conforming cells will be produced by the following two methods:
   a. The PCR is set to 20,000 cells/s and the transmitted cell rate is set to 40,000 cells/s (periodic, burst size of 1). The CDV tolerance is set to 1000 microseconds. This should cause 20,000 non-conforming cells to be received per second. The test is gated for a period of 3 seconds.
   b. The PCR will be set equal to the transmitted cell rate of 20,000 cells/s. The cells are transmitted in the periodic burst mode with a burst size of 2000 cells. The CDV tolerance is set to 74980 microseconds (derived from the max 1 Point CDV equation) and no non-conforming cells are received.
   c. The burst size is increased to 2001 cells and 30 non-conforming cells should be received in 3 seconds.
6. Max 1 Point CDV: two tests are performed for different cell rates by setting the PCR equal to the transmitted cell rate with the CDV tolerance is disabled and the cells transmitted in periodic burst mode with a burst size of 2000 cells. Both tests are run for a three second period.

Trail Trace

The F/G stream is set to fill the whole of the 34M signal with the default distribution and header values. The Trail Trace is captured and checked against the corresponding value. The USER string is 15 characters in length containing a range of ascii characters. - "abcdABCD0123!@#"

Performance Management OAM

1. The F/G stream is set to up with the default header and 40,000 cells/s containing 2^23-1 PRBS are transmitted at 34M. Different POAM flows are added to the FG stream using block size of 512 cells. The receiver block size is set to 128 and Loss of POAM is tested to be active. The receiver block size is then set to 512 and Loss of POAM is tested to be inactive.
2. Different POAM flows are added to the FG stream using block size of 512 cells. The BEDC error count is checked to be 0 ±0 for 3 seconds and then single bit errors are added to the Tx causing 3 ±0 BEDC BIP-16 errors in 3 seconds.
3. Cell Loss and Misinsertion: Each of the following tests are run for a period of 3 seconds. The BEDC error count is tested to be 0 ±0 in each case.
   a. Cell loss can be emulated by adding double header errors at the transmitter which will cause the cells to be discarded at the receiver.
   b. Cell misinsertion can be emulated by adding a BG stream (10 % at 34 M) with the same header values as the FG to the FG stream of 51200 cells/s.

Services Tests

Tests Summary

Test Name
Distribution
AAL
Channel View
Services Processor

Overall Connections

TX Unbalanced Data To RX Unbalanced Data

Distribution

The instrument is set up to default settings of 140M and a payload of test cell. The fg and 9 bgs are set up as shown below. The rx monitors each channel in turn and checks rx cell rate and 1-pt CDV. PCR is set up for expected average cell rate.

The following distributions are set up.

Channel	Cell Rate	Type	Burst Size	Peak Rate
fg	29500	constant	n/a	n/a
bg1	2951	constant	n/a	n/a
bg2	5902	burst	4096	326037
bg3	8853	constant	n/a	n/a
bg4	11804	constant	n/a	n/a
bg5	14505	burst	167	123456
bg6	17706	constant	n/a	n/a

Channel	Cell Rate	Type	Burst Size	Peak Rate
bg7	20657	constant	n/a	n/a
bg8	23608	constant	n/a	n/a
bg9	26559	random	n/a	n/a

AAL

A stored cell stream containing at least two channels of AAL-1, AAL-3/4 & AAL-5 is transmitted. For each AAL, one channel has no impairments and one channel has added impairments. AUTO AAL is selected in the receiver and a check is made to ensure correct AAL has been identified, that AAL loss alarm is not active and that results are as expected. AAL loss alarm is also checked in a separate test.

Channel View

A stored cell is transmitted and selected Channel View VPI, VCIs are checked against the expected result. Total number of received channels is checked.

Services Processor

Subtest 22

This test gets the results of the Services processor power on tests, and if any are not 0, fails the self test.

These tests are:

- The processors power up test.
- The processors check of the type of boot Flash rom.
- The processors check of the CRC over the boot flash rom.
- The processors check on the RAM.
- The processors check on the DUAL PORT ram.
- The processors check on the type of APPLICATION flash ROM.
- The processors check on the CRC over the application flash ROM.

Subtest 23

This subtest tests the TMS chip.

- It sets the output to LAN.
- It sets the input to LAN.
- It sets the protocol to IPX (so dummy addresses will work OK)
- It sets the MAC type to ETHERNET.
- It checks that the TMS selftest is OK.
- It then sets the MAC type to TOKEN RING.
- It then checks the TMS selftest is OK.

Service Sheet G11 - PDH Multiple Outputs Module

Introduction

This Service Sheet should be used when troubleshooting faults associated with the instrument PDH Multiple Outputs Module after performing the troubleshooting described in General Service Sheet G-1. A faulty Multiple Outputs Module will be indicated as a Selftest failure when running the PDH Selftest with each of the outputs from the PDH Multiple Outputs Module looped to the PDH Receiver in turn-see service Sheet G2 for more information on running the selftest.

NOTE A pass must first be obtained on the PDH Selftest with the standard 75Ω PDH Transmitter port looped to the PDH 75Ω Receiver Input port. If the test fails under these conditions the fault is likely to be on the PDH Module or SPDH Modules. Troubleshoot using G9 or G10 Service Sheets.

Troubleshooting Multiple Outputs Selftest Failure

The PDH Multiple Outputs Module has four replaceable on-board fuses. These are fitted to protect output circuitry in the event of electrical overload caused by application of external out-of-spec conditions.

The following troubleshooting aims to isolate the fault to one of the four on-board fuses or another component on the A14 Multiple Outputs Board. In the event of failure of one of these fuses it may be replaced using the part number from the Replaceable Parts section of this Manual .

If the fault is not caused by a fuse, the A14 board assembly should be replaced using the Replacement Procedures section in this Manual. The correct part to order will be found in the Replaceable Parts section in this Manual.

Troubleshooting Procedure

Use the following procedure to troubleshoot a PDH Multiple Outputs Selftest failure.

1 Check which of the three additional Multiple Outputs ports (Output 1 to Output 3 on the Multiple Output Module) is connected to the PDH Receiver 75Ω Input port when selftest failure occurs:
If Output 1, suspect A14 F2 (see diagram on next page).
If Output 2, suspect A14 F3 (see diagram on next page).
If Output 3, suspect A14 F4 (see diagram on next page).
If Outputs 1, 2, 3 all fail, suspect A14 F1.

2 Replace the suspect fuse and re-run the PDH selftest with the faulty output port looped to the PDH Receiver 75Ω input port.
If failure still occurs, suspect the A14 Multiple Outputs Board.

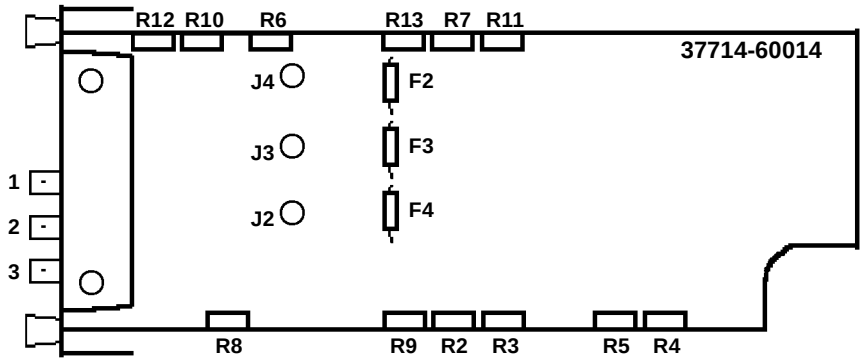


Figure 5-6 A14 Board Assembly Layout

Service Sheet G12 - SDH Module

Introduction

This Service Sheet should be used when troubleshooting faults associated with the instrument SDH Module after performing the troubleshooting described in General Service Sheet G1. A faulty SDH module will normally be indicated as an SDH selftest failure when running the instrument selftest.

NOTE If Structured PDH modules are fitted, the instrument must pass the SPDH selftest before troubleshooting SDH failure.

Troubleshooting Selftest Failure

As these Modules are on the Module Exchange program, no board level troubleshooting is required. If the SDH Selftest fails check the SDH OUT port is looped to the SDH IN port via a good 75Ω cable and the correct RS449 looping connections are made (see Service Sheet G2). If OK carry out the SDH adjustments given in Section 3. If selftest still fails order a new assembly using the numbers from the Replaceable Parts Section.

SDH Tests (A1T/A3R Module)

Subtests 1 to 2 STM1 TX/RX

These tests check that the unit under test Transmitter can transmit an STM1 signal and that the unit under test Receiver can receive that signal, via the STM1 digital circuits and the analogue input stages. An external STM1 loopback is used.

The unit under test is reset to its SDH default state and then set up as follows:

TEST TIMING	3 SECONDS
LOOPBACK	STM1 EXTERNAL

Subtest 1

The unit under test Receiver is checked for no Loss of Signal.

Subtest 2

The unit under test is allowed to gain pattern sync and is then gated for 3 seconds. At the end of the gating period, the bit error count should be within the specified limits.

Subtest 3 STM1 RX Monitor Test

This tests checks that the unit under test Receiver can switch to Monitor mode (High impedance input). An external STM1 loopback is used.

The unit under test is reset to its SDH default state and then set up as follows:

TEST TIMING	3 SECONDS
SIGNAL IN	MONITOR
LOOPBACK	STM1 EXTERNAL

Subtest 3

The unit under test Receiver should not synchronise to the received signal.

Subtests 4 STM1 RX Loss of Signal Test

This tests checks that the unit under test Receiver can detect Loss Of Signal. An external STM1 loopback is used.

The unit under test is reset to its SDH default state and then set up as follows:

TEST TIMING	3 SECONDS
ALARM	Loss Of Signal
LOOPBACK	STM1 EXTERNAL

Subtest 4

The unit under test Receiver id checked for no Loss Of Signal.

Subtest 5 Frequency Measurement

This test checks that the frequency measurement circuitry is functioning correctly. This test is *NOT* intended to check transmit clock accuracy.

The unit under test is reset to its SDH default state. External STM1 Loopback is used.

The received clock rate is measured and compared against limits.

Subtests 6 to 7 Clock Offset Measurement STM-1

These tests check that the frequency measurement circuitry can detect clock offsets of ±-100 ppm. This test is *NOT* intended to check transmit clock accuracy.

The unit under test is reset to its SDH default state. Then setup as follows:

TX Clock Offset as in the following Table.
External STM1 Loopback is used.

The received clock offset is measured and compared against limits.

Subtest Number	Frequency Offset		
	Nominal	min (-5 ppm)	max (+5 ppm)
6	+100.00 ppm	+95.00 ppm	+105.00 ppm
7	-100.00 ppm	105.00 ppm	-95.00 ppm

Subtests 8 to 9 Clock Reference Source

These subtests check that the clock can be referenced to the internal source.

The unit under test is reset to its SDH default state, then set up as follows:

LOOPBACK	STM1 EXTERNAL

Subtest 8

The ALARM register is checked for no Clock Loss.

Subtest 9

The Reference Clock divide ratio is then set to 193 by setting CTRSEL (0..4).

This is a special command which introduces the wrong divide ratio into the PLL.

The ALARM register is checked for Clock Loss.

Subtest 10 ODL Processor Tests

These tests checks that the ODL Processor is running and that the ODL Processor can transmit and receive in all soh and poh bytes.

NOTE A special test function in the ODL code is used to transmit and check reception on STM-1 overhead channels is utilized. This function is not selecTable from the front panel.

This test first check that the ODL processor is running.

This test involves the ODL processor transmitting a known pattern in each Transmit SOH and POH channel and checking that the pattern can be received in the corresponding Receive SOH and POH channels. Each channel is tested in sequence.

To achieve this, the ODL processor writes to the TRSTM-1 ASIC to update the overhead byte being tested and monitors the overhead byte received by the ASIC.

External STM1 Loopback is used.

Subtest 11 VC4 POH

This subtest checks that the unit under test Transmitter can send a message in the J1 bytes and that the unit under test Receiver can receive that message.

The unit under test is reset to its SDH default state, the following default message is sent in the J1 bytes.

HEWLETT PACKARD HP37714A PDH/SDH

FIELD TEST SET, 0000U00000 (CR) (LF)

NOTE The instrument number and serial number will vary between instruments.

Subtests 12 to 16 STM1 B1, B2, B3, MS FEBE, AU-4 IEC Error Detection

These tests check that the unit under test Receiver can generate and detect errors in the specified overhead bytes.

The unit under test is reset to its SDH default state, then set up as follows:

TX	
Error Add	as in the following Table
RX	
Test Timing	3 seconds
Loopback	STM-1 External

For each subtest, the unit under test is allowed to gain FRAME and POINTER sync and is then gated for 3 seconds. The results are checked against the limits.

.

Subtest Number	Error	Error Add	Result	
			min	max
12	B1	Single	1	1
13	B2	Single	1	1
14	B3	Single	1	1
15	(M1) MS FEBE	Single	1	1
16	(Z5)AU-4 IEC	Single	1	1

Subtest 17 STM-1 A1A2 Error Add

This test checks that the unit under test Tx can generate Frame A1A2 errors.

The unit under test is reset to its SDH default state, then set up as follows:

Tx

Test Function	SDH ERR and ALARM
Error Add Type	(A1A2 FRAME)
Error Add Rate	As per Table
Loopback	STM-1 EXTERNAL

The unit under test is allowed to gain FRAME sync. Frame errors are then generated at an increasing rate until LOF occurs at 4 in 4 error rate. The error rate is then decreased until FRAME sync is regained at 2 in 4 error rate.

Subtest Number	Frame A1 A2 Error Rate
17	OFF
	1 in 4
	2 in 4
	3 in 4
	4 in 4
	3 in 4
	2 in 4
	1 in 4
	OFF

Subtest 18 STM1 140 Mb/s Payload Bit Error Add & Detect

This test checks that the unit under test Transmitter can insert bit errors into the 140M payload and that the unit under test Receiver can detect these errors.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The unit under test will source payload from the the SPDH module if it is present, otherwise the payload is sourced by the unit under test.

TX

PAYLOAD	ERROR ADD - SINGLE
MODE	UNFRAMED

RX

TEST TIMING	3 SECONDS
LOOPBACK	STM1 EXTERNAL

The unit under test is allowed to gain PATTERN sync and is then gated for 3 seconds. The received Bit Error Count is checked.

Subtest 19 to 20 STM1 140 Mb/s Payload VC Offset Test

This test checks that the unit under test Transmitter can frequency offset the 140M payload and that the unit under test Receiver can detect these errors in the presence of payload frequency offset.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The unit under test will source payload from the SPDH module if it is present, otherwise the payload is sourced by the unit under test.

TX

PAYLOAD	ERROR ADD - 1E-3
MODE	UNFRAMED
140M OFFSET	As Specified in Table

RX

TEST TIMING	3 SECONDS
LOOPBACK	STM1 EXTERNAL

The unit under test is allowed to gain PATTERN sync and is then gated for 3 seconds. The received Bit Error Count is checked against the expected result.

Subtest Number	VC Offset	Bit Error Count	
		min	max
19	+100 ppm	417832	417836
20	-100 ppm	417748	417752

Subtest 21 VC3 POH

This subtest checks that the unit under test Transmitter can send a message in the J1 bytes and that the unit under test Receiver can receive that message.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU3

RX

PAYLOAD TU3
LOOPBACK STM-1 External

The following default message is sent in the J1 bytes and checked in the Receiver:

“HEWLETT-PACKARD, HP37714A PDH/SDH

FIELD TEST SET, 0000U0000 (CR) (LF)”.

NOTE The instrument number and serial number will vary between instruments.

Subtests 22 STM1 VC3 B3 Error Detection

This test checks that the unit under test Receiver can generate and detect VC3 path B3 errors.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD TU3
ERROR ADD As per Table

RX

PAYLOAD TU3
TEST TIMING 3 SECONDS
LOOPBACK STM-1 EXTERNAL

The unit under test is allowed to gain FRAME and POINTER sync and is then gated for 3 seconds.

Subtest Number	Errors Added	Error Add	Error Rate	
			min	max
22	VC3 Path B3	Single	1	1

Subtest 23 STM1 VC3 Path FEBE Error Detection

This test checks that the unit under test Receiver can generate and detect VC3 Path FEBE errors.

The unit under test is reset to its SDH default state, then set up as follows:

TX

ERROR ADD As per Table
PAYLOAD TU3

RX

PAYLOAD TU3
TEST TIMING 3 seconds
LOOPBACK STM-1 External

The unit under test is allowed to gain FRAME and POINTER sync and is then gated for 3 seconds.

Subtest Number	Errors Added	Error Add	Error Rate	
			min	max
23	VC3 Path FEBE	Single	1	1

Subtest 24 STM1 TU3 Payload Bit Error Add & Detect

This test checks that the unit under test Transmitter can insert bit errors into the 34M payload and that the unit under test Receiver can detect these errors.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The unit under test will source payload from the SPDH module if it is present, otherwise the payload is sourced by the unit under test.

TX

PAYLOAD TU3
ERROR ADD SINGLE (PAYLOAD)

RX

PAYLOAD TU3
TEST TIMING 3 SECONDS
LOOPBACK STM1 EXTERNAL

The unit under test is allowed to gain PATTERN sync and is then gated for 3 seconds.

Subtests 25 to 26 TU3 Background Pattern Tests

These tests check that the unit under test Transmitter can transmit an STM-1 TU3 payload with the correct background pattern.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD TU3 in TUG[2]
BACKGROUND TUG[1] -01010101
TUG[3] -00001111

RX

PAYLOAD TU3 in TUG[1] and in TUG[3]
LOOPBACK STM-1 External

Subtest 25

Check unit under test Rx for Pattern Loss.

Subtest 26

Check unit under test for pattern sync on TUG[1].

Check unit under test for pattern sync on TUG[3].

Subtests 27 to 33 STM1 with TU12 Payload (Async)

These tests check that the unit under test Transmitter can transmit the correct values for the specified overhead bytes and that the unit under test Receiver can detect these values.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The unit under test will source payload from the SPDH module if it is present, otherwise the payload is sourced by the unit under test.

TX

PAYLOAD	TU12
MODE	Async

RX

PAYLOAD	TU12
TEST TIMING	3 SECONDS
LOOPBACK	STM1 EXTERNAL

The unit under test is allowed to gain FRAME and POINTER sync and is then gated for 3 seconds.

Subtests 34 to 40 STM1 with TU12 Payload (Floating Byte Sync)

- These tests check that the unit under test Transmitter can transmit the correct values for the specified overhead bytes and that the unit under test Receiver can detect these values.
- The unit under test is reset to its SDH default state, then set up as follows:

NOTE The unit under test will source payload from the SPDH module if it is present, otherwise the payload is sourced by the unit under test.

TX

PAYLOAD	TU12
MODE	Floating Byte

RX

PAYLOAD	TU12
TEST TIMING	3 SECONDS
LOOPBACK	STM1 EXTERNAL

The unit under test is allowed to gain FRAME and POINTER sync and is then gated for 3 seconds.

Subtests 41 to 42 STM1 TU12 V5 BIP-2, V5 FEBE Error Detection (Async)

These tests check that the unit under test can generate and detect errors in the specified overhead bytes.

The unit under test is reset to its SDH default state, then set up as follows:

TX

ERROR Add	As per Table
PAYLOAD	TU12
MODE	Async

RX

PAYLOAD	TU12
MODE	Async
TEST TIMING	3 SECONDS
LOOPBACK	STM-1 EXTERNAL

The unit under test is allowed to gain FRAME and POINTER sync and is then gated for 3 seconds.

Subtest Number	Errors Added	Error Add	Error Rate	
			min	max
41	V5 BIP-2	1E-3	9.990E-4	1.001E-3
42	V5 FEBE	1E-4	9.990E-5	1.001E-4

Subtest 43 STM1 TU12 Payload Bit Error Add & Detect (Async)

This test checks that the unit under test Transmitter can insert bit errors into the TU12 payload and that the unit under test Receiver can detect these errors.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The unit under test will source payload from the SPDH module if it is present, otherwise the payload is sourced by the unit under test.

TX

PAYLOAD	TU12
MODE	Async
ERROR ADD	SINGLE (PAYLOAD)

RX

PAYLOAD	TU12
MODE	Async
TEST TIMING	3 SECONDS
LOOPBACK	STM1 EXTERNAL

The unit under test is allowed to gain PATTERN sync and is then gated for 3 seconds.

Subtest 44 STM1 TU12 Payload Bit Error Add & Detect (Floating Byte Sync)

This test checks that the unit under test Transmitter can insert bit errors into the TU12 payload and that the unit under test Receiver can detect these errors.

NOTE The unit under test will source payload from the SPDH module if it is present, otherwise the payload is sourced by the unit under test.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU12
MODE	Floating Byte
ERROR ADD	SINGLE (PAYLOAD)

RX

PAYLOAD	TU12
MODE	Floating Byte
TEST TIMING	3 SECONDS
LOOPBACK	STM1 EXTERNAL

The unit under test is allowed to gain PATTERN sync and is then gated for 3 seconds.

Subtests 45 to 48 Pattern Tests

These tests check that the unit under test Transmitter can transmit an STM-1 payloads containing the correct test patterns and that the unit under test Receiver can detect these patterns error free.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	As per Table
PATTERN	As per Table

RX

PAYLOAD	As per Table
PATTERN	As per Table

The Receiver is first checked to have a signal present, then Pattern Sync is checked.

Subtest Configurations					
Subtest Number	**Freq**	**Pattern**	**Error Add**	**Test Time**	**Nominal count**
45	140M	PRBS(23)	Single	1	1
46	TU3	PRBS(15)	Single	1	1
47	TU12	WORD_1*	Single	1	1
48	TU2	PRBS(9)	Single	1	1

Subtests 49 to 50 TU12 Background Pattern Tests (Async)

These tests check that the unit under test Transmitter can transmit an STM-1 TU12 payload with the correct background pattern.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU12 (Async)
TU	TUG3[1] TUG2[1] TU[1]
BACKGROUND PATTERN	2^9-1 PRBS

RX

PAYLOAD	TU12 (Async)
TU	TUG3[2]
	TUG2[1]
	TU[1]
LOOPBACK	STM-1 External
PATTERN	2^9-1 PRBS

Subtest 49

Check unit under test Rx TUG[1] for Pattern Loss.

Subtest 50

Check unit under test Rx TUG[2] for Pattern Loss.

Subtest 51 STM1 TU2 Payload Bit Error Add & Detect (Async)

This test checks that the unit under test Transmitter can insert bit errors into the TU12 payload and that the unit under test Receiver can detect these errors.

NOTE The unit under test will source payload from the SPDH module if it is present, otherwise the payload is sourced by the unit under test.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU2
MODE	Async
ERROR ADD	SINGLE (PAYLOAD)

RX

PAYLOAD	TU2
MODE	Async
TEST TIMING	3 SECONDS
LOOPBACK	STM1 EXTERNAL

The unit under test is allowed to gain PATTERN sync and is then gated for 3 seconds.

Subtests 52 to 58 140 Mb/s Frequency Offset Pointer Movements

These tests check that the unit under test can generate and detect frequency offset pointer movements and that no errors or major alarms are generated.

This test is *NOT* intended to check the accuracy of frequency offset pointer moves.

The unit under test is reset to its SDH default state. Then setup as follows:

TX

PAYLOAD	40 Mb/s
FREQUENCY OFFSET	Pointer movements As per Table

RX
External STM1 Loopback is used.

In the presence of +100 ppm Frequency offset alarms and errors are checked The received clock offset is measured and compared against limits.

Subtest Number	Implied VC Offset		
	Nominal	min (-5 ppm)	max (+5 ppm)
57	+100.00 ppm	+95.00 ppm	+105.00 ppm
58	-100.00 ppm	-105.00 ppm	-95.00 ppm

Subtests 59 to 66 TU3 Frequency Offset Pointer Movements

These tests check that the unit under test can generate and detect frequency offset pointer movements and that no errors or major alarms are generated.

This test is *NOT* intended to check the accuracy of frequency offset pointer moves.

The unit under test is reset to its SDH default state. Then setup as follows:

TX
PAYLOAD TU3
Frequency Offset Pointer movements As per Table

RX
External STM1 Loopback is used.

In the presence of +100 ppm Frequency offset alarms and errors are checked.

The received clock offset is measured and compared against limits.

Subtest Number	Implied VC Offset		
	Nominal	min (-5 ppm)	max (+5 ppm)
65	+100.00 ppm	+95.00 ppm	+105.00 ppm
66	-100.00 ppm	-105.00 ppm	-95.00 ppm

Subtests 67 to 74 TU12 Frequency Offset Pointer Movements

These tests check that the unit under test can generate and detect frequency offset pointer movements and that no errors or major alarms are generated.

This test is *NOT* intended to check the accuracy of frequency offset pointer moves.

The unit under test is reset to its SDH default state. Then setup as follows:

TX
PAYLOAD TU12
Frequency Offset Pointer movements As per Table

RX
External STM1 Loopback is used.

In the presence of +100 ppm Frequency offset, alarms and errors are checked The received clock offset is measured and compared against limits.

Subtest 75 STM-1 Thru Mode tests

This test checks the unit under test THRU Mode circuitry. A special function provides loopback of received data in the presence of TU12 Payload, a check is performed on the H4

Subtest Number	Frequency Offset		
	Nominal	min (-5 ppm)	max (+5 ppm)
73	+100.00 ppm	+95.00 ppm	+105.00 ppm
74	-100.00 ppm	-105.00 ppm	-95.00 ppm

Framing status of the looped back TU12 data. Successfully finding H4 Framing pattern indicates that the THRU mode circuitry is functioning (i.e.. received data is correctly looped back to be retranmitted)

The unit under test is set to its SDH default state. Then setup as follows:

TX
MODE STM1e THRU
Special Function to select TEST Mode in 'LoopThru' LCA.

RX
PAYLOAD TU12
Special Function to check for H4 Framing Status.

Using Special Receive Function Check for H4 Frame synchronization for the received signal.

Subtest 76 to 77 DCC Port Tests

These tests check that the Datacomm interface is functioning. As both the Drop and Insert DCC functions require a clock from the module, an internal loopback has been provided for selftest. The test uses an external Datacomm Loopback. A special function on the ODL processor is invoked for this test.

External Datacomm Loopback is used.

The unit under test is reset to its default state (panel 0), then set up as follows:

TX
DCC INSERT REGEN DCC or MULTI DCC

RX
DCC DROP REGEN DCC or MULTI DCC

Other
Loopback (DCC Data) External
Loopback (DCC CLOCK) Internal

A special test function on the ODL processor check that the RSOH or MSOH can be Dropped and Inserted.

A3R Additional Tests (STM-1)

NOTE All the tests in this section (Subtests 78 to 104) are valid for both A1T and A3R. The functionality tested here was introduced with A3R firmware, but the features all work with A1T hardware as well.

Subtest 78 to 80 STM-1 Bulk Filled Payload Pattern Sync Test

This test checks that the unit under test Receiver can sync up to the unit under test Transmitter.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The unit under test will source payload from the SPDH module if it is present, otherwise the payload is sourced by the unit under test.

TX
PAYLOAD as per Table

RX
PAYLOAD AU-4 Unframed to check for PSL, then switch to the TX payload mapping to check for gain of sync.
LOOPBACK STM-1 External

The test begins in a 'loss of sync' state (i.e., differing payload mappings on the Transmitter and Receiver). We check to ensure that we have PATTERN SYNC LOSS.

The RX is then switched to use the same payload mapping as the TX. The unit under test should then gain PATTERN sync.

Subtest Number	Payload
78	AU-4 BULK
79	TU-3 BULK
80	TU-12 BULK

Subtest 81 to 83 STM-1 DS3 Payload Framing Test

This test checks that the unit under test Receiver can sync up to the unit under test Transmitter.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The SPDH module must be present for this test. DS3 is not available in SDH stand alone mode.

TX

PAYLOAD as per Table

RX

PAYLOAD TU-3 Unframed to check for PSL, then switched to the TX payload mapping to check for gain of sync.
LOOPBACK STM-1 External

The test begins in a 'loss of sync' state (i.e., differing payload mappings on the Transmitter and Receiver). We check to ensure that we have PATTERN SYNC LOSS.

The RX is then switched to use the same payload mapping as the TX. The unit under test should then gain PATTERN sync.

Subtest Number	Payload
81	DS3 Unframed
82	DS3 M23
83	DS3 C-Bit

Subtest 84 to 87 STM-1 DS1 Payload Framing Test

This test checks that the unit under test Receiver can sync up to the unit under test Transmitter.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The SPDH module must be present for this test. DS1 is not available in SDH stand alone mode.

TX
PAYLOAD as per Table

RX

PAYLOAD	TU-12 Unframed to check for PSL, then switch to the TX payload mapping to check for gain of sync.
LOOPBACK	STM-1 External

The test begins in a 'loss of sync' state (i.e., differing payload mappings on the Transmitter and Receiver). We check to ensure that we have PATTERN SYNC LOSS.

The RX is then switched to use the same payload mapping as the TX. The unit under test should then gain PATTERN sync.

Subtest Number	Payload
84	DS1 Unframed
85	DS1 D4
86	DS1 ESF
87	DS1 SLC-96

Subtest 88 STM-1 J0 Message

This subtest checks that the unit under test Transmitter can send a message in the J0 bytes and that the unit under test Receiver can receive that message.

The unit under test is reset to its SDH default state, the following default message is sent in the J0 bytes (15 bytes & 1 byte CRC).

HEWLETT-PACKARD

NOTE The instrument number and serial number will vary between instruments.

Sub-Tests 89 to 93 New A3R Payloads Pattern Tests

These tests check that the unit under test Transmitter can transmit an STM-1 payloads containing the correct test patterns and that the unit under test Receiver can detect these patterns error free.

NOTE The SPDH module must be present for tests 92 and 93. DS3 and DS1 are not available in SDH stand alone mode.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD As per Table
PATTERN As per Table

RX

PAYLOAD As per Table
PATTERN As per Table

The Receiver is first checked to have a signal present, then Pattern Sync is checked. For each of the settings the bit error count is measured, and checked to be one.

Subtest Configurations					
Subtest Number	**Payload**	**Pattern**	**Error Add**	**Test Time**	**Nominal count**
89	C-4 Bulk	PRBS(11)	Single	1	1
90	C-3 Bulk	PRBS(9)	Single	1	1
91	C-12 Bulk	WORD_1*	Single	1	1
92	DS-3 Unframed	PRBS(20)	Single	1	1
93	DS-1 Unframed	QRSS	Single	1	1

NOTE WORD _1 = 1100010011110110

Subtests 94 to 96 TU-3 Mixed Payload Tests

These tests check that the unit under test Transmitter can transmit an STM-1 TU-12 Background mapping in the selected TUG-3 while the foreground is a TU-3 mapping.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD TU-3
MAPPING 34 Mb/s
BACKGROUND MAPPING TU-12 in TUG-3 #2

RX

PAYLOAD	TU-12
MAPPING	Async 2 Mb/s
TUG-3 #	As per Table
LOOPBACK	STM-1 External

.

Subtest Number	RX TUG3 # under test
94	2
95	1
96	3

Check TUG-3 #2 in the RX is free of alarms.
Check TUG-3 #1 & #3 sync up to a TU-3 mapping

Subtest 97 to 99 TU-12 Mixed Payload Tests

These tests check that the unit under test Transmitter can transmit an STM-1 TU-3 Background mapping in the selected TUG-3 while the foreground is a TU-12. mapping.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU-12
MAPPING	Async 2 Mb/s
BACKGROUND MAPPING	TU-3 in TUG-3 #1

RX

PAYLOAD	TU-3
MAPPING	34 Mb/s
TUG-3 #	As per Table
LOOPBACK	STM-1 External

.

Subtest Number	RX TUG3 # under test
97	1
98	2
99	3

Check TUG-3 #1 in the RX is free of alarms.
Check TUG-3 #2 & #3 sync up to a TU-12 mapping.

Subtests 100 to 101 TU12 Background Pattern Tests (DS1)

These tests check that the unit under test Transmitter can transmit an STM-1 TU12 DS1 payload with the correct background pattern.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU12
MAPPING	As per Table
TU	TUG3[x] TUG2[y] TU[z] as per Table
BACKGROUND PATTERN	As per Table

RX

PAYLOAD	TU12
MAPPING	As per Table
TU	Check foreground [x,y,z] and then background [m,n,p]
LOOPBACK	STM-1 External
PATTERN	As per Table

Subtest Number	TX Foreground Mapping	RX Trib to test for Foreground Mapping	RX Trib to test for Background Mapping	Expected Background Mapping	Background Pattern
100	Unframed	x=3, y=1, z=2	m=2, n=1, p=2	D4	2^9-1 PRBS
101	ESF	x=2,y=3,z=1	m=2,n=3,p=3	D4	2^15-1 PRBS

For each mapping type:
Check unit under test RX foreground for Pattern Sync.
Check unit under test Rx background TUG3 for Pattern Sync.
x = TUG-3 #
y = TUG-2 #
z = TUG #

Subtest 102 to 104 STM-1 Service Disruption Test

This subtest checks that the unit under test can measure error burst lengths in the RX.

NOTE The SPDH module must be present for this test. Service Disruption is not available in SDH stand alone mode nor if the UPDH module is fitted.

The unit under test is reset to its SDH default state and then set up as follows:

TX

PAYLOAD	SDH AU-4
TIMING	3 SECONDS
PATTERN	As per Table
LOOPBACK	STM1 EXTERNAL

RX

PAYLOAD	SDH AU-4
TIMING	3 SECONDS
PATTERN	As per Table
LOOPBACK	STM-1 EXTERNAL

The instrument is gated and then the burst length is read back. Note that for Test 104, gating must be started before the pattern is changed. Ensure the pattern changes before 2 gating seconds have elapsed.

Subtest Number	TX Pattern	RX Pattern
102	PRBS23	PRBS23
103	PRBS15	PRBS23
104	PRBS23	PRBS23

A3R STM-0 Tests

NOTE All the tests in this section (Subtests 105 to 124) are only valid if an A3R module is fitted. An A1T module cannot run the following tests as it does not allow STM-0 electrical operation.

Subtests 105 to 106 STM-0 TX/RX

These tests check that the unit under test Transmitter can transmit an STM-0 signal and that the unit under test Receiver can receive that signal, via the STM-0 digital circuits and the analogue input stages. An external STM-0 loopback is used.

The unit under test is reset to its SDH default state and then set up as follows:

RATE	STM-0 AU-3
GATING TIME	3 SECONDS
LOOPBACK	STM-0 EXTERNAL

Subtest 105

The unit under test Receiver is checked for no Loss of Signal.

Subtest 106

The unit under test is allowed to gain pattern sync and is then gated for 3 seconds. At the end of the gating period, the bit error count should be within the specified limits.

Subtests 107 STM-0 RX Loss of Signal Test

This tests checks that the unit under test Receiver can detect Loss Of Signal. An external STM-0 loopback is used.

The unit under test is reset to its SDH default state and then set up as follows:

RATE	STM-0 AU-3
GATING TIME	3 SECONDS
ALARM	Loss Of Signal
LOOPBACK	STM-0 EXTERNAL

Subtest 107

The unit under test Receiver is checked for no Loss Of Signal.

Subtests 108 to 110 STM-0 TX/RX Pulse Shape Test

These tests check that the unit under test Transmitter can transmit an STM-0 signal and that the unit under test Receiver can receive that signal, via the STM-0 digital circuits and the analogue input stages. An external STM-0 loopback is used.

The unit under test is reset to its SDH default state and then set up as follows:

RATE	STM-0 AU-3
TX PULSE SHAPE	As per Table
RX PULSE SHAPE	As per Table
GATING TIME	1 SECOND
LOOPBACK	STM-0 EXTERNAL

The unit under test is allowed to gain pattern sync and is then gated for 1 second. At the end of the gating period, the bit error count should be within the specified limits.

Subtest Number	TX Pulse Shape	RX Pulse Shape	Bit Error Count	
			min	max
108	HI	HI	0	0
109	LO	LO	0	0
110	X-CONNECT	HI	0	0

Subtest 111 Frequency Measurement

This test checks that the frequency measurement circuitry is functioning correctly. This test is *NOT* intended to check transmit clock accuracy.

The unit under test is reset to its SDH default state, and then the Transmitter and Receiver are set to STM-0 AU-3. External STM-0 Loopback is used.

The received clock rate is measured and compared against limits.

Subtest 112 to 114 STM-0 Payload Framing Test

This test checks that the unit under test Receiver can sync up to the unit under test Transmitter.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The unit under test will source payload from the SPDH module if it is present, otherwise the payload is sourced by the unit under test.

- TX
  PAYLOAD - as per Table
- RX
  PAYLOAD - AU-3 Unframed to check for PSL, then switch to the TX payload mapping to check for gain of sync.
  LOOPBACK - STM-1 External

The test begins in a 'loss of sync' state (i.e., differing payload mappings on the Transmitter and Receiver). We check to ensure that we have PATTERN SYNC LOSS.

The RX is then switched to use the same payload mapping as the TX. The unit under test should then gain PATTERN sync.

Subtest Number	Payload
112	C3-BULK
113	TU-2 BULK
114	DS1 Unframed

Subtests 115 to 119 STM-0 B1, B2, B3, MS FEBE, AU-3 IEC Error Detection

These tests check that the unit under test Receiver can generate and detect errors in the specified overhead bytes.

The unit under test is reset to its SDH default state, then set up as follows:

TX
RATE: STM-0 AU-3
ERROR ADD: As per Table

RX
RATE: STM-0 AU-3
TEST TIMING: 3 SECONDS
LOOPBACK: STM-0 EXTERNAl

For each subtest, the unit under test is allowed to gain FRAME and POINTER sync and is then gated for 3 seconds. The results are checked against the limits.

Subtest Number	Error	Error Add	Result	
			min	max
115	B1	Single	1	1
116	B2	Single	1	1
117	B3	Single	1	1
118	(M1) MS FEBE	Single	1	1
119	(Z5)AU-3 IEC	Single	1	1

Subtest 120 to 123 STM-0 VC-3 Payload VC Offset Test

This test checks that the unit under test Transmitter can frequency offset the AU-3 payload and that the unit under test Receiver can detect these errors in the presence of payload frequency offset.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The unit under test will source payload from the SPDH module if it is present, otherwise the payload is sourced by the unit under test.

TX

RATE	STM-0
PAYLOAD	1E-3
ERROR ADD	
MODE	UNFRAMED
34M OFFSET	As specified in Table

RX

RATE	STM-0 AU-3
TEST TIMING	3 SECONDS
LOOPBACK	STM-0 EXTERNAL

The unit under test is allowed to gain PATTERN sync and is then gated for 3 seconds. The received Bit Error Count is checked.

Subtest Number.	Mapping	VC Offset	Bit Error Count	
			min	max
120	34 Mb/s	+100 ppm	103112	103116
121	34 Mb/s	-100 ppm	103092	103096
122	DS-3	+100 ppm	134220	134224
123	DS-3	-100 ppm	134192	134196

Subtest 124 STM-0 Thru Mode tests

NOTE This test is not implemented.

This test checks the unit under test THRU Mode circuitry. A special function provides loopback of received data in the presence of TU12 Payload, a check is performed on the H4 Framing status of the looped back TU12 data. Successfully finding H4 Framing pattern indicates that the THRU mode circuitry is functioning (i.e.. received data is correctly looped back to be retranmitted).

The unit under test is set to its SDH default state. Then setup as follows:

TX
MODE STM-0e THRU

Special Function to select TEST Mode in 'LoopThru' LCA

RX
PAYLOAD TU12

Special Function to check for H4 Framing Status.

Using Special Receive Function Check for H4 Frame synchronisation for the received signal.

G.707 Additional Tests (TU-11 and AU-3)

All Option 120 features are standard for A3R, (excluding SONET which is the only feature of Option 120). Therefore, the TU-11 and AU-3 tests do not require Option 120 to be fitted. All TU-11 tests require option 110.

Subtests 125 to 131 STM1 with TU11 Payload (Async)

These tests check that the unit under test Transmitter can transmit the correct values for the specified overhead bytes and that the unit under test Receiver can detect these values.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The unit under test will source payload from an SPDH module.

TX

PAYLOAD TU11
MODE Async

RX

PAYLOAD TU11
TEST TIMING 3 SECONDS
LOOPBACK STM1 EXTERNAL

The unit under test is allowed to gain FRAME and POINTER sync and is then gated for 3 seconds. The Received overhead bytes are checked for no errors.

Subtests 132 to 133 STM1 TU11 V5 BIP-2, V5 FEBE Error Detection

These tests check that the unit under test can generate and detect errors in the specified overhead bytes.

The unit under test is reset to its SDH default state, then set up as follows:

TX

ERROR Add	As per Table.
Payload	TU11
Mode	Async

RX

Payload	TU11
Mode	Async
Test Timing	3 seconds
Loopback	STM-1 External

The unit under test is allowed to gain FRAME and POINTER sync and is then gated for 3 seconds. The results are checked against the limits.

Subtest Number	Errors Added	Error Add	Error Rate	
			min	max
132	V5 BIP-2	1E-3	9.990E-4	1.001E-3
133	V5 LP-REI	1E-4	9.990E-5	1.001E-4

Subtest 134 STM1 TU11 Payload Bit Error Add & Detect (Async)

This test checks that the unit under test Transmitter can insert bit errors into the TU11 payload and that the unit under test Receiver can detect these errors.

The unit under test is reset to its SDH default state, then set up as follows:

NOTE The unit under test will source payload from an spdh module.

TX

PAYLOAD	TU11
MODE	Async
ERROR ADD	SINGLE (PAYLOAD)

RX

PAYLOAD	TU11
MODE	Async
TEST TIMING	3 SECONDS
LOOPBACK	STM1 EXTERNAL

The unit under test is allowed to gain PATTERN sync and is then gated for 3 seconds. The received Bit Error Rate is checked against the result.

Subtests 135 to 136 TU11 Background Pattern Tests (Async)

These tests check that the unit under test Transmitter can transmit an STM-1 TU11 payload with the correct background pattern.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU11 (Async)
FOREGROUND PATTERN	2^15 PRBS
TU	TUG3[1] TUG2[1] TU[1]
BACKGROUND PATTERN	2^9-1 PRBS

RX

PAYLOAD	TU11 (Async)
TU	TUG3[2] TUG2[1] TU[1]
LOOPBACK	STM-1 External
PATTERN	2^9-1 PRBS

Subtest 135

Check unit under test Rx TUG[1] for Pattern Loss.

Subtest 136

Check unit under test Rx TUG[2] for Pattern Loss.

Subtests 137 to 144 TU11 Frequency Offset Pointer Movements

These tests check that the unit under test can generate and detect frequency offset pointer movements and that no errors or major alarms are generated.

This test is *NOT* intended to check the accuracy of frequency offset pointer moves.

The unit under test is reset to its SDH default state. Then setup as follows:

- TX
  PAYLOAD - TU11
  Frequency Offset Pointer movements as per Table.
- RX
  External STM1 Loopback is used.

In the presence of +100 ppm Frequency offset, alarms and errors are checked.

The received clock offset is measured and compared against limits..

Subtest Number	Frequency Offset		
	Nominal	min (-5 ppm)	max (+5 ppm)
143	+100.00 ppm	+95.00 ppm	+105.00 ppm
144	-100.00 ppm	-105.00 ppm	-95.00 ppm

Subtests 145 to 147 TU-3 Mixed Payload Tests

These tests check that the unit under test Transmitter can transmit an STM-1 TU-11 Background mapping in the selected TUG-3 while the foreground is a TU-3. mapping.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU-3
FOREGROUND	TU-3 34 Mb/s
TUG3 #1	
TUG3 #2	TU-11 MAP
TUG3 #3	TU-3 WORD

RX

PAYLOAD	As per Table
MAPPING	As per Table
TUG-3 #	As per Table
LOOPBACK	STM-1 External

Check TUG-3 #2 in the RX is free of any of the alarms. .
Check TUG-3 #1 & #3 sync up to a TU-3 mapping.

Subtest Number	RX TUG3 # under test	RX Mapping
145	2	TU-11 DS1
146	1	TU-3 34 Mb/s
147	3	TU-3 Word

Subtest 148 to 150 TU-11 Mixed Payload Tests

These tests check that the unit under test Transmitter can transmit an STM-1 TU-3 Background mapping in the selected TUG-3 while the foreground is a TU-11. mapping.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU-11
TUG3 #1	TU-3 Word
FOREGROUND	TU-11 Async DS1
TUG3 #2	
TUG3 #3	TU-11 Word 1100

RX

PAYLOAD	As per Table
MAPPING	As per Table
TUG-3 #	As per Table
LOOPBACK	STM-1 External

Check TUG-3 #1 in the RX is free of any of the alarms.
Check TUG-3 #2 & #3 sync up to a TU-11 mapping.

Subtest Number	RX TUG3 # under test	RX Mapping
148	1	TU-3 34 Mb/s
149	2	TU-11 DS1
150	3	TU-11 Word

Subtests 151 to 152 - TU11 Background Pattern Tests (DS1)

These tests check that the unit under test Transmitter can transmit an STM-1 TU11 DS1 Async payload with the correct background pattern.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU11
MAPPING	As per Table
TU	TUG3[x] TUG2[y] TU[z] As per Table
BACKGROUND PATTERN	As per Table

RX

PAYLOAD	TU11
MAPPING	As per Table
TU	Check foreground [x,y,z] and then background [m,n,p]
LOOPBACK	STM-1 External
PATTERN	As per Table

For each mapping type:
Check unit under test RX foreground for Pattern Sync.
Check unit under test RX background TUG3 for Pattern Sync.

Subtest Number	TX Foreground Mapping	RX Trib to test for Foreground Mapping	RX Trib to test for Background Mapping	EXPECTED Background Mapping	Background Pattern
151	Unframed	x=3, y=1, z=4	m=2, n=1, p=2	D4	2^9-1 PRBS
152	ESF	x=2,y=3,z=1	m=2,n=3,p=3	D4	2^15-1 PRBS

Subtest 153 AU3 POH

This subtest checks that the unit under test Transmitter can send a message in the J1 bytes and that the unit under test Receiver can receive that message.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	VC-3
MAPPING	AU-3
AU	AU3[1]

RX

PAYLOAD	VC-3
MAPPING	AU-3
AU	AU3[1]
LOOPBACK	STM-1 EXTERNAL

The following default message is sent in the J1 bytes and checked in the Receiver:

“HEWLETT-PACKARD, HP37714A PDH/SDH

FIELD TEST SET, 0000U0000 (CR) (LF)”.

NOTE The instrument & serial number will vary between instruments.

Subtest 154 AU-3 TU-2 Payload Bit Error Add & Detect

This test checks that the unit under test Transmitter can insert bit errors into the TU2 payload and that the unit under test Receiver can detect these errors.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU-2
MAPPING	AU-3
ERROR ADD	SINGLE (PAYLOAD)
AU	AU3[2]
TUG2	TUG2[1]

RX

PAYLOAD	TU-2
MAPPING	AU-3
AU	AU3[2]
TUG2	TUG2[1]
LOOPBACK	STM-1 EXTERNAL

The unit under test is allowed to gain PATTERN sync and is then gated for 3 seconds. The received Bit Error Rate is checked.

Subtest 155 AU-3 with TU-12 Payload (Floating Byte Sync)

This test checks that the unit under test Transmitter can insert bit errors into the TU12 payload and that the unit under test Receiver can detect these errors.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU-12
MAPPING	AU-3
MODE	FLOATING BYTE 2M
ERROR ADD	SINGLE (PAYLOAD)
AU	AU3[3]
TUG2	TUG2[2]
TU	TU[1]

RX

PAYLOAD	TU-12
MAPPING	AU-3
MODE	FLOATING BYTE 2M
AU	AU3[3]
TUG2	TUG2[2]
TU	TU[1]
GATING TIME	3 SECS
LOOPBACK	STM-1 EXTERNAL

The unit under test is allowed to gain PATTERN sync and is then gated for 3 seconds. The received Bit Error Rate is checked.

Subtest 156 AU-3 with TU-11 Payload (Async)

This test checks that the unit under test Transmitter can insert bit errors into the TU11 payload and that the unit under test Receiver can detect these errors.

The unit under test is reset to its SDH default state, then set up as follows:

TX

PAYLOAD	TU-11
MAPPING	AU-3
MODE	ASYNC DS1
ERROR ADD	SINGLE (PAYLOAD)
AU	AU3[1]
TUG2	TUG2[3]
TU	TU[2]

RX

PAYLOAD	TU-11
MAPPING	AU-3
MODE	ASYNC DS1
AU	AU3[1]
TUG2	TUG2[3]
TU	TU[2]
GATING TIME	3 SECS
LOOPBACK	STM-1 EXTERNAL

The unit under test is allowed to gain PATTERN sync and is then gated for 3 seconds. The received Bit Error Rate is checked.

Subtest 157 to 160 AU-3 Pattern Tests

These tests check that the unit under test Transmitter can transmit an STM-1 payload containing the correct test patterns and the unit under test Receiver can detect these patterns error free.

The unit under test is reset to its SDH default state, then setup as follows:

TX

PAYLOAD	As Per Table
MAPPING	AU-3
PATTERN	As Per Table
AU3	AU3[x]
TUG2	TUG2[y]
TU	TU[z]

RX

PAYLOAD	As Per Table
MAPPING	AU-3
PATTERN	As Per Table
AU3	AU3[x]
TUG2	TUG2[y]
TU	TU[z]
LOOPBACK	STM-1 EXTERNAL

The Receiver is first checked to have a signal present, then Pattern Sync is checked. With Single Error Add, the bit error count is measured and checked to be 1.

Subtest Number	Payload		Pattern	Error Add	Test Time	Nominal Count	x	y	z
157	VC-3	34M	PRBS23	Single	1	1	1	N/A	N/A
158	TU-2	Bulk Fld	PRBS15	Single	1	1	2	4	N/A
159	TU-12	Fl. Byte 2M	WORD_1	Single	1	1	3	5	3
160	TU-11	Async DS1	PRBS9	Single	1	1	1	6	4

NOTE WORD_1 = 1100010011110110.

NOTE Entry in italics are default fixed payload types.

Service Sheet G13 - Optical Interface Module (Options UH1, 130 and 131)

Introduction

This Service Sheet should be used when troubleshooting faults associated with the instrument OPTICAL INTERFACE Module after performing the troubleshooting described in General Service Sheet G-1. A faulty OPTICAL INTERFACE Module will normally be indicated as an OPTICAL INTERFACE Selftest failure when running the instrument selftest.

NOTE If the Optics option fitted to your instrument is Option UH1, 130 or 131, use Service Sheet G13. If the Optics option is Option USN or UKT, use Service Sheet G14.

NOTE The Optical Interface Selftest requires a fully operational SDH Module. Ensure that the instrument passes the SDH Selftest before troubleshooting Optics failure.

WARNING **The following safety precautions must be observed when servicing the optical module. The optical modules generate laser signals which can cause serious injury. The following instructions must be followed:**

Check the connector configuration of the Fibre Optic Interfaces. If these are fitted with a connector interface other than FC/PC ensure you have the correct type of connector cable.

Check for any damage to the HP 37717C Fibre Optic Interface spring-loaded aperture covers and connectors. Do not power up the instrument if in any doubt about the integrity of these connectors.

Make all connections to the HP 37717C Fibre Optic Interfaces before powering up the instrument.

CAUTION Many optical Interface problems are caused by contamination on the Optical Interface connectors or/and couplings. Always cover the ends of optical cables and connectors with protective caps when not in use.
Examine the ends of Optical Cables before use. If visible contamination is present DO NOT USE - dirt is easily transferred to the Optical Module connector which may result in permanent damage. If in doubt, the cable should be replaced or cleaned. If the Optical Interface Selftests still fail, the optical interfaces on the Module should be cleaned.
When cleaning, refer to Hewlett-Packard booklet Lightwave Connection Techniques for better Measurements HP Part Number 08703-90028.

Troubleshooting

The following Troubleshooting aim to isolate the fault to the Optical Transmitter or Receiver. Once this has been achieved, the appropriate Optical coupler can be replaced (see Service Sheet G15). If this fails to fix the fault, the complete Optical Module must be replaced (or exchanged).

Troubleshooting Procedure

If the OPTICAL INTERFACE Selftest fails, use the following procedure and accompanying selftest information to troubleshoot the fail code.

1. Check that the OPTICAL INTERFACE Tx and Rx ports are looped using a suiTable Optical cable.
2. If the Failcode indicates **Loss of Signal** then check the OPTICAL Transmitter output on a Power Meter (a procedure is given in the Performance Tests section of the Calibration Manual).
   If the OPTICAL Transmitter output signal is OK, then suspect the OPTICAL Receiver Assembly.
   If the OPTICAL Transmitter output signal is NOT OK, then suspect the OPTICAL Transmitter Assembly.
3. If the failcode indicates **No Pattern Sync,** setup another HP 37717C or equivalent STM OPTICAL Transmitter to the same Transmit Parameters as were frozen at selftest failure (see Service Sheet G2) and connect the OPTICAL output of this instrument to the OPTICAL Receiver of the faulty unit.
   Setup the Receiver parameters of the faulty unit to be the same as those in the subtest which fails (see the descriptions which follow).
   Check to see if the **No Pattern Sync** indication is still present.
   If **No Pattern Sync** indication is still present, suspect the OPTICAL Receiver Assembly.
   If **No Pattern Sync** indication is no longer present, suspect the OPTICAL Transmitter Assembly.
4. If the failcode indicates **Incorrect Errors Counted,** setup another HP 37717C or equivalent OPTICAL Transmitter to the same Transmit Parameters as were frozen at selftest failure (see Service Sheet G2) and connect the OPTICAL transmitter output of this instrument to the OPTICAL Receiver of the faulty unit.
   Setup the Receiver parameters of the faulty unit to be the same as those in the subtest which fails (see the descriptions which follow).
   Start and run an error measurement for the required time.
   Check the Error Count on the HP 37717C Results page when the measurement ends:
   If the Error Result is high or low, suspect the OPTICAL Receiver Assembly.
   If the Error Result is now OK, suspect the OPTICAL Transmitter Assembly.

Test 9 : Optical Interface Tests

Subtests 1 through 9 are applicable for the STM-1 module, tests 10 through 26 are applicable for the STM-1/STM-4 module.

Subtests 1 to 5 STM-1 Optical, Error Add and Detect

These subtests check that the unit under test Transmitter can transmit an STM-1 Optical signal and that the unit under test Receiver can receive that signal.

This test depends on an External loopback and therefore tests the Optical output and input circuitry on the Optical Interface Module.

The unit under test is reset to its SDH default state, then set up as follows:

TX

TRANSMIT SIGNAL	STM1 Optical
PATTERN	2^15-1 PRBS

RX

RECEIVE SIGNAL	STM1 Optical
PATTERN	2^15-1 PRBS
TEST TIMING	3 SECONDS
LOOPBACK	STM-1 OPTICAL

Subtest 1

Check unit under test RX for no Loss of Signal.

Subtest 2

Check the SDH register for a result of 0.

Subtest 3

Check unit under test RX is allowed to gain PATTERN sync and is then gated for 3 seconds. At the end of the gating period, the bit error count should be zero.

Subtest 4

The unit under test TX has 1E-3 error add enabled.

The unit under test RX is again allowed to gain PATTERN Sync and is gated for 3 seconds. At the end of the gating period, the bit error rate should be within the specified limits.

Subtest 5

The unit under test Transmitter is switched off. Check RX for Loss of Signal.

Subtests 10-34 STM-1 Optical Payload Error Add and Detect

NOTE Sub-tests 10 to 37 are ONLY executed if an STM-1/STM-4 optical module is fitted in the unit under test.

These sub-tests check that the unit under test transmitter can transmit an STM-1 Optical signal and the unit under test receiver can receive that signal.

The test requires an external loopback and therefore tests the output and input circuitry.

Set up

As per SDH default settings except:

TX

INTERFACE	STM-1 Optical
PATTERN	2^15-1PRBS

RX

INTERFACE	STM-1Optical
PATTERN	2^15-1 PRBS
TEST TIMING	3 seconds
LOOPBACK	STM-1 Optical

Subtest 12

The Rx is allowed to gain pattern sync and is then gated for 3 seconds. At the end of the gating period, the bit error count should be zero.

Subtest 13

The Optical Transmitter has 1E-3 error add enabled.

The RX is allowed to gain pattern sync gated for 3 seconds and checked against test limits of: MIN = 9.4E-4; MAX 1.06E-3

The Optical Transmitter is switched off for subtest 14.

Subtest 35 to 37 STM-4 Optical A1, A2, B1, B2 Defaults

These sub-tests check that the unit under test transmitter transmits the correct values for the specified overhead bytes and the unit under test receiver can detect these values.

These tests are taken from HP 37704 CARE Self Test ERS, Test 6, Subtest 35-36.

Set up

As per default settings except:

TX	
INTERFACE	STM-4 Optical
RX	
INTERFACE	STM-4 Optical
TEST	3 seconds
TIMING	
LOOPBACK	External

The unit under test is gated for 3 seconds. At the end of the gating time the received overhead bytes are checked for no errors.

Subtests 38 to 41 - STM-1 Rx Pattern Loss Detect

NOTE Subtests 38 to 40 are performed only if option US1 is fitted.

These tests check that when a particular STM-1 is transmitted it is not detected when a different STM-1 is selected on the receiver.

Set-Up

LOOPBACK	OPTICAL

Subtest 38

Set the Tx STM-1 Number to 1 and check the Receiver detects Pattern Loss when the Rx STM-1 Number is set to 2, 3 or 4.

Subtest 39

Set the Tx STM-1 Number to 2 and check the Receiver detects Pattern Loss when the Rx STM-1 Number is set to 1, 3 or 4.

Subtest 40

Sets the Tx STM-1 Number to 3 and checks the Receiver detects Pattern Loss when the Rx STM-1 Number is set to 1, 2 or 4.

Subtest 41

Sets the Tx STM-1 Number to 4 and checks the Receiver detects Pattern Loss when the Rx STM-1 Number is set to 1, 2 or 3.

Subtest 42 - STM-4 Optical MS-AIS

This test checks that the unit under test Tx can generate an MS-AIS signal and that the unit under test Rx can detect the alarm condition.

NOTE Subtest 42 is performed only if option US1 is fitted.

The unit under test is reset to its SDH default state, then set-up as follows:-

Set-Up

TX	
INTERFACE	STM-4 OPTICAL
PATTERN	ALL ONES
TEST FUNCTION	SDH ERR and ALARM
ALARM TYPE	MS-AIS
RX	
INTERFACE	STM-4 OPTICAL
PATTERN	ALL ONES
LOOPBACK	OPTICAL

Subtest 42

The unit under test Rx is allowed to gain Pattern sync. The unit under test Tx then generates the MS-AIS alarm and the alarm register is checked for MS-AIS. Finally, the alarm is cancelled and a check is made that the alarm register is cleared.

Subtest 43-STM-4 Optical MS-RDI

This test checks that the unit under test Tx can generate an MS-RDI alarm and that the unit under test Rx can detect the alarm condition.

NOTE Subtest 43 is performed only if option US1 is fitted.

The unit under test is reset to its SDH default state, then set-up as follows:

Set Up

TX

INTERFACE	STM-4 OPTICAL
TEST FUNCTION	SDH ERR and ALARM
ALARM TYPE	MS-RDI

RX

INTERFACE	STM-4 OPTICAL
LOOPBACK	OPTICAL

Subtest 43

The unit under test Rx is allowed to gain Pattern sync. The unit under test Tx then generates the MS-RDI alarm and the alarm register is checked for MS-RDI. Finally, the alarm is cancelled and a check is made that the alarm register is cleared.

Service Sheet G14 - (Options USN, UKT, 130 and 131)

Troubleshooting (Option UKT)

There are no parts that can be replaced separately in the Option UKT Module, so an exchange module must be obtained if the Selftest fails (after checking that the Optical Tx and Rx is loop and the Optical connectors are good).

Troubleshooting Procedure (Option USN)

If the Optical Interface Selftest fails, use the following procedure and accompanying Selftest information for Troubleshooting based on the fail code.

All Test Failure:

1. Check the 1310 nm Optical Tx and Rx ports are looped using a suiTable good cable.
2. Run the Optical Module Test, loop the 1550 nm Optical Tx and Rx ports using a suiTable good cable via 10 dB Optical Attenuator.

   If the Optical Module Test passes, then the 1550 nm Optical Transmitter is OK, Order an Option UKT Exchange Module and fit the 1550 nm Tx Assembly from the original Option USN Module.

   If the Optical Module Test Fails, carry out a check of the 1550 nm Optical Transmitter power output. (See Adjustments Section 3).

   If power output is good, the 1550 nm Tx Assembly is good. Order an exchange Option UKT Module and fit the 1550 nm Tx Assembly from the original Option USN module (A67).

   If the power output is bad, order an Exchange Option USN Module.

All Test Pass:

1. Run the Optical Module Test. Loop the 1550 nm Optical Tx and Rx ports using a suiTable good cable via a 10 dB Optical Attenuator.
   If the Optical Module Test fails, suspect the 1550 nm Transmitter Assembly-see Replaceable Parts in Section 4.

General Information

Due to the various options available for this module and the need to possibly test several output and input paths the tests performed have been split into four test groups:

1. STM-1 a set of tests which mainly check the STM-1 logic, electrical or optical path routing with a loopback fitted.
2. STM-4 a set of tests which check the STM-4 board control logic fully, plus optical input and output paths with a loopback fitted.
3. STM-4 a subset of the above which is intended to check the selected electrical or optical input and output path only. This group comprises, Subtests 7,8,9,19 and 20.
4. STM-1/4 optical power and frequency measurement.

The major subtests in these test groups are as follows:

Subtests 1 to 6 - test STM-1 logic and optical link over 1310 nm or 1550 nm Tx optics. Here the SDH will have been already fully tested and we need only to check the routing of the four bit 39 MHz path, from the SDH module through the Option USN/UKT/130/131 module and back. These tests are included in test group 1.

Subtests 7 to 68- test STM-4 logic and optical link over 1310 nm Tx optics. Here a comprehensive set of tests is performed in order to fully check the Option USN/UKT/130/131 modules operation, These tests are included in test group 2. For 1550 nm optics only tests in group 3 are performed.

Subtests 70 to 73 - test STM-1 logic and electrical link over binary interface. Tests 1-6 are performed over the binary interface, These tests are included in test group 1. (test 64 is reserved for additional tests).

Subtests 75 to 79 - test STM-4 electrical link over the binary interface. Test group 3 is used to check the optional electrical path.

Subtests 80 and 83 - test 1310 nm and 1550 nm optical power and frequency measurement. These tests are included in test group 4.

Subtests 84 to 99 - test 130/131 specific features only.

When testing the unit on customer premises, the self-test performed will be selected via the 'self-test' screen selection 'ALL' or module 'STM-1/4 OPTICS'.

When 'ALL' is selected it is assumed that a loopback on the 1310 nm Tx optics is fitted, tests 1 to 68 and 80 to 83 are carried out with the 1310 nm Tx optics looped back to the Rx optics. The Binary interface, if fitted, will have tests 60 to 69 performed. **No testing of 1550 nm optics is performed.**

When 'STM-1/4 OPTICS' is selected the action depends upon the module fitted, for UKT/131 the tests are as described above. For Option USN/130 a loopback on the 1550 nm optics is assumed and tests 1 to 9, 19, 20 and 80 to 85 are performed.

When testing the unit at HP (CARE testing), the action shall be as described above for the customer. The test computer must select tests 'ALL' then 'STM-1/4 OPTICS', with an optical coupler fitted, in order to fully test the dual wavelength option.

Notes Relevant To All Tests

NOTE The selection of tests available is also dependent on the SDH Option which is fitted 'A1T' or 'US1'. All tests may be performed as detailed when Option A1T is fitted, tests not applicable, when Option US1 is fitted are noted 'Not Applicable US1'. When Option US1 is fitted receive detection of Loss of Signal is not available, marked ' [N/A to US1]'.

NOTE When testing the 1550 nm optics an attenuator of 10 dBm in the loopback is required.

NOTE The optical coupler used during the CARE testing should have path losses of 6.5 ±1 dBm (1550 nm), 3.0 ±1 dBm (1310 nm).

NOTE The selftest cannot test the circuits unique to the STM-4 'through modes' or the PMP input option. External test equipment is required to test the module when using these options.

The allocation of error codes for each test is based upon the system as follows :

Test fail number = XXYYZ where,

XX = the module test number which is always 10.

YY = the subtest number in the test sequence.

Z = the type of failure as follows,

1 = loss of sync error during 1310 nm/binary interface test.

2 = various meanings, see individual tests.

3 = test result low during 1310 nm/binary interface test.

4 = test result high during 1310 nm/binary interface test.

5 = loss of sync error during 1550 nm test.

6 = various meanings, see individual tests.

7 = test result low during 1550 nm test.

8 = test result high during 1550 nm test.

Messages Displayed During Selftest

The following messages will be displayed on the equipment front panel display when selftest 10 is selected.

Option USN or 130 module fitted, no 0YH (binary interface) -

'IF RUNNING ALL TESTS, CONNECT STM-1/4 OUT (1310) TO STM1/4 IN, ELSE CONNECT STM-1/4 OUT (1550) VIA A 10 DBM ATTENUATOR TO STM-1/4 IN'

Option USN or 130 module fitted, 0YH fitted (binary interface)

'IF RUNNING ALL TESTS, CONNECT STM-1/4 OUT (1310) TO STM1/4 IN, ELSE CONNECT STM-1/4 OUT (1550) VIA A 10 DBM ATTENUATOR TO STM-1/4 IN'.

'CONNECT STM-1/4 CLOCK AND DATA OUT TO STM-1/4 CLOCK AND DATA IN'

Option UKT or 131 module fitted, no 0YH (binary interface) -

'CONNECT STM-1/4 OUT TO STM-1/4 IN'

UKT or 131 module fitted, 0YH (binary interface) -

'CONNECT STM-1/4 OUT TO STM-1/4 IN'

'CONNECT STM-1/4 CLOCK AND DATA OUT TO STM-1/4 CLOCK AND DATA IN

Subtest 1 - STM1 Link From SDH over Optics

This subtest checks that the 39 MHz four bit parallel link between the SDH Module and the optical module is functioning correctly.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-1 OPT
PATTERN	PRBS 2^15

RX:

SIGNAL	STM-1 OPT
PATTERN	PRBS 2^15
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

Subtest 1

The unit under test receiver is checked for no loss of signal.

The unit under test receiver is checked for pattern sync.

Subtests 2 to 4 - STM1 Optical Error Add and Detect

As the STM-1 signal and the path through the optical module have already been tested these subtests carry out a more detailed check of the STM-1 optical link on the USN/UKT/130/131 board.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-1 OPT
PATTERN	PRBS 2^15

RX:

SIGNAL	STM-1 OPT
PATTERN	PRBS 2^15

TX:

TEST FUNCTION	ERROR & ALARM
ERROR ADD LOCATION	PAYLOAD
ERROR ADD TYPE	(BIT)
ERROR ADD RATE	1E-4

RESULTS:

TEST TIMING	3 SECONDS
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

Subtest 2

The unit under test receiver is checked for no LOF, OOF and LOP.

Subtest 3

The unit under test receiver is allowed to gain pattern sync and is then gated for 3 seconds. At the end of the gating period, the bit error rate should be within the limits.

Subtest 4

The unit under test transmitter is switched off for A1T or LOF set for US1. Check the receiver for loss of signal.

The unit under test receiver is checked to ensure LOF, OOF and LOP occurred.

Subtests 5 and 6 - STM1 Optical Stress Test

NOTE Not Applicable US1.

This subtest checks that when a block of zeros is added to the unit under test transmitter, the unit under test receiver can frame sync and that Out Of Frame is not detected during a gating period.

The unit under test is reset to its default state and then set up as follows:

TX:	
SIGNAL	STM-1 OPT
PATTERN	PRBS 2^15
RX:	
SIGNAL	STM-1 OPT
PATTERN	PRBS 2^15
TX:	
TEST FUNCTION	STRESS TEST
STRESSING PATTERN	ALL ZEROS
BLOCK LENGTH	12 BYTES
RESULTS:	
TEST TIMING	3 SECONDS
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

Subtest 5

The unit under test transmit and receive are set up and the receive is allowed to gain frame sync, the receiver is checked to ensure it has frame sync (no OOF, LOF).

Subtest 6

The start command is sent and the unit under test is gated for 3 seconds. At the end of the gating period, the history register is checked to ensure Out of Frame (OOF) did not occur.

Subtests 7 to 18 - STM-4 Optical Error Add and Detect

These subtests check that the unit under test transmitter can transmit an STM-4 Optical signal and that the unit under test receiver can receive that signal. This test depends on an external loopback and therefore tests the Optical output and input circuitry on the USN/UKT/130/131 module.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT STM1#1
STM under test	PRBS 2^15
PATTERN	

RX:

SIGNAL	STM-4 OPT
STM under test	STM1#1
	PRBS 2^15
PATTERN	

TX:

TEST FUNCTION	ERROR & ALARM
ERROR ADD LOCATION	PAYLOAD
ERROR ADD TYPE	(BIT)
ERROR ADD RATE	1E-4

RESULTS:

TEST TIMING	3 SECONDS
LOOPBACK	OPTICAL 1310 or
	OPTICAL 1550

Subtest 7

Select STM1#1 under test for transmit and receive, the unit under test receiver is checked for no loss of signal.

The unit under test receiver is checked to ensure no LOF, OOF and LOP occurred.

Subtest 8

The unit under test receiver is allowed to gain pattern sync and is then gated for 3 seconds. At the end of the gating period, the bit error rate should be within specified limits.

Subtest 9

The unit under test transmitter is switched off for A1T or LOF set for US1. Check the receiver for loss of signal.

The unit under test receiver is checked to ensure LOF, OOF and LOP occurred.

Subtest 10 - 12

Same as for 7 - 9 but STM1#2 selected, only 1310 tested.

Subtest 13 - 15

Same as for 7 - 9 but STM1#3 selected, only 1310 tested.

Subtest 16 - 18

Same as for 7 - 9 but STM1#4 selected.

Subtests 19 and 20 - STM-4 Optical A1, A2, B1 and B2 Defaults

These subtests check that the unit under test transmitter transmits the correct values for the specified overhead bytes and the unit under test receiver can detect these values.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
STM under test	STM1#1

RX:

SIGNAL	STM-4 OPT
STM under test	STM1#1

RESULTS:

TEST TIMING	3 SECONDS
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

Subtest 19

The unit under test is allowed to gain frame and pointer sync and is then gated for 3 seconds, the received overhead bytes are then checked for sync. Note that STM-4 frame sync depends on both LOF and OOF alarms being inactive.

The B1 errors = 0 is checked.

Subtest 20

The B2 errors = 0 are then checked (note sync check is not repeated).

Subtest 21 - STM-4 Optical B2 Error Add and Detect

NOTE Not Applicable US1.

This subtest checks that the unit under test transmitter can insert errors into the B2 overhead byte and the unit under test receiver can detect these errors.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
STM under test	STM1#1

RX:

SIGNAL	STM-4 OPT
STM under test	STM1#1

TX:

TEST FUNCTION	ERROR & ALARM
ERROR ADD LOCATION	OVERHEAD
ERROR ADD TYPE	MS B2 BIP
ERROR ADD RATE	1E-4

RESULTS:

TEST TIMING	3 SECONDS
LOOPBACK	OPTICAL 1310

Subtest 21

The unit under test receiver is allowed to gain frame sync and is then gated for 3 seconds. At the end of the gating period, sync should have been achieved and the bit error rate should be within the limits specified.

Subtests 22 to 25 - STM-4 Clock Recovery tests

NOTE These tests form part of the USN selftest.

NOTE Not Applicable US1.

These subtests check the clock recovery circuit of both the receiver and transmitter.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4
STM UNDER TEST	STM1#1

RX:

SIGNAL	STM-4
STM UNDER TEST	STM1#1

Subtest 22

The unit under test is checked for LOS.

The unit under test is checked for no OOF or LOP.

Subtest 23

The transmitter is switched from electrical to optical and the unit under test checked for no OOF or LOP.

Subtest 24

The receiver is switched from optical to electrical and the unit under test checked for no OOF or LOP.

Subtest 25

Both the receiver and transmitter are switched from electrical to optical and the unit under test is checked for no OOF or LOP.

Subtests 26 to 27 - STM-4 Optical section Overhead, Overwrite and Detect (RX STM1 not under test)

NOTE Not Applicable to Option US1.

These subtests check that the STM-4 multiplexer can over write accessible section overhead bytes with 0A5H, followed by 05AH and that the receiver can detect these patterns. The ODL processor transmits the over-write data via the ODL link and the multiplexer over-writes the transport overhead bytes in STM-1 number 1. The modified overhead is verified by reading it back from the STM-4 receiver, the expected value of E2 is specified as this changes as the section overhead changes.

All section overhead bytes which can be modified, except A1, A2, B1, B2, H1, H2 and H3, are tested.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
STM under test	STM1#2

RX:

SIGNAL	STM-4 OPT
STM under test	STM1#2

TX:

SECTION OVERHEAD	See Table (col2)
OVERHEAD BYTE - PATTERN	See Table (col3)
LOOPBACK	OPTICAL 1310

Subtest 26

The modifiable Section Overhead bytes are set to the pattern shown. The unit under test is then checked for frame sync and that the bytes were received correctly. Note that frame sync depends on both LOF and OOF alarms being inactive. .

Subtest Number	Columns	Tx/Rx OH Byte pattern	E2
26 - 1310	1,4 and 7	10100101b	c4h

Subtest 27

Subtest 26 is repeated but with data 0x55.

Subtest Number	Columns	Tx/Rx OH Byte pattern	E2
27 - 1310	1,4 and 7	01011010b	3bh

Subtests 28 to 33 - STM-4 Optical Demux Section Overhead Extraction

NOTE Not Applicable US1.

These subtests check that the STM-4 demultiplexer can extract the transport overhead of STM-1 number 1, inserting and extracting via the ODL processor.

All transport overhead bytes which can be modified, except (A1, A2), are tested. The expected value of E2 is specified as this changes as the section overhead changes.

Unequipped is invoked to give known values for H1, H2 and H3.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
STM under test	STM1#1

RX:

SIGNAL	STM-4 OPT
STM under test	STM1#1

TX:

SECTION OVERHEAD	See Table (col2)
OVERHEAD BYTE -	
PATTERN	See Table (col3)
ALARM	See Table (col4)
LOOPBACK	OPTICAL 1310

Subtest 28

The modifiable Section Overhead bytes are set to the pattern shown below and an alarm should be generated as detailed in the Table. The unit under test is checked for frame sync and then the receiver checks that the STM-1 'number 1' bytes, including H1, H2 & H3, were received correctly. Note that frame sync depends on both LOF and OOF alarms being inactive.

Subtest Number	Column	Tx/Rx OH Byte	Tx Alarm	Rx pattern H1/H2, H3,E2 hex
28-1310	1,4,7	10100101b	PathAIS	FFFF, FF,00

Subtest 29

Test as subtest 28 but with columns 2,5 and 8.

Subtest Number	Column	Tx/Rx OH Byte	Tx Alarm	Rx pattern H1/H2, H3,E hex
29-1310	2,5,8	10100101b	PathAIS	FFFF, FF,00

Subtest 30

Test as subtest 28 but with columns 3,6 and 9.

Subtest Number	Column	Tx/Rx OH Byte	Tx Alarm	Rx pattern H1/H2, H3,E hex
30-1310	3,6,9	10100101b	PathAIS	FFFF, FF,00

Subtest 31

Test as subtest 28 but with TX/RX Pattern 0x55.

Subtest Number	Column	Tx/Rx OH Byte	Tx Alarm	Rx pattern H1/H2, H3,E2 hex
31-1310	1,4,7	01011010b	PathUnequ	6800,00,00

Subtest 32

Test as subtest 31 but with columns 2,5 and 8.

Subtest Number	Column	Tx/Rx OH Byte	Tx Alarm	Rx pattern H1/H2, H3,E hex
32-1310	2,5,8	01011010b	PathUnequ	93FF,00,00

Subtest 33

Test as subtest 31but with columns 3,6 and 9.

Subtest Number	Column	Tx/Rx OH Byte	Tx Alarm	Rx pattern H1/H2, H3,E hex
33-1310	3,6,9	01011010b	PathUnequ	93FF,00,00

Subtests 34 to 57 - STM-4 Optical Section Overhead RAM

NOTE Not Applicable US1.

These subtests check that the unit under test transmitter can modify specified section overhead bytes with 0A5H, followed by 05AH and that the receiver can detect these patterns. The Section Overhead area of the RAM is tested.

All setTable section overhead bytes are tested, except A1, A2. Except when STM1#1 cols 147 are under test (34 and 46) only the RSOH is checked for the pattern, the MSOH is tested for 00 and the expected value of E2.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL STM-4 OPT

RX:

SIGNAL STM-4 OPT

TX:

STM-1 UNDER TEST See Table (col2)
SECTION OVERHEAD See Table (col3)
OVERHEAD BYTE -
PATTERN See Table (col4)
ALARM See Table (col5)

RX:

STM-1 UNDER TEST	See Table (col2)
SOH MONITOR	See Table (col3)
OVERHEAD BYTE - PATTERN	See Table (col4)
LOOPBACK	OPTICAL 1310

Subtest 34

The modifiable Section Overhead bytes are set to the pattern detailed and the unit under test is checked for frame sync. The receiver then checks that the bytes were received correctly, as per the Table. Note that frame sync depends on both LOF and OOF alarms being inactive.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E2	Tx Alarm
34-1310	04 --- 01	147	10100101b, c4h	Off

Subtest 35

As for subtest 34 except columns 2,5 and 8.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
35-1310	04 --- 01	258	10100101b, 7dh	Off

Subtest 36

As for subtest 34 except columns 3,6 and 9.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
36-1310	04 --- 01	369	10100101b, 7dh	Off

Subtest 37

As for subtest 34 except Rx channel 2.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
37-1310	04 --- 02	147	10100101b, 61h	Off

Subtest 38

As for subtest 37 except columns 2,5 and 8.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
38-1310	04 --- 02	258	10100101b, 7dh	Off

Subtest 39

As for subtest 37 except columns 3,6 and 9.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
39-1310	04 --- 02	369	10100101b, 7dh	Off

Subtest 40

The modifiable Section Overhead bytes are set to the pattern detailed and the unit under test is checked for frame sync. The receiver then checks that the bytes were received correctly, as per the Table. Note that frame sync depends on both LOF and OOF alarms being inactive.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
40-1310	04 --- 03	147	10100101b, 61h	Off

Subtest 41

As for subtest 40 except columns 2,5 and 8.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
41-1310	04 --- 03	258	10100101b, 7dh	Off

Subtest 42

As for subtest 40 except columns 3,6 and 9 .

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
42-1310	04 --- 03	369	10100101b, 7dh	Off

Subtest 43

As for subtest 40 except Tx-1 and RX-4.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
43-1310	01 --- 04	147	10100101b, 61h	Off

Subtest 44

As for subtest 43 except columns 2,5 and 8.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
44-1310	01 --- 04	258	10100101b, 7dh	Off

Subtest 45

As for subtest 43 except columns 3,6 and 9.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
45-1310	01 --- 04	369	10100101b, 7dh	Off

Subtest 46

The modifiable Section Overhead bytes are set to the pattern detailed and the unit under test is checked for frame sync. The receiver then checks that the bytes were received correctly, as per the Table. Note that frame sync depends on both LOF and OOF alarms being inactive.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E2	Tx Alarm
46-1310	04 --- 01	147	01011010b, 3bh	Path Unequ

Subtest 47

As for subtest 46 except columns 2,5 and 8.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
47-1310	04 --- 01	258	01011010b, 7dh	Path Unequ

Subtest 48

As for subtest 46 except columns 3,6 and 9.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
48-1310	04 --- 01	369	01011010b, 7dh	Path Unequ

Subtest 49

As for subtest 46 except RX-2.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
49-1310	04 --- 02	147	01011010b, 61h	Path Unequ

Subtest 50

As for subtest 49 except columns 2,5 and 8.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
50-1310	04 --- 02	258	01011010b, 7dh	Path Unequ

Subtest 51

As for subtest 49 except columns 3,6 and 9.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
51-1310	04 --- 02	369	01011010b, 7dh	Path Unequ

Subtest 52

The modifiable Section Overhead bytes are set to the pattern detailed and the Unit Under Test is checked for frame sync. The receiver then checks that the bytes were received correctly, as per the Table. Note that frame sync depends on both LOF and OOF alarms being inactive.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
52-1310	04 --- 03	147	01011010b, 61h	Path Unequ

Subtest 53

As for subtest 52 except columns 2,5 and 8.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
53-1310	04 --- 03	258	01011010b, 7dh	Path Unequ

Subtest 54

As for subtest 52 except columns 3,6 and 9.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
54-1310	04 --- 03	369	01011010b, 7dh	Path Unequ

Subtest 55

As for subtest 52 except Tx-1, RX-4.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
55-1310	01 --- 04	147	01011010b, 61h	Path Unequ

Subtest 56

As for subtest 55 except columns 2,5 and 8.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
56-1310	01 --- 04	258	01011010b, 7dh	Path Unequ

Subtest 57

As for subtest 55 except columns 3,6 and 9.

Subtest Number	STM-1 test TX -- RX	Col	Tx/Rx OH Byte pat, E byte	Tx Alarm
57-1310	01 --- 04	369	01011010b, 7dh	Path Unequ

Subtests 59 and 60 - STM-4 Optical Frame Sync/Loss

NOTE Not Applicable US1.

These subtests check that the Out Of Frame and Loss Of Frame conditions do not occur unexpectedly.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
STM1 under test	STM1#1

RX:

SIGNAL	STM-4 OPT
STM1 under test	STM1#1

TX:

ALARM	MS AIS
LOOPBACK	OPTICAL 1310

Subtest 59

The alarm register is then checked for no OOF or LOF.

Subtest 60

The history register is reset and the unit under test transmitter sends 3 in 4 framing patterns in error. The history register is then checked for no OOF or LOF.

Subtests 61 to 63 - STM-4 Optical MS AIS

These tests check that the unit under test Transmitter can generate an MS AIS signal and that the unit under test Receiver can detect the alarm condition.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
STM1 under test	STM1#1

RX:

SIGNAL	STM-4 OPT
STM1 under test	STM1#1
LOOPBACK	OPTICAL 1310

Subtest 61

The unit under test receiver is allowed to gain pattern sync.

Subtest 62

The unit under test transmitter then generates MS AIS alarm and the receiver alarm register is checked.

Subtest 63

The unit under test transmitter is set to produce no MS AIS alarm and the alarm register is reset. The receiver is checked for no MS AIS alarm.

Subtests 64 to 66 - STM-4 Optical MS FERF

These tests check that the unit under test Transmitter can generate an MS FERF alarm and that the unit under test Receiver can detect the alarm condition.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
STM1 under test	STM1#1

RX:

SIGNAL	STM-4 OPT
STM1 under test	STM1#1
LOOPBACK	OPTICAL 1310

Subtest 64

The unit under test receiver is allowed to gain pattern sync.

Subtest 65

The unit under test transmitter then generates MS FERF alarm and the receiver alarm register is checked.

Subtest 66

The unit under test transmitter is set to produce no MS FERF alarm and the alarm register is reset. The receiver is checked for no MS FERF alarm.

Subtest 67 - STM-0 Link From SDH over Optics

This subtest checks that the STM-0 optical link link between the SDH A3R Module and the 130/131 optical module is functioning correctly. This test is only applicable if A3R and 130/131 are fitted.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-0 OPT
PATTERN	PRBS 2^15

RX:

SIGNAL	STM-0 OPT
PATTERN	PRBS 2^15
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

Subtest 67

The unit under test receiver is checked for no loss of signal.

The unit under test receiver is checked for pattern sync.

Subtests 68 to 69 - STM-0 Optical Error Add and Detect

As the STM-0 signal and the path through the optical module have already been tested these subtests carry out a more detailed check of the STM-0 optical link on the 130/131 board. This test is only applicable if A3R and 130/131 are fitted.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-0 OPT
PATTERN	PRBS 2^15

RX:

SIGNAL	STM-0 OPT
PATTERN	PRBS 2^15

TX:

TEST FUNCTION	ERROR & ALARM
ERROR ADD LOCATION	PAYLOAD
ERROR ADD TYPE	(BIT)
ERROR ADD RATE	1E-4

RESULTS:

TEST TIMING	3 SECONDS
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

Subtest 68

The unit under test receiver is checked for no LOF, OOF and LOP.

Subtest 69

The unit under test receiver is allowed to gain pattern sync and is then gated for 3 seconds. At the end of the gating period, the bit error rate should be within the limits.

Subtest 70 - STM1 Link From SDH over Binary Interface

This subtest checks that the 39 MHz four bit parallel link between the SDH Module and the binary interface is functioning correctly.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-1 BINARY
PATTERN	PRBS 2^15

RX:

SIGNAL	STM-1 BINARY
PATTERN	PRBS 2^15
LOOPBACK	BINARY I/F

Subtest 70

The unit under test receiver is checked for no loss of signal.

The unit under test receiver is checked for pattern sync.

Subtests 71 to 73 - STM1 Binary Interface Error Add and Detect

As the STM-1 signal and the path through the binary interface have already been tested these subtests carry out a more detailed check of the STM-1 binary link on the USN/UKT/130/131 board.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-1 BINARY
PATTERN	PRBS 2^15

RX:

SIGNAL	STM-1 BINARY
PATTERN	PRBS 2^15

TX:

TEST FUNCTION	ERROR & ALARM
ERROR ADD LOCATION	PAYLOAD
ERROR ADD TYPE	(BIT)
ERROR ADD RATE	1E-4

RESULTS:

TEST TIMING	3 SECONDS
LOOPBACK	BINARY I/F

Subtest 71

The unit under test receiver is checked for no LOF, OOF and LOP.

Subtest 72

The unit under test receiver is allowed to gain pattern sync and is then gated for 3 seconds. At the end of the gating period, the bit error rate should be within the limits specified.

Subtest 73

The unit under test transmitter is switched off for A1T or LOF set for US1. Check the receiver for loss of signal.

The unit under test receiver is checked to ensure LOF, OOF, LOP and pattern sync loss occurred.

Subtests 75 to 77 - STM-4 BINARY Interface Error Add and Detect

These subtests check that the unit under test transmitter can transmit an STM-4 signal via the binary interface and that the unit under test receiver can receive that signal. This test depends on an external loopback and therefore tests the binary output and input circuitry on the USN/UKT/130/131 module.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 BINARY
STM1 under test	STM1#1
PATTERN	PRBS 2^15

RX:

SIGNAL	STM-4 BINARY
STM1 under test	STM1#1
PATTERN	PRBS 2^15

TX:

TEST FUNCTION	ERROR & ALARM
ERROR ADD LOCATION	PAYLOAD
ERROR ADD TYPE	(BIT)
ERROR ADD RATE	1E-4

RESULTS:

TEST TIMING	3 SECONDS
LOOPBACK	BINARY I/F

Subtest 75

The unit under test receiver is checked for no loss of signal.

The unit under test receiver is checked to ensure no LOF, OOF and LOP occurred.

Subtest 76

The unit under test receiver is allowed to gain pattern sync and is then gated for 3 seconds. At the end of the gating period, the bit error rate should be within the limits specified.

Subtest 77

The unit under test transmitter is switched off for A1T or LOF is set for US1. Check the receiver for loss of signal.

The unit under test receiver is checked to ensure LOF, OOF and LOP occurred.

Subtests 78 and 79 - STM-4 BINARY Interface A1, A2, B1 and B2 Defaults

These subtests check that the unit under test transmitter transmits the correct values for the specified overhead bytes and the unit under test receiver can detect these values.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 BINARY
STM1 under test	STM1#2

RX:

SIGNAL	STM-4 BINARY
STM1 under test	STM1#2

RESULTS:

TEST TIMING	3 SECONDS
LOOPBACK	BINARY I/F

Subtest 78

unit under test is allowed to gain frame and pointer sync and is then gated for 3 seconds, the received overhead bytes are then checked for sync. Note that STM-4 frame sync depends on both LOF and OOF alarms being inactive.

Check the B1 errors = 0.

Subtest 79

The B2 errors are then checked (note sync check is not repeated).

Subtest 80 - STM1 Optical Power Measurement

This test checks the optical power measurement circuit on the module at 155 MHz receive rate. The paths and transmitter / receiver have already been fully tested.

NOTE It is important that all optics used for the loopback have been thoroughly cleaned in order to avoid any excessive external power loss which may cause the test to fail.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-1 OPT
PATTERN	PRBS 2^15

RX:

SIGNAL	STM-1 OPT
PATTERN	PRBS 2^15

RESULTS:

TEST TIMING	2 SECONDS
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

Subtest 80

The unit under test receiver is allowed to gain sync/pattern sync and then the optical power is measured after 2 seconds. At the end of the measurement period, the power level should be within the limits specified.

Subtest 81 - STM-4 Optical Power Measurement

This test checks the optical power measurement circuit on the module at 620 MHz receive rate. The paths and transmitter / receiver have already been fully tested.

NOTE It is important that all optics used for the loopback have been thoroughly cleaned in order to avoid any excessive external power loss which may cause the test to fail.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
PATTERN	PRBS 2^15

RX:

SIGNAL	STM-4 OPT
PATTERN	PRBS 2^15

RESULTS:

TEST TIMING	2 SECONDS
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

Subtest 81

The unit under test receiver is allowed to gain sync/pattern sync and then the optical power is measured after 2 seconds. At the end of the measurement period, the power level should be within the limits specified.

Subtest 82 - STM1 Frequency Measurement

This test checks the frequency measurement circuit on the module at 155 MHz receive rate. The paths and transmitter / receiver have already been fully tested.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
PATTERN	PRBS 2^15

RX:

SIGNAL	STM-4 OPT
PATTERN	PRBS 2^15

RESULTS:

TEST TIMING	3 SECONDS
LOOPBACK	OPTICAL 1310

Subtest 82

The unit under test receiver is allowed to gain sync/pattern sync and then the frequency is measured. At the end of the measurement period, the frequency should be within the limits specified. LOS is not applicable to US1.

Subtest 83 - STM-4 Frequency Measurement

This test checks the frequency measurement circuit on the module at 620 MHz receive rate. The paths and transmitter / receiver have already been fully tested.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
STM1 under test	STM1#4
PATTERN	PRBS 2^15

RX:

SIGNAL	STM-4 OPT
STM1 under test	STM1#4
PATTERN	PRBS 2^15

RESULTS:

TEST TIMING	3 SECONDS
LOOPBACK	OPTICAL 1310

Subtest 83

The unit under test receiver is allowed to gain pattern sync and then the frequency is measured. At the end of the measurement period, the frequency should be within the limits specified. LOS is not applicable to US1.

130/131 Tests

Subtests 84 to 85 - STM-4 Optical SOH Error Add

NOTE Not Applicable to Options USN, UKT and US1.

These subtests check that the unit under test transmitter can insert errors into various overhead bytes and the unit under test receiver can detect these errors.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
TEST FUNCTION	ERROR & ALARM
ERROR ADD TYPE	B1, B2, A1A2, FEBE
ERROR ADD RATE	As per Table

RX:

SIGNAL	STM-4 OPT
LOOPBACK	OPTICAL 1310

RESULTS:

TEST TIMING	3 SECONDS

Subtest 84

Errors are inserted into the MS B2 bytes. The unit under test receiver is allowed to gain frame sync and is then gated for 3 seconds. At the end of the gating period the bit error count is checked against the limits.

Subtest 85

The test is repeated for other bytes in the SOH. The limits are specified in the Table.

Subtest No.	Error Rate	Byte tested	Error count	
			min.	max
85 - 1310	1 in 4	Frame A1A2	287952	288048
85 - 1310	1E-4	RS BIP (B1)	451006	451010
85 - 1310	1E-4	MS-FEBE	180305	180411

Subtest 86 - STM-4 Optical Stress Test

NOTE Not Applicable to Options USN and UKT.

This subtest checks that when a block of zeros is added to the unit under test transmitter, the unit under test receiver can frame sync and that Out Of Frame is not detected during a gating period.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
TEST FUNCTION	STRESS TEST
STRESSING PATTERN	ALL ZEROS
BLOCK LENGTH	9 BYTES (ITU G.958)

RX:

SIGNAL	STM-4 OPT
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

The unit under test transmit and receive are set up and the receive is allowed to gain frame sync, the receiver is checked to ensure it has frame sync (no OOF, LOF).

The unit under test is gated for 3 seconds. At the end of the gating period, the history register is checked to ensure Out of Frame (OOF) did not occur.

Subtest 87 - STM4 Optical Loss of Signal

NOTE Not Applicable to Options USN and UKT.

This tests checks that the unit under test Receiver can detect Loss Of Signal. An external STM1 loopback is used.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 OPT
ALARM	LOS

RX:

SIGNAL	STM-4 OPT
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

The unit under test is checked for frame sync.

Loss of frame is generated by setting the unit under test transmitter to STM1 electrical and the receiver is checked for loss of signal.

The alarm is cleared by setting the unit under test transmitter to optical and the receiver is checked for no loss of signal.

Subtest 88 - STM4 Binary Loss of Signal

NOTE Not Applicable to Options USN, UKT and US1.

This tests checks that the unit under test Receiver can detect Loss Of Signal. An external STM1 loopback is used.

The unit under test is reset to its default state and then set up as follows:

TX:

SIGNAL	STM-4 BINARY
ALARM	LOS

RX:

SIGNAL	STM-4 BINARY
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

The unit under test is checked for frame sync.

Loss of frame is generated by setting the unit under test transmitter to STM1 electrical and the receiver is checked for loss of signal.

The alarm is cleared by setting the unit under test transmitter to binary and the receiver is checked for no loss of signal.

The alarm is cleared and the unit under test receiver checked for no loss of signal.

Subtest 89 - STM-4c POH

NOTE Not Applicable to Options USN and UKT.

This subtest checks that the unit under test Transmitter can send a message in the J1 bytes and that the unit under test Receiver can receive that message.

The unit under test is reset to its SDH default state, then set up as follows:

TX

SIGNAL	STM-4c
TEST PATTERN	J1

RX

SIGNAL	STM-4c
LOOPBACK	OPTICAL 1310 or OPTICAL 1550

The following default message is sent in the J1 bytes.

HP3771xx COMMUNICATIONS PERFORMANCE ANALYZER

GB00000001 (CR) (LF)

The received bytes are checked for any errors in reception.

NOTE The instrument number and serial number will vary between instruments.

Sub-Tests 90 to 93 - STM-4c Pattern Tests

NOTE Not Applicable to Options USN and UKT.

These tests check that the unit under test Transmitter can transmit an STM-4c payload containing the correct test patterns and that the unit under test Receiver can detect these patterns error free.

The unit under test is reset to its SDH default state, then set up as follows:

TX:

SIGNAL	STM-4c
PATTERN	As per Table

RX:

SIGNAL	STM-4c
LOOPBACK	OPTICAL 1310

Subtest 90 - 93

For each of the patterns below the unit under test is checked for pattern sync and then a single error is added and the bit error rate counted.

Subtest Number	Pattern	Error Add	Test Time (secs)	Nominal count
90	2^{23}-1PRBS	Single	1	1
91	2^{15}-1PRBS	Single	1	1
92	WORD_1*	Single	1	1
93	2^{9}-1PRBS	Single	1	1

Subtests 94 to 95 - Frequency Offset Pointer Movements

NOTE Not Applicable to Options USN, UKT and US1.

These tests check that the unit under test can generate and detect frequency offset pointer movements and that no errors or major alarms are generated.

This test is *NOT* intended to check the accuracy of frequency offset pointer moves.

The unit under test is reset to its SDH default state. Then setup as follows:

TX:

PAYLOAD STM-4c
OFFSET As per Table

RX:

PAYLOAD STM-4c
LOOPBACK OPTICAL 1310

RESULTS:

TEST TIMING 3 SECONDS

Subtest 94

The frequency offset is set to +100 ppm and the unit under test checked for errors not present.

Subtest 95

The frequency offset is measured and checked against limits . The frequency offset is then set to -100 ppm and the test repeated.

Subtest No.	Implied VC Offset		
	Nominal	min (-5 ppm)	max (+5 ppm)
95	+100.00 ppm	+95.00 ppm	+105.00 ppm
	-100.00 ppm	-105.00 ppm	-95.00 ppm

Subtest 96 - STM4 Background Payloads

NOTE Not Applicable to Options USN and UKT.

These tests check the fixed values of the background payload of the STM-4 signal.

The unit under test is reset to its SDH default state. Then setup as follows:

TX:

SIGNAL	STM-4 OPT
PATTERN	2^{15}-1 PRBS
STM under test	STM1#2

RX:

SIGNAL	STM-4 OPT
USER WORD	0001000100010001
STM under test	STM1#3
LOOPBACK	OPTICAL 1310

Subtest 96

The unit under test is checked for pattern sync.

The unit under test is checked for no errors.

Subtest 97 - STM4 Foreground Payloads

NOTE Not Applicable to Options USN and UKT.

These tests check the foreground payload of the STM-4 signal.

The unit under test is reset to its SDH default state. Then setup as follows:

TX:

SIGNAL	STM-4 OPT
PAYLOAD	AU4
BACKGROUND	AS FG
PATTERN	2^{15}-1 PRBS
STM UNDER TEST	STM1#3

RX:

SIGNAL	STM-4 OPT
PAYLOAD	AU4
PATTERN	2^{15}-1 PRBS
STM UNDER TEST	STM1#1,2,3,4
LOOPBACK	OPTICAL 1310

Subtest 97

For each STM-1 the unit under test is checked for pattern sync, a single error is added and the bit error rate counted.

Subtest 98 - STM-4 Thru Mode tests

NOTE Not Applicable to Options USN and UKT.

This test checks the unit under test THRU Mode circuitry. A special function provides loopback of received data.

The unit under test is set to its SDH default state. Then setup as follows:

TX:

MODE STM-4 THRU

Special Function to select TEST Mode in 'LoopThru' LCA

RX:

Special Function to check for H4 Framing Status

Subtest 98

The H4 framing status is checked.

Subtest 99 - DCC Port Tests

NOTE Not Applicable to Options USN and UKT.

These tests check that the Datacomm interface is functioning. As both the Drop and Insert DCC functions require a clock from the module, an internal loopback has been provided for selftest. The test uses an external Datacomm Loopback. A special function on the ODL processor is invoked for this test.

External Datacomm Loopback is used.

The unit under test is reset to its default state (panel 0), then set up as follows:

TX

STM-4
DCC INSERT
REGEN DCC or MULT DCC

RX

STM-4
DCC DROP
REGEN DCC or MULT DCC

Other
Loopback (DCC Data) External
Loopback (DCC CLOCK) Internal

Subtest 99

The ODL processor is checked by transmitting a known pattern in each transmit SOH and POH channel and checking that the pattern can be received in the corresponding receive channel. Each channel is tested in sequence.

A special test function on the ODL processor checks that the RSOH or MSOH can be Dropped and Inserted.

Service Sheet G15 - Jitter Transmitter and Receiver Modules

Introduction

This Service Sheet should be used when troubleshooting faults associated with the instrument Jitter Transmitter & Receiver Modules after performing the troubleshooting described in General Service Sheet G1. A faulty Jitter Transmitter or Receiver Module will normally be indicated as a Jitter Selftest failure when running the instrument selftest.

NOTE If the instrument is fitted with Transmit Only or Receive Only options, then some of the selftest subtests will not be run, see the following descriptions for more information.

NOTE The PDH section of the Jitter Selftest requires a fully operational PDH Module. The SDH section of the Jitter Selftest requires a full operational SDH Module Electrical and Optical if fitted. Ensure that the instrument passes both PDH and SDH Selftests before Troubleshooting Selftest failure.

The following troubleshooting aims to isolate the fault to either the Jitter Transmit Board Assembly on the Jitter Transmitter Module or the Jitter Receive Board Assembly on the Jitter Receiver Module. Once the faulty board assembly has been located it should be replaced using the Replacement Procedures section in this Manual. The correct part to order will be found in the Replaceable Parts section in this Manual.

NOTE If SDH Jitter Receiver Modules (double width) are on the Exchange Program.

2M Wander Ref In Troubleshooting

A fault in the 2M Wander Reference Input stages of the Jitter Receiver Module will be indicated by failure of the relevant Performance Test in the Calibration Manual.

If the instrument display indicates “No Reference Input” or similar message, then check the on-board fuse on the Jitter Receiver Board using an ohmmeter. If this fuse is blown it may be replaced using the part number from the Replaceable Parts Section in this Manual. After replacement, rerun the failing Performance Test to verify repair. The on-board fuse is identified as an in-line, two-wire, through-hole type normally coloured green and approximately 7 mm x 2 mm diameter. The rating is stamped on the fuse body.

Troubleshooting Procedure

If the Jitter Selftest fails, use the following procedure and accompanying selftest information to troubleshoot the fail code.

1. Check that the correct ports have been looped on the Modules-see Service Sheet G2.
2. Carry out the Jitter Transmitter Calibration as described in the Adjustments section of this Manual.

If the Jitter Transmitter Calibration still can not be made to pass, suspect a fault on the JITTER TRANSMITTER Assembly.

If the JITTER TRANSMITTER Calibration is OK, and the selftest still fails, carry out the automatic Jitter Receiver Performance Tests as described in the Calibration Manual.

NOTE If Optical Jitter Receiver is fitted, the STM-1 and STM-4 Recovered Clocks need to be set up before running Jitter Rx Calibration (see section 3).

CAUTION If Jitter RX Calibration encounters a problems, (i.e. cables missing or Recovered Clock maladjusted) no message will be displayed-the instrument will simply freeze until the problem is rectified.

If the Jitter Selftest still fails, or the calibration will not complete, suspect a fault on the JITTER RECEIVER Assembly. If the Self Test failcode indicates an Optical failure check the Optical Adaptor as below before changing the Module.

CAUTION Many Optical Interface problems are caused by contamination on the Optical Interface connectors or/and couplings. Always cover the ends of optical cables and connectors with protective caps when not in use.
Examine the ends of Optical Cables before use. If visible contamination is present DO NOT USE-dirt is easily transferred to the Optical Module connector which may result in permanent damage. If in doubt, the cable should be replaced or cleaned. If the Optical Interface Selftests still fail, the optical interfaces on the Module should be cleaned.
When cleaning, refer to Hewlett-Packard booklet Lightwave Connection Techniques for better Measurements HP Part Number 08703-90028.

Test 14 - Jitter Tests

The jitter self tests are grouped into three main test sections to allow for varying combinations of functionality, these are:

- Jitter Generator Module Present Only
- Jitter Receiver Module Present Only
- Both Jitter Modules Present

When only one jitter module is present only the test section applicable to that module is performed. When both modules are present all three test sections are performed.

An extra test is included in the first section which will be performed *only* when an SDH module is fitted in the unit under test.

140M and 8M tests will not be performed when option 110 is present.

Jitter Generator Only

Subtests 1 to 10

These tests check that the jitter generator module can generate jitter sufficient to cause errors in the PDH receiver, and that jitter generated below that level causes no errors.

An external loopback PDH Tx to Rx is used.

The unit under test is reset to its default SDH state and then setup as follows:

Test Timing	3 seconds
Loopback	PDH External
Clock Rate	See Table below
Clock Source	Jitter Generator
PDH Pattern	PRBS23
Jitter Amplitude	10 UI
Modulation Frequency	See Table below

The unit under test transmit signal is jittered at increasing frequencies until errors are detected.

NOTE An additional test has been added as part of sub-tests 1 and 3 to detect the illegal option mix of UHK jitter Tx. and SDH clock card modified for 155 MHz. This is the first action in the first jitter subtest. If this error is detected, no further tests are run.

Subtest Number:	Clock Rate:	Modulation Frequency
1*	140M	2kHz
2*	140M	5kHz
3	34M	2kHz
4	34M	5kHz
5**	34M	100kHz
6*	8M	2kHz
7*	8M	5kHz
8**	8M	50kHz
9	2M	2kHz
10**	2M	5kHz

* These sub-tests are not run if the option 110 PDH module is present.

** These sub-tests are not run as the SPDH received was improved to be more tolerance of high frequency, high amplitude jitter such that it can not be guaranteed to produce errors.

NOTE Sufficient jitter cannot be generated to cause errors at 140 Mb/s.

Subtest 11 to 12

If the unit under test is fitted with an SDH module then these tests are performed.

These tests check that the jitter generator module can generate sufficient jitter in the 140 MHz clock supplied to the SDH transmitter to cause errors in the SDH receiver, and that jitter generated below that level causes no errors.

An external loopback SDH Tx to Rx is used.

The unit under test is reset to its default SDH state and then setup as follows:

Test Timing	3 seconds
Loopback	SDH External
Clock Rate	See Table below
Clock Source	Jitter Generator
PDH Pattern	PRBS23
Jitter Amplitude	10 UI
Modulation Frequency	See Table below

The unit under test transmit signal is jittered at increasing frequencies until errors are detected.

Subtest No:	Clock Rate:	Modulation Frequency
11	140M	2kHz
12	140M	5kHz

NOTE Sufficient jitter cannot be generated to cause errors in SDH signal.

Jitter Receiver Only

Subtests 13 to 28

These tests check that the jitter receiver module can correctly measure the intrinsic jitter from the PDH transmit module.

An external loopback from PDH Tx to PDH Rx is used.

The unit under test is reset to its default PDH state and then setup as follows:

Test Timing	3 seconds
Loopback	PDH External
Filters	Off
Jitter Range	1.6 UI
Clock Rate	See Table below
Pattern	See Table below

The unit under test receiver recovered clock is measured and jitter values are compared against limits in the following Table for various patterns.

The test is repeated for 2M, 8M, 34M and 140M rates.

Subtest No:	Clock Rate	Test Pattern	Upper Limit (UI)	Lower Limit (UI)
13*	140M	PRBS23	0.2	0.00
14*	140M	All zeroes	0.12	0.00
15*	140M	1000	0.2	0.00
16*	140M	All ones	0.2	0.00
17	34M	PRBS23	0.13	0.00
18	34M	All zeroes	0.07	0.00
19	34M	1000	0.13	0.00
20	34M	All ones	0.05	0.00
21*	8M	PRBS23	0.12	0.00
22*	8M	All zeroes	0.05	0.00
23*	8M	1000	0.12	0.00
24*	8M	All ones	0.04	0.00
25	2M	PRBS23	0.12	0.00
26	2M	All zeroes	0.05	0.00

Subtest No:	Clock Rate	Test Pattern	Upper Limit (UI)	Lower Limit (UI)
27	2M	1000	0.12	0.00
28	2M	All ones	0.04	0.00

* These tests are not run if the option 110 PDH module is present.

Additions to Subtests 14, 18, 22 & 26

These tests check the PDH jitter receiver module can correctly measure the intrinsic jitter from the SPDH or uPDH transmit module.

The PDH module output is looped back to the PDH input.

The unit under test is reset to its default PDH state and then set up as follows:

Test Timing	3 seconds
Loopback	PDH External
Filters	Off
Pattern	See Table below

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Subtest Number	Bit Rate	Range	Test Payload	Upper Test Limit	Lower Test Limit
14	10M	1.6 UI	all zeros	0.016	0.000
18	34M	1.6 UI	all ones	0.026	0.000
22	8M	1.6 UI	all ones	0.009	0.000
26	2M	1.6 UI	all ones	0.010	0.000

Transmitter = 0.004 (0.01 UI pp),
Receiver = 0.002 ±intrinsics of (0.01, 0.02, 0.003, 0.004)

Jitter Generator and Receiver Present

Subtests 29 to 44

These tests check that the jitter generator module can correctly generate various levels and frequencies of jitter in the PDH transmit signal and that the jitter receiver can correctly measure the jitter in the PDH receive signal.

An external loopback from PDH Tx to PDH Rx is used.

The unit under test is reset to its default PDH state and then setup as follows:

Test Timing	3 seconds
Loopback	PDH External
Clock Rate	See Table below
Clock Source	Jitter Generator
Pattern	All Ones (140M All Zeroes)
Jitter Amplitude	See Table below
Modulation Frequency	See Table below

The unit under test receiver recovered clock is measured and jitter values are compared against limits in Table for all zeroes at 140M and all ones are 34M, 8M and 2M.

The test is repeated for 2M, 8M, 34M and 140M rates

Subtest No:	Clock Rate	Modulation Frequency (Hz)	Upper Limit (UI)	Lower Limit (UI)
29*	140M	Off	0.12	0.00
30*	140M	10	11.2	8.8
31*	140M	1	1.2	0.8
32*	140M	0.6	0.8	0.4
33	34M	Off	0.05	0.00
34	34M	10	11.2	8.8
35	34M	1	1.2	0.8
36	34M	0.6	0.8	0.4
37*	8M	Off	0.04	0.00
38*	8M	10	11.2	8.8
39*	8M	1	1.2	0.8
40*	8M	0.6	0.8	0.4
41	2M	Off	0.04	0.00
42	2M	10	11.2	8.8
43	2M	1	1.2	0.8
44	2M	0.6	0.8	0.4

* These tests are not run it the option 110 PDH module is present.

Additions to Subtests 31, 35, 39 & 43

These tests check the PDH jitter receiver module can correctly measure the jitter from the Jitter Generator via the SPDH or UPDH transmit module.

The PDH module output is looped back to the PDH input.

The unit under test is reset to its default PDH state and then set up as follows:

Test Timing	3 seconds
Loopback	PDH External
Filters	Off
Pattern	All Ones (140M all Zeros)

The unit under test receiver recovered clock is measured and jitter values are compared against limits in the Table for the various patterns.

10 UI pp = 3.536 rms 1 UI = 0.354 rms

Subtest Number	Bit Rate	Jitter Amplitude UIpp	Mod. Frequency Hz	Upper Test Limit	Lower Test Limit
31	140M	1	10K	0.415	0.292
35	34M	1	200K	0.422	0.285
39	8M	1	100K	0.401	0.306
43	2M	1	25K	0.402	0.305

Transmitter = 3.536 ± 5% ±(0.014, 0.011, 0.007, 0.007),
Receiver = ±5% +- 0.02 ± (0.04, 0.05, 0.04, 0.04)

Transmitter = 0.354 ± 5% ±(0.014, 0.011, 0.007, 0.007),
Receiver = ±5% +- 0.002 ± (0.01, 0.02, 0.003, 0.004)

Subtests 45 to 48

These tests check for correct operation of the hits detector.

An external loopback from PDH Tx to PDH Rx is used.

The unit under test is reset to its default PDH state and then setup as follows:

Loopback	PDH External
Test Timing	1 second
Clock Rate	See Table below
Clock Source	Jitter Generator
Pattern	All Ones (140M All Zeroes
Jitter Amplitude	1 UI
Modulation Frequency	1000 Hz
Hits Threshold	0.7 UI

Subtest No:	Clock Rate	Upper Limit	Lower Limit
45	2M	2100	1900
46*	8M	2100	1900
47	34M	2100	1900
48*	140M	2100	1900

* These tests are not run if the option 110 PDH module is present.

A3K Jitter Generator Only

Subtest 88 *{Requires any PDH Tx/Rx, A3K Jitter Tx modules.}*

This test checks that the jitter generator module can generate jitter at PDH 2 Mb/s range 80. Note that sufficient jitter cannot be generated to cause errors.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback PDH Tx to Rx
Test Timing	3 seconds
Tx Jitter Range	80 UI
Clock Source	Jitter Generator
PDH Pattern	PRBS23

Subtest 89 *{Requires any PDH Tx/Rx, A3K Jitter Tx, any Jitter Rx modules.}*

This test checks that the jitter generator module can correctly generate jitter at PDH 2 Mb/s range 80 in the PDH transmit module and that the jitter receiver can correctly measure the jitter in the PDH receive signal.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback PDH Tx to Rx
Test Timing	3 seconds
Tx Jitter Range	80 UI
Rx Jitter Range	16 UI
Clock Source	Jitter Generator
PDH Pattern	All Ones

Subtest 90 *{Requires any PDH Tx/Rx, A3K Jitter Tx, any Jitter Rx modules.}*

This test checks that the jitter generator module can generate sufficient jitter at PDH 2 Mb/s range 80 in the PDH transmit module and that the jitter receiver can correctly detect an over-range condition, but does not lose lock.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback PDH Tx to Rx
Test Timing	3 seconds
Filters	Off
Tx Jitter Range	80 UI
Rx Jitter Range	16 UI
Clock Source	Jitter Generator
PDH Pattern	All Ones

Subtest 91 *Requires any SDH Tx/Rx, A3K Jitter Tx modules.*

This test checks that the jitter generator module can generate jitter at SDH 155 Mb/s range 50. Note that sufficient jitter cannot be generated to cause errors.

Runs only when ALL TESTS is selected.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback SDH Tx to Rx
Test Timing	3 seconds
Tx Jitter Range	50 UI
Clock Source	Jitter Generator

Loopback	External loopback SDH Tx to Rx
Test Timing	3 seconds
PDH Pattern	PRBS23

Subtest 92 *Requires any SDH Tx, A3K Jitter Tx, STM-1e Jitter Rx modules.*

This test checks jitter generator module can correctly generate jitter at range 50 in the SDH transmit module and that the jitter receiver can correctly measure the jitter in the 155 MHz electrical receive signal.

Runs only when JITTER TESTS is selected.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback SDH output to STM-1e Jitter input
Test Timing	3 seconds
Filters	Off
Tx Jitter Range	50 UI
Rx Jitter Range	16 UI
Clock Source	Jitter Generator
PDH Pattern	PRBS23

Subtest 93 *Requires UH1 / UH2 / URU / USN / UKT SDH Tx, A3K Jitter Tx, STM-1o Jitter Rx modules.*

This test checks jitter generator module can correctly generate jitter at range 50 in the SDH transmit module and that the jitter receiver can correctly measure the jitter in the 155 MHz optical receive signal.

Runs only when JITTER TESTS is selected.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback SDH output to STM-1o input
Test Timing	3 seconds
Filters	Off
Jitter Range	16 UI
Clock Source	Jitter Generator
Pattern	PRBS23

Subtest 94 *Requires UH2 / URU / USN / UKT SDH Tx, A3K Jitter Tx, STM-4O Jitter Rx modules.*

This test checks jitter generator module can correctly generate jitter at range 200 in the SDH transmit module and that the jitter receiver can correctly measure the jitter in the 622 MHz optical receive signal.

Runs only when JITTER TESTS is selected.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback SDH output to STM-4o Jitter input
Test Timing	3 seconds
Filters	Off
Tx Jitter Range	200 UI
Rx Jitter Range	16 UI
Clock Source	Jitter Generator
PDH Pattern	PRBS23

STM Jitter Receiver Selftests

STM Jitter Receiver Selftests

These jitter self tests are grouped into three main test sections to allow for:

- STM-1e electrical interface at 155 Mb/s
- STM-1e + 10 electrical interface at 155 Mb/s plus optical interface at 155 Mb/s
- STM-1e + 10 + 40 as above plus 622 Mb/s optical interface

Each test MUST have a corresponding SDH transmitter fitted otherwise no self tests are possible. If a jitter generator is fitted then further tests can be carried out.

STM-1e plus SDH Tx Present

Subtests 49 - 54

These tests check the 155 MHz electrical jitter receiver module can correctly measure the intrinsic jitter from the SDH transmit module.

The SDH module output is looped back to both the SDH input and the STM-1e input using very short cables and a T-piece on the SDH output.

The unit under test is reset to its default SDH state and then set up as follows:

Loopback	SDH external, STM-1e external
Test Timing	3 seconds
Filters	Off
STM Payload	140 Mb/s
Pattern	See Table below

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Subtest Number	Range	Test Payload	Upper Test Limit	Lower Test Limit
49	1.6 UI	PRBS23	0.04	0.00
50	1.6 UI	All Zeros	0.04	0.00
51	1.6 UI	All Ones	0.04	0.00
52	16 UI	PRBS23	0.14	0.00
53	16 UI	All Zeros	0.14	0.00
54	16 UI	All Ones	0.14	0.00

Additions to Subtest 49

These tests check the 155 MHz electrical jitter receiver module can correctly measure the intrinsic jitter from the SDH transmit module.

The SDH module output is looped back to both the SDH input and the STM-1e input using very short cables and a T-piece on the SDH output.

The unit under test is reset to its default SDH state and then set up as follows:

Loopback	SDH external, STM-1e external
Test Timing	3 seconds
Filters	Off
STM Payload	140 Mb/s
Pattern	See Table below

The unit under test receiver recovered clock is measured and jitter values are compared against limits in the Table for the various patterns.

Sub Test No Range

Test Payload Upper Test Limit Lower Test Limit Error Codes for Result Low High VCO Not Jitter STM LOS Settling Unlock.

Subtest Number	Range	Test Payload	Upper Test Limit	Lower Test Limit
49	1.6 UI	PRBS23	0.012	0.000

Transmitter = 0.004 (0.01 UI pp), Receiver = 0.002 ±0.006

STM-1e plus SDH Tx plus Jitter Generator Present

Subtests 55 - 60

These tests check the 155 MHz electrical jitter receiver module can correctly measure the jitter from the Jitter Generator via the SDH transmit module.

The SDH module output is looped back to both the SDH input and the STM-1e input using very short cables and a T-piece on the SDH output.

The unit under test is reset to its default SDH state and then set up as follows:

Loopback	SDH external, STM-1e external
Test Timing	3 seconds
Clock Source	Jitter Generator
Filters	Off
STM Payload	140 Mb/s
Pattern	PRBS23 payload

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Additions to Subtest 59

These tests check the 155 MHz electrical jitter receiver module can correctly measure the jitter from the Jitter Generator via the SDH transmit module.

The SDH module output is looped back to both the SDH input and the STM-1e input using very short cables and a T-piece on the SDH output.

The unit under test is reset to its default SDH state and then set up as follows::

Loopback	SDH external, STM-1e external
Test Timing	3 seconds
Clock Source	Jitter Generator
Filters	Off
STM Payload	140 Mb/s
Pattern	PRBS23 payload

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Tx = 1.768 UI ± 5% ±0. 014,Rx = ± 5% ±0.06
Tx = 0.354 UI ± 5% ± 0.014 Rx = ± 5% ±0.008

Subtest 61

This test checks for correct operation of the hits detector.

The SDH module output is looped back to both the SDH input and the STM-1e input using very short cables and a T-piece on the SDH output.

The unit under test is rest to its default SDH state and then set up as follows:

Loopback	SDH external, STM-1e external
Test Timing	1 second
Clock Source	Jitter Generator
Filters	Off
STM Payload	140 Mb/s
Pattern	PRBS23 payload
RX Threshold	0.7 UI

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

STM-10 plus SDH Tx Present

Subtests 62 - 67

These tests check the 155 MHz optical jitter receiver module can correctly measure the intrinsic jitter from the SDH transmit module.

The SDH module output is looped back to the STM-1o input.

The unit under test is reset to its default SDH state and then set up as follows:

Test Timing	3 seconds
Loopback	SDH external, STM-10E external
Filters	Off
STM Payload	140 Mb/s
Test Timing	3 seconds
Loopback	SDH external, STM-40 external
Clock Source	Jitter Generator
Filters	Off
STM Payload	140 Mb/s
Pattern	PRBS23 payload

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Additions to Subtest 62

These tests check the 155 MHz optical jitter receiver module can correctly measure the intrinsic jitter from the SDH transmit module.

The SDH module output is looped back to the STM-1o input.

The unit under test is reset to its default SDH state and then set up as follows:

Test Timing	3 seconds
Loopback	SDH external, STM-1o external
Filters	Off
STM Payload	140 Mb/s
Pattern	See Table below

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Subtest Number.	Range	Test Payload	Upper Test Limit	Lower Test Limit
62	1.6 UI	All Ones	0.023	0.000

Transmitter = 0.004 (0.01 UI pp), Receiver = 0.015 ±0.00

STM-10 plus SDH Tx plus Jitter Generator Present.

Subtests 68 - 73

These tests check the 155 MHz optical jitter receiver module can correctly measure the jitter from the Jitter Generator via the SDH transmit module.

The SDH module output is looped back to the STM-1o input.

The unit under test is reset to its default SDH state and then set up as follows:

Test Timing	3 seconds
Loopback	SDH external, STM-1O external
Filters	Off
STM Payload	140 Mb/s
Pattern	See Table below

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Subtest Number	Jitter Amp	Mod Freq	Upper Test Limit	Lower Test Limit
68	Off	-	0.05	0.00
69	5.0 UI	100 Hz	6.1	3.9
70	5.0 UI	1 kHz	6.1	3.9
71	1.0 UI	10 kHz	1.14	0.86
72	1.0 UI	100 kHz	1.14	0.86
73	0.3 UI	1 MHz	0.37	0.23

Additions to Subtest 72

These tests check the 155 MHz optical jitter receiver module can correctly measure the jitter from the Jitter Generator via the SDH transmit module.

The SDH module output is looped back to the STM-1o input.

The unit under test is reset to its default SDH state and then set up as follows::

Test Timing	3 seconds
Loopback	SDH external, STM-1O external
Clock Source	Jitter Generator
Filters	Off
STM Payload	140 Mb/s
Pattern	PRBS23 payload

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Tx = 1.768 UI ± 5% ±0. 014, Rx = ± 5% ±0.02 ±0.04
Tx = 0.354 UI ± 5% ±0.014Rx = ± 5% ±0.002 ±0.015

Subtest 74

This test checks for correct operation of the hits detector.

The SDH module output is looped back to the STM-1o input.

The unit under test is reset to its default SDH state and then set up as follows:

Test Timing	3 seconds
Loopback	SDH external, STM-1o external
Clock Source	Jitter Generator
Filters	Off
STM Payload	140 Mb/s
Pattern	PRBS23 payload
RX Threshold	0.7 UI

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

STM-40 plus SDH Tx Present

Subtests 75 - 80

These tests check the 622 MHz optical jitter receiver module can correctly measure the intrinsic jitter from the SDH transmit module.

The SDH module output is looped back to the STM-4o input.

The unit under test is reset to its default SDH state and then set up as follows:

Test Timing	3 seconds
Loopback	SDH external, STM-4o external
Filters	Off
STM Payload	140 Mb/s
Pattern	See Table below

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Subtest Number	Range	Test Payload	Upper Test Limit	Lower Test Limit
75	1.6 UI	PRBS23	0.06	0.00
76	1.6 UI	All Zeros	0.06	0.00
77	1.6 UI	All Ones	0.06	0.00
78	16 UI	PRBS23	0.26	0.00
79	16 UI	All Zeros	0.26	0.00
80	16 UI	All Ones	0.26	0.00

Additions to Subtest 75

These tests check the 622 MHz optical jitter receiver module can correctly measure the intrinsic jitter from the SDH transmit module.

The SDH module output is looped back to the STM-4o input.

The unit under test is reset to its default SDH state and then set up as follows:

Test Timing	3 seconds
Loopback	SDH external, STM-4o external
Filters	Off
STM Payload	140 Mb/s
Pattern	See Table below

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Subtest Number.	Range	Test Payload	Upper Test Limit	Lower Test Limit
75	1.6 UI	All Zeros	0.036	0.000

Transmitter =0.014 (0.04 UI pp), Receiver = 0.002 ±0.02

STM-40 plus SDH Tx plus Jitter Generator Present

Subtests 81 - 86

These tests check the 622 MHz optical jitter receiver module can correctly measure the jitter from the Jitter Generator via the SDH transmit module.

The SDH module output is looped back to the STM-4o input.

The unit under test is reset to its default SDH state and then set up as follows:

Test Timing	3 seconds
Loopback	SDH external, STM-4o external
Clock Source	Jitter Generator
Filters	Off
STM Payload	140 Mb/s
Pattern	PRBS23 payload

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Additions to Subtest 85

These tests check the 622 MHz optical jitter receiver module can correctly measure the jitter from the Jitter Generator via the SDH transmit module.

The SDH module output is looped back to the STM-4o input.

The unit under test is reset to its default SDH state and then set up as follows:

Test Timing	3 seconds
Loopback	SDH external, STM-4o external
Clock Source	Jitter Generator
Filters	Off
STM Payload	140 Mb/s
Pattern	PRBS23 payload

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

Tx = 1.768 UI ± 5% ±0. 035, Rx = ± 5% ±0.02 ±0.08
Tx = 0.354 UI ± 5% ± 0.035 Rx = ± 5% ±0.002 ±0.02

Subtest 87

This test checks for correct operation of the hits detector.

The SDH module output is looped back to the STM-4o input.

The unit under test is reset to its default SDH state and then set up as follows:

Test Timing	1 second
Loopback	SDH external, STM-4o external
Clock Source	Jitter Generator
Filters	Off
STM Payload	140 Mb/s
Pattern	PRBS23 payload
RX Threshold	0.7 UI

The unit under test receiver recovered clock is measured and jitter values are compared against limits for the various patterns.

A3K Jitter Generator

The following additional subtests are performed when Option A3K Jitter Generator Module is fitted.

Subtest 88

Requires any PDH Tx/Rx, A3K Jitter Tx modules.

This test checks that the jitter generator module can generate jitter at PDH 2 Mb/s range 80. Note that sufficient jitter cannot be generated to cause errors.

The unit under test is reset to its default state and then setup as follows:

LoopbackExternal loopback PDH Tx to Rx.
Test Timing3 seconds
Tx Jitter Range80 UI

Clock SourceJitter Generator
PDH PatternPRBS23

Subtest 89

Requires any PDH Tx/Rx, A3K Jitter Tx, any Jitter Rx modules.

This test checks that the jitter generator module can correctly generate jitter at PDH 2 Mb/s range 80 in the PDH transmit module and that the jitter receiver can correctly measure the jitter in the PDH receive signal.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback PDH Tx to Rx.
Test Timing	3 seconds
Filters	Off
Tx Jitter Range	80 UI
Rx Jitter Range	16 UI
Clock Source	Jitter Generator
PDH Pattern	All Ones

Subtest 90

Requires any PDH Tx/Rx, A3K Jitter Tx, any Jitter Rx modules.

This test checks that the jitter generator module can generate sufficient jitter at PDH 2 Mb/s range 80 in the PDH transmit module and that the jitter receiver can correctly detect an over-range condition, but does not lose lock.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback PDH Tx to Rx.
Test Timing	3 seconds
Filters	Off
Tx Jitter Range	80 UI
Rx Jitter Range	16 UI
Clock Source	Jitter Generator
PDH Pattern	All Ones

Subtest 91

Requires any SDH Tx/Rx, A3K Jitter Tx modules.

This test checks that the jitter generator module can generate jitter at SDH 155 Mb/s range 50. Note that sufficient jitter cannot be generated to cause errors.

Runs only when ALL TESTS is selected.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback SDH Tx to Rx.
Test Timing	3 seconds
Tx Jitter Range	50 UI
Clock Source	Jitter Generator
Pattern	PRBS23

Requires any SDH Tx, A3K Jitter Tx, STM-1e Jitter Rx modules.

This test checks jitter generator module can correctly generate jitter at range 50 in the SDH transmit module and that the jitter receiver can correctly measure the jitter in the 155 MHz electrical receive signal.

Runs only when JITTER TESTS is selected.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback SDH output to STM-1e Jitter input.
Test Timing	3 seconds
Filters	Off
Tx Jitter Range	50 UI
Rx Jitter Range	16 UI
Clock Source	Jitter Generator
Pattern	PRBS23

Subtest 93

Requires USN / UKT SDH Tx, A3K Jitter Tx, STM-1o Jitter Rx modules.

This test checks jitter generator module can correctly generate jitter at range 50 in the SDH transmit module and that the jitter receiver can correctly measure the jitter in the 155 MHz optical receive signal.

Runs only when JITTER TESTS is selected.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback SDH output to STM-1o input.
Test Timing	3 seconds
Filters	Off
Jitter Range	16 UI
Clock Source	Jitter Generator
Pattern	PRBS23

Subtest 94

Requires USN / UKT SDH Tx, A3K Jitter Tx, STM-4o Jitter Rx modules.

This test checks jitter generator module can correctly generate jitter at range 200 in the SDH transmit module and that the jitter receiver can correctly measure the jitter in the 622 MHz optical receive signal.

Runs only when JITTER TESTS is selected.

The unit under test is reset to its default state and then setup as follows:

Loopback	External loopback SDH output to STM-4o Jitter input.
Test Timing	3 seconds
Filters	Off
Tx Jitter Range	200 UI
Rx Jitter Range	16 UI
Clock Source	Jitter Generator
Pattern	PRBS23

General Service Sheet G16 - Dismantling and Re-assembly Procedures

This section provides the following information:

- How to remove and replace Modules in the HP 37717C.
- How to dismantle each module and remove board assemblies for repair/replacement.
- How to remove and service the PSU Module, the Line Module and Cooling Fans.
- How to remove the Front Panel Assembly the Interface Boards, OEM Display and Printer.

Removing Modules from the Instrument

1. Switch off the HP 37717C and disconnect the power cord and any interconnecting cables.
2. Place the instrument face down on the workbench.
3. Remove the 4 screws securing the rubber feet to the rear panel.
4. If Optical Modules are fitted unscrew the optical shield from the input and output connectors.
5. Withdraw the outer cabinet sleeve back and out of the instrument.
6. Unscrew the clamp screws securing the modules along the Right hand Side of the instrument.
7. Withdraw each module (or Blanking Plate) out of the righthand side of the instrument along two guide-rails. There is a socket at the end of each board assembly within the module which engages in a socket on the motherboard when the module is pushed fully home. There are two knobs fitted to each module front panel to help with module removal.

NOTE If difficulty is experienced, insert an 8 mm (15/16 AF) open-ended spanner under one side of the module knobs and carefully lever against the knob on the adjacent module.

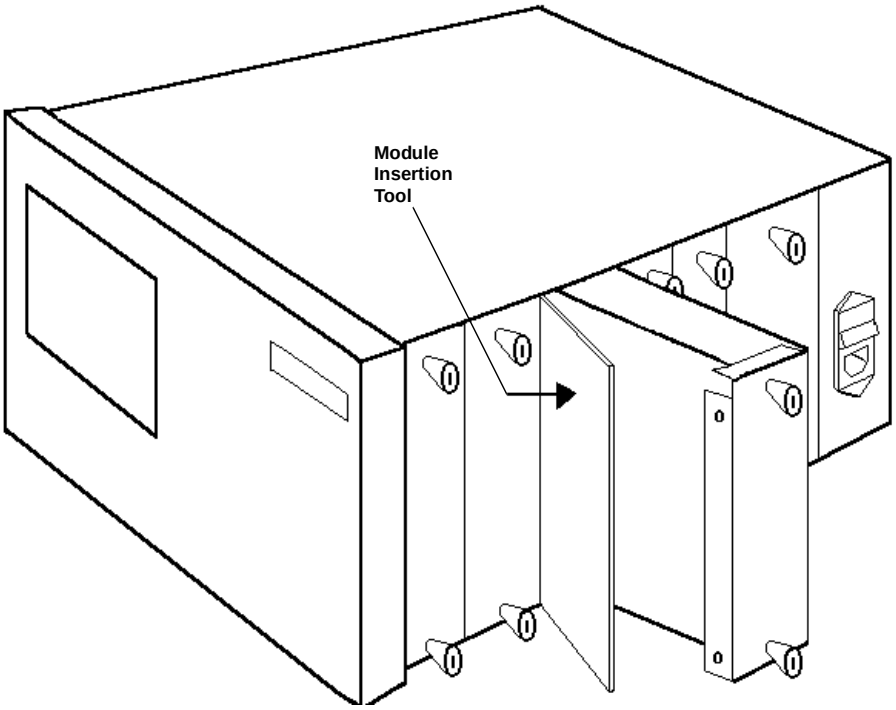
CAUTION Never use a screwdriver or sharp implement to lever the module as circuit tracks may be cut or the module metalwork irreplaceably damaged.

8. Fit each removed module in an anti-static container and place SAFELY to one side.

Replacing Modules in the Instrument

Modules must be replaced in the order shown on the next page.

NOTE **You must use special tool hp part number 03776-00016 or a thin LOW-STATIC plastic or fibre card (200 mm x 135 mm x 0.5 mm) when replacing a module back into the instrument. This is necessary to prevent removal of, or damage to the metal RFI STRIP on the right-hand side of the module next to the one being replaced. Place this card against the RFI Strip on the module TO THE LEFT of the one being replaced, then slide the new Module back into the instrument. Push the Module fully home, then pull out the card. The following diagram illustrates this process.**



CAUTION Severe damage can result if an RFI Strip is dislodged and fall inside the instrument. Always ensure that RFI strips are securely in position and unbroken.

NOTE If neither the above tool or a suiTable card is available, the only accepTable way to replace the module without damaging RFI strips is to remove ALL modules to the LEFT of the one being replaced, then refit all modules working from the back of the instrument (Processor end) forward.

When the module has been pushed fully home in its slot, it should be secured using the two screws and the Outer Cabinet Sleeve, Optical module Shields, and Rear Panel feet fitted as a reversal of the removal procedure.

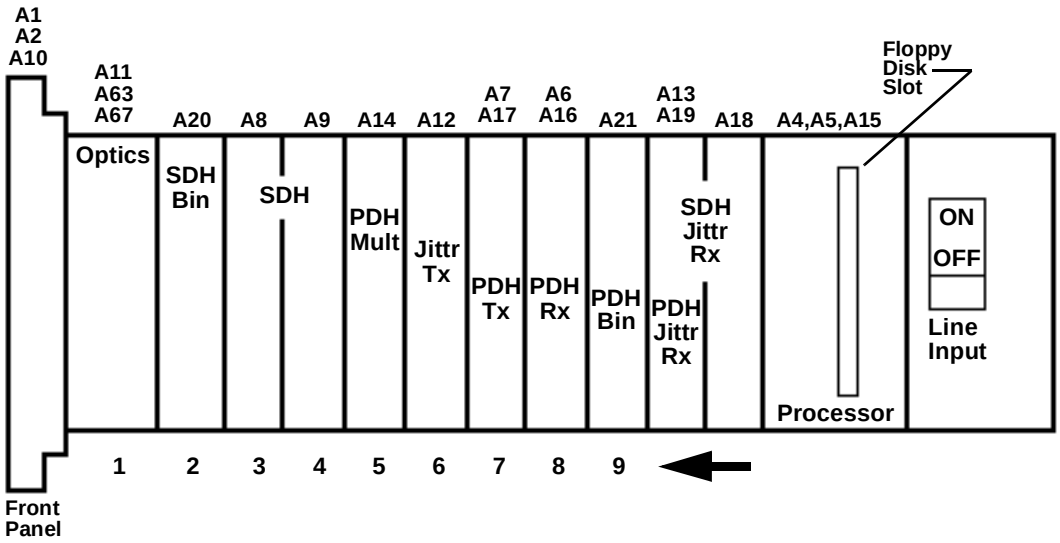


Figure 5-1 Possible Configurations of HP 37717C Modules and Board Assemblies

Removing Board Assemblies from a Module

Each module within the HP 37717C contains one or more replaceable Board Assembly.

The figures and Tables on the following pages show layouts and component parts for all modules current to the HP 37717C. These should be used to help with dismantling an re-assembly when undertaking module repairs.

Processor Disk-Drive Module

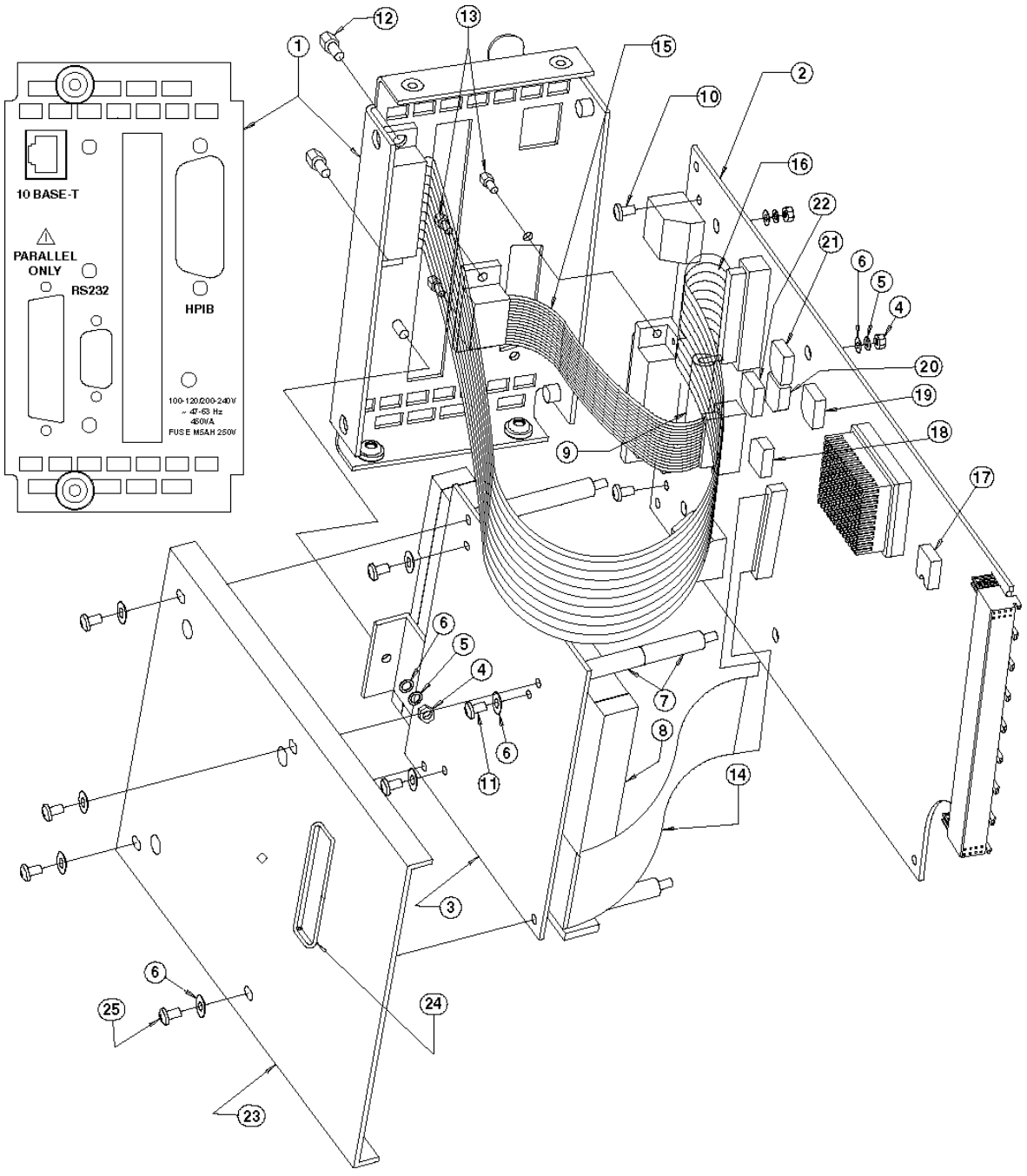


Figure 5-2 Processor Disk-Drive Module - Exploded View

SDH Module

This module has two board assemblies, A8 and A9.

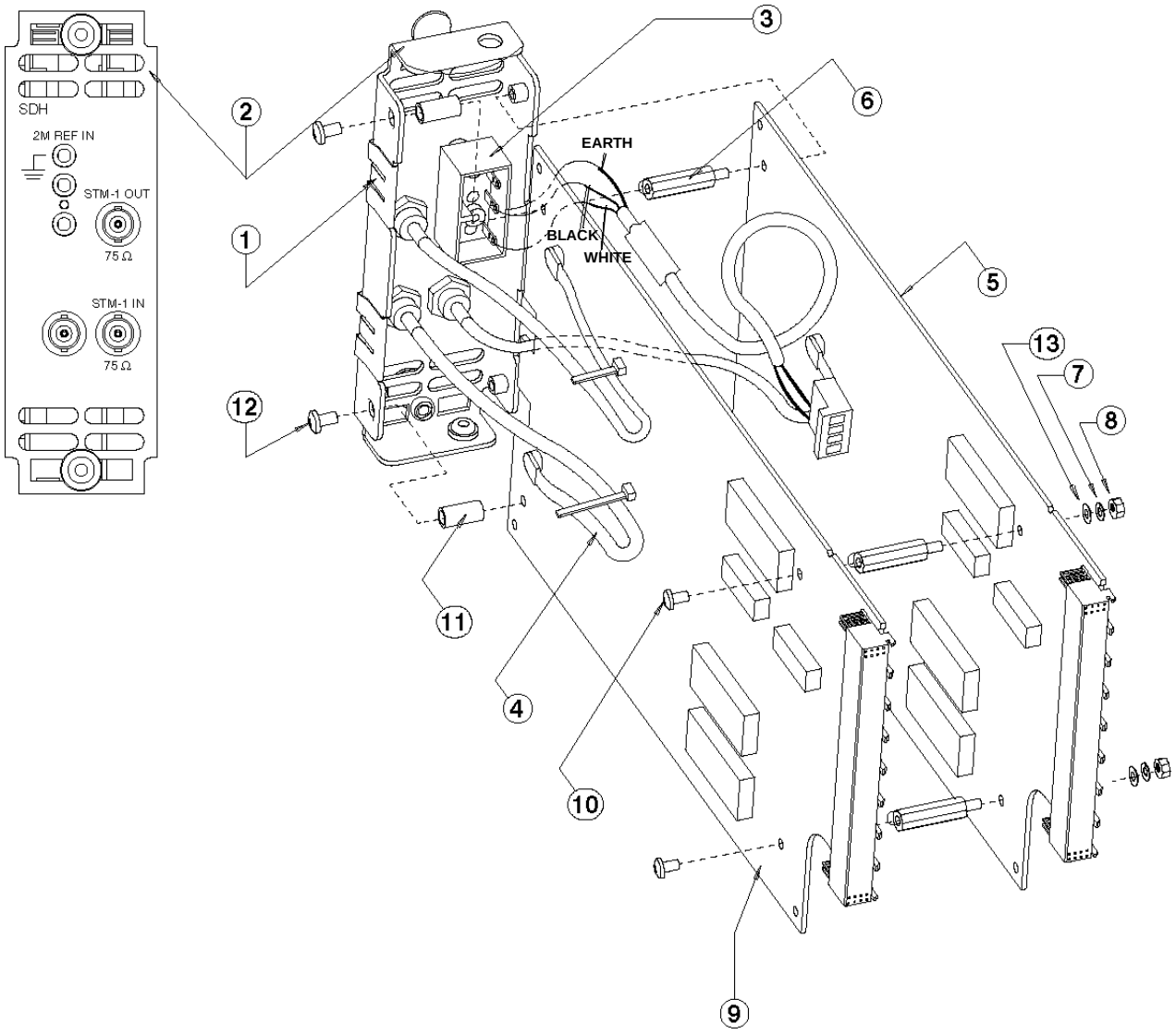


Figure 5-3 SDH Module (BNC) - Exploded View

AIT, SDH Module

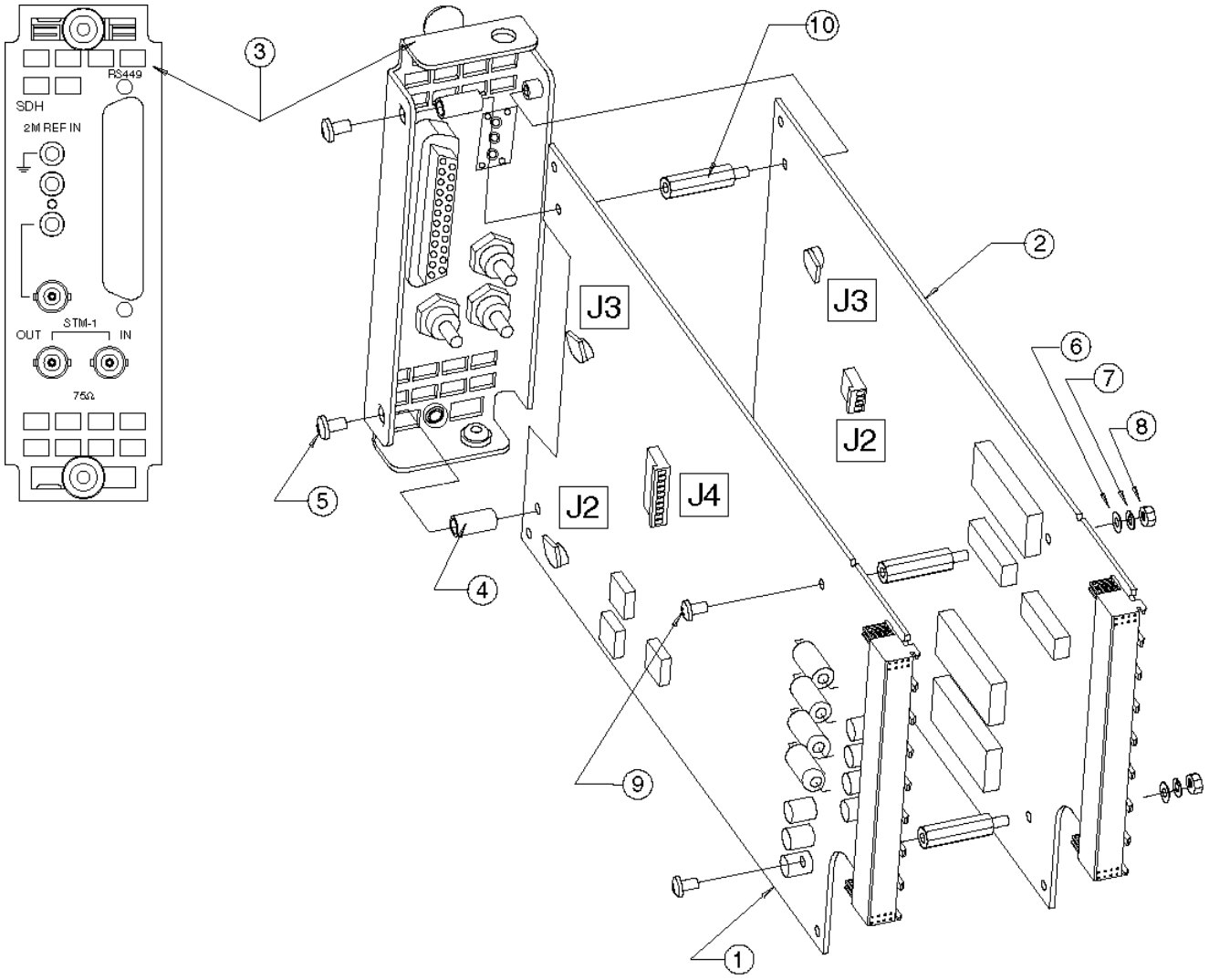


Figure 5-4 AIT SDH Module - Exploded View

Servicing the Module

Each of the two board assemblies can be replaced individually by following the procedure below.

1. Remove the module from the HP 37717C.
2. Unscrew the 4 screws which join the two board assemblies together. The two front screws also secure the boards to the module metalwork.
3. Unplug any cables from each board assembly.
4. Separate the boards taking care not to damage any cables or lose the screws/spacers.

UPDH Module

This module has two board assemblies, A6 and A7.

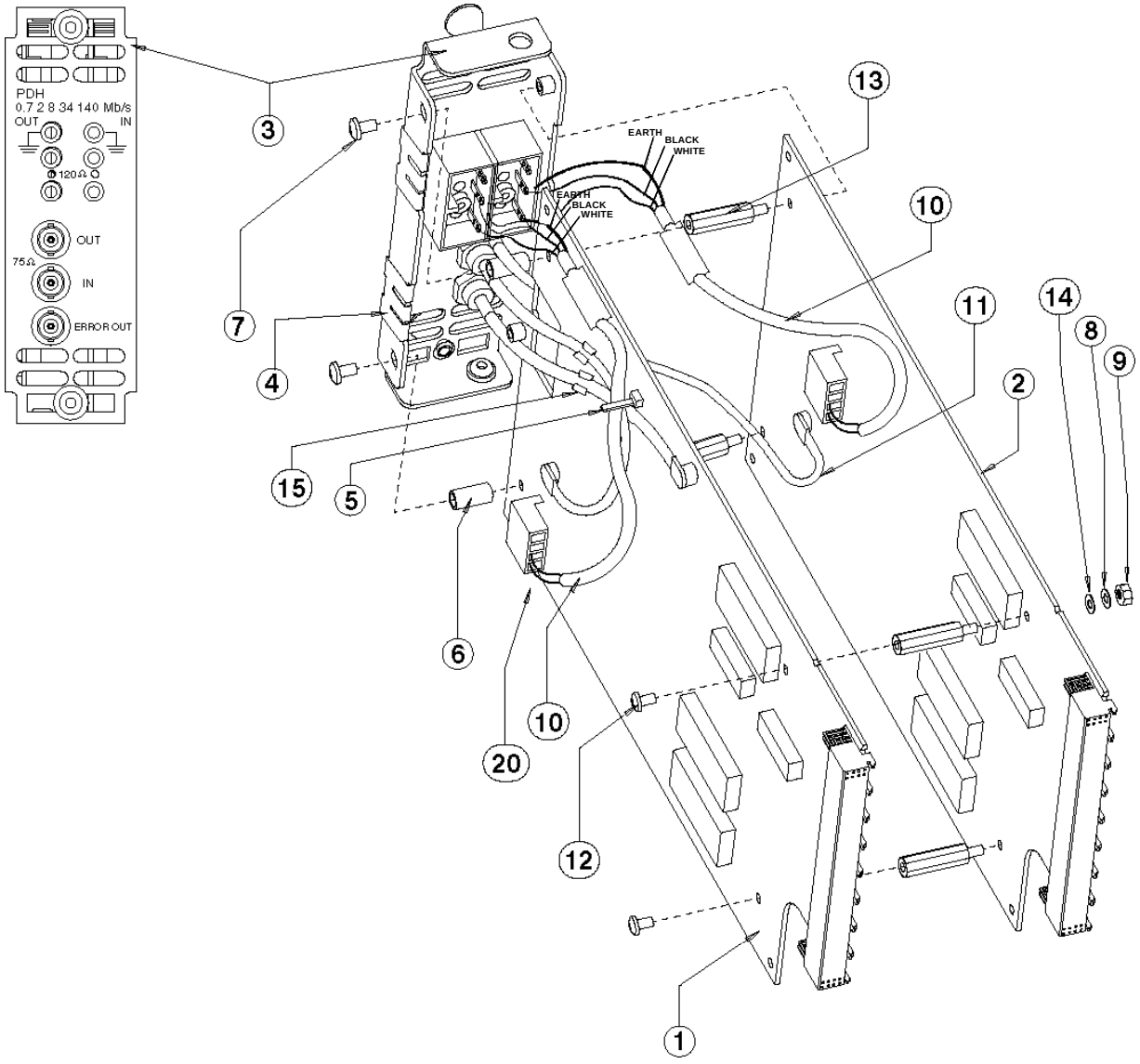


Figure 5-5 UPDH Module (BNC) - Exploded View

Servicing the Module

Each of the two board assemblies can be replaced individually by following the procedure below.

1. Remove the module from the HP 37717C.
2. Unscrew the 4 screws which join the two board assemblies together. The two front screws also secure the boards to the module metalwork.
3. Unplug any cables from each board assembly.
4. Separate the boards taking care not to damage any cables or lose the screws/spacers.

SPDH Receiver

This Module has one board assembly, A16.

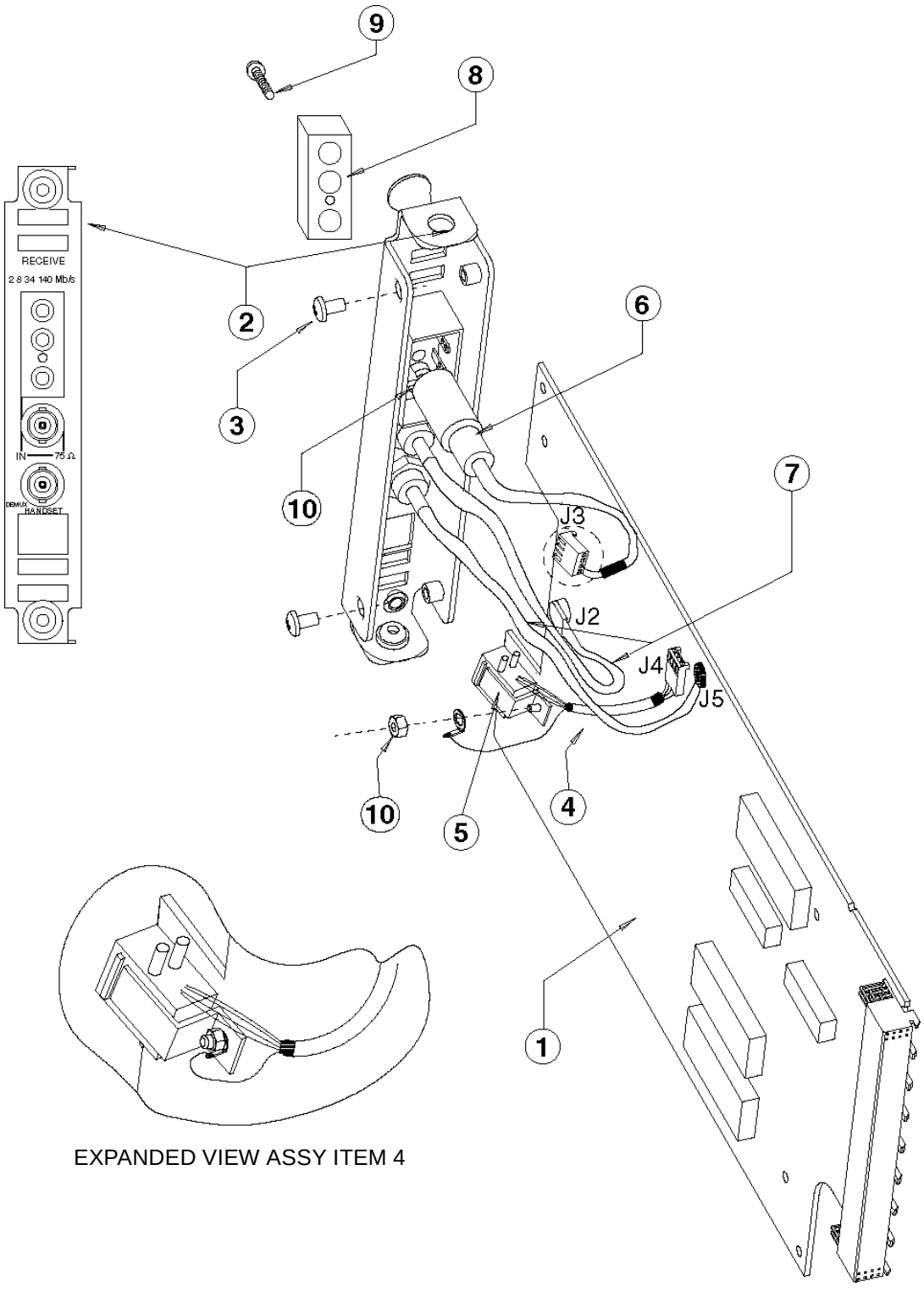


Figure 5-6 SPDH Receiver - Exploded View

Servicing the Module

The single board assembly can be replaced by following the procedure below.

1. Remove the module from the HP 37717C.
2. Unscrew the two front screws which secure the board to the module metalwork.
3. Unplug any cables from the board assembly.
4. Remove the board taking care not to damage any cables or lose the screws/spacers.

SPDH Transmitter

This module has one board assembly, A17.

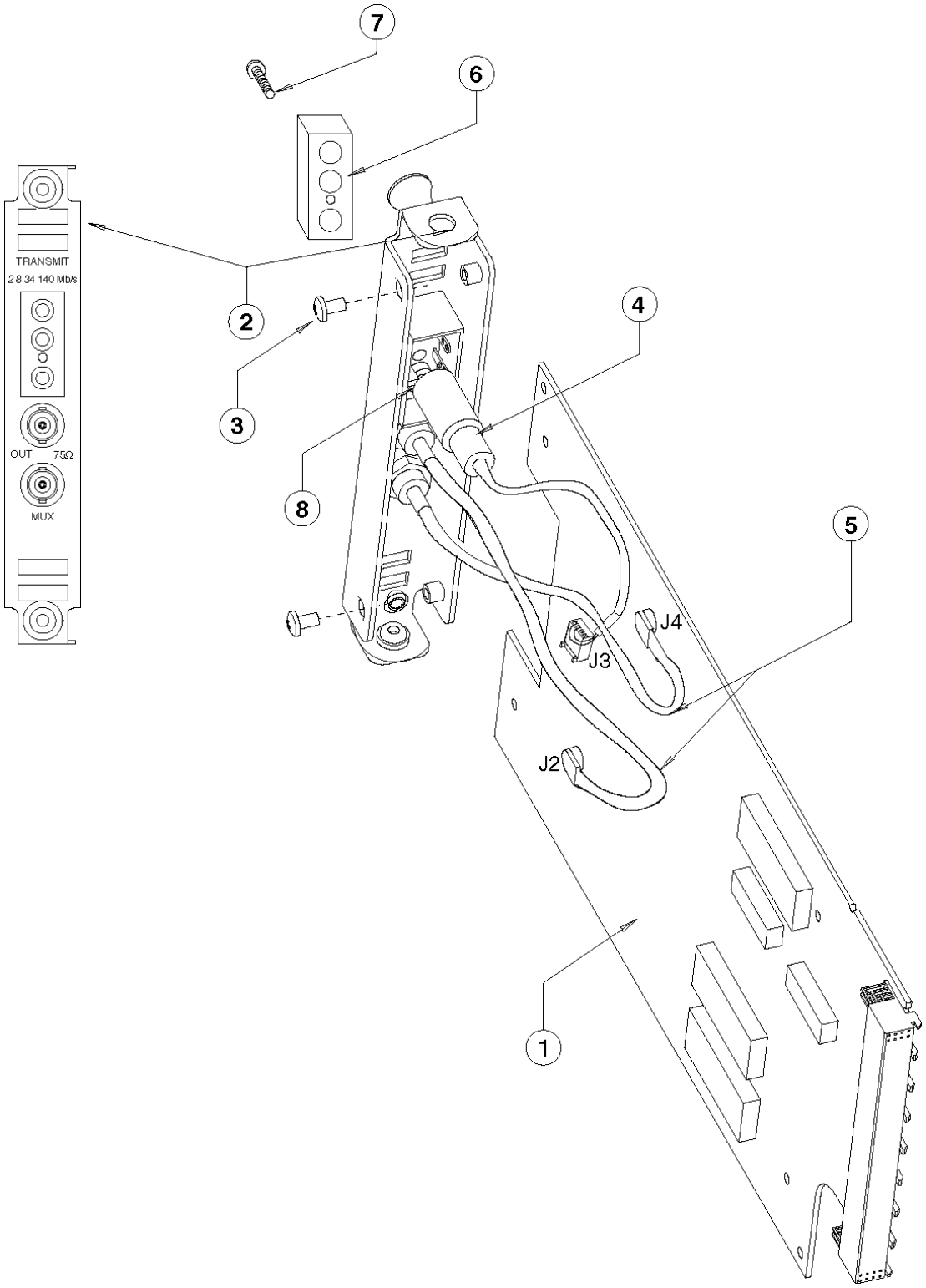


Figure 5-7 SPDH Transmitter - Exploded View

Servicing the Module

The single board assembly can be replaced by following the procedure below.

1. Remove the module from the HP 37717C.
2. Unscrew the two front screws which secure the board to the module metalwork.
3. Unplug any cables from the board assembly.
4. Remove the board taking care not to damage any cables or lose the screws/spacers.

1310 nm STM-1/4 Optical Module (Option UH1)

This module has one board assembly, A11.

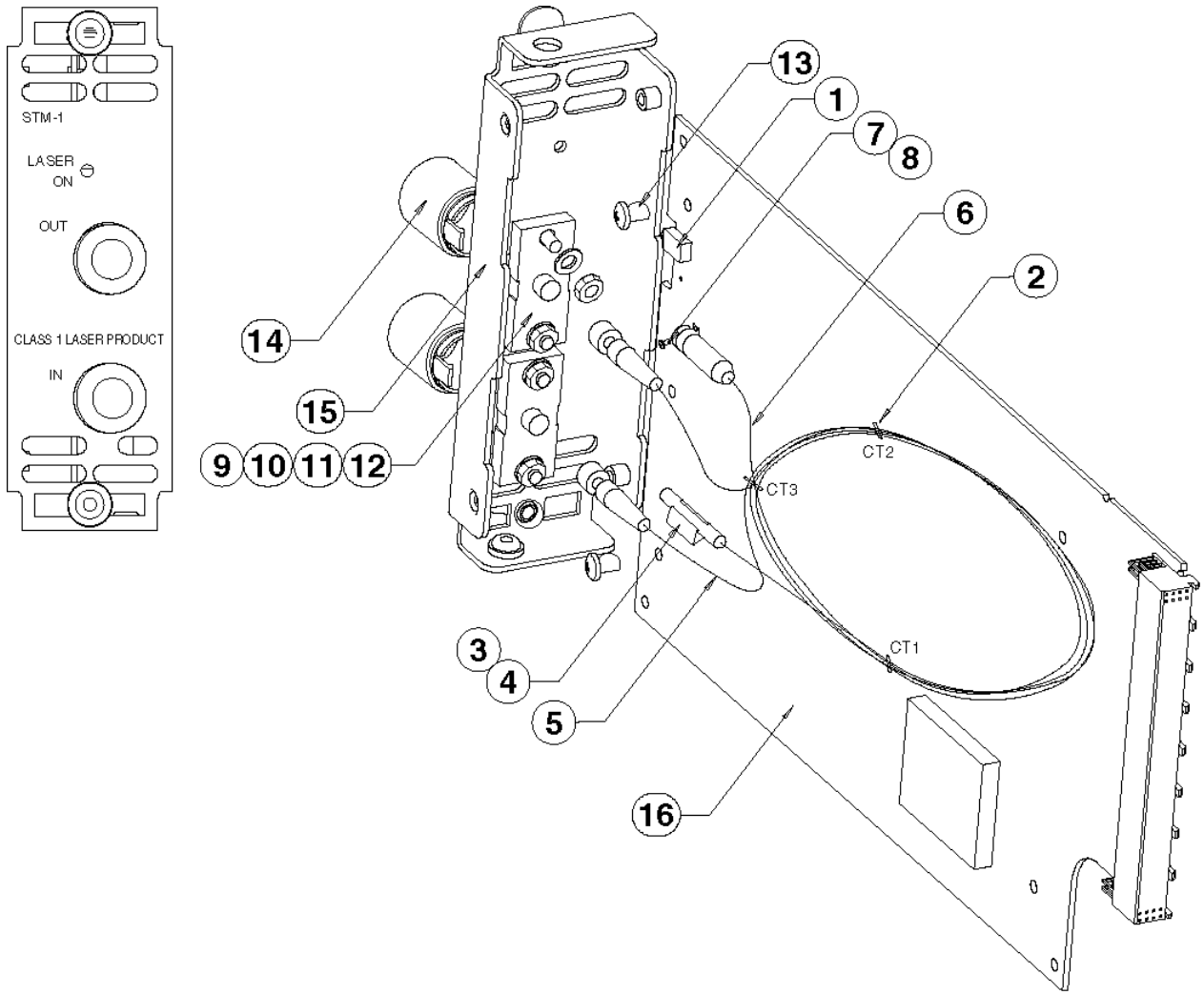


Figure 5-8 1310 nm STM-1 Optics Module - Exploded View

Servicing the Module

The single board assembly used in this module can be replaced by following the procedure below.

1. Remove the module from the HP 37717C.
2. Unscrew the two front screws which secure the board to the module metalwork.
3. Unscrew the fibre-optic interface cables from the module metalwork.
4. Remove the board taking care not to damage the fibre-optic cables or lose the screws/ spacers.

1310 nm STM-1/4 Optical Module (UH2)

This module has one board assembly, A11.

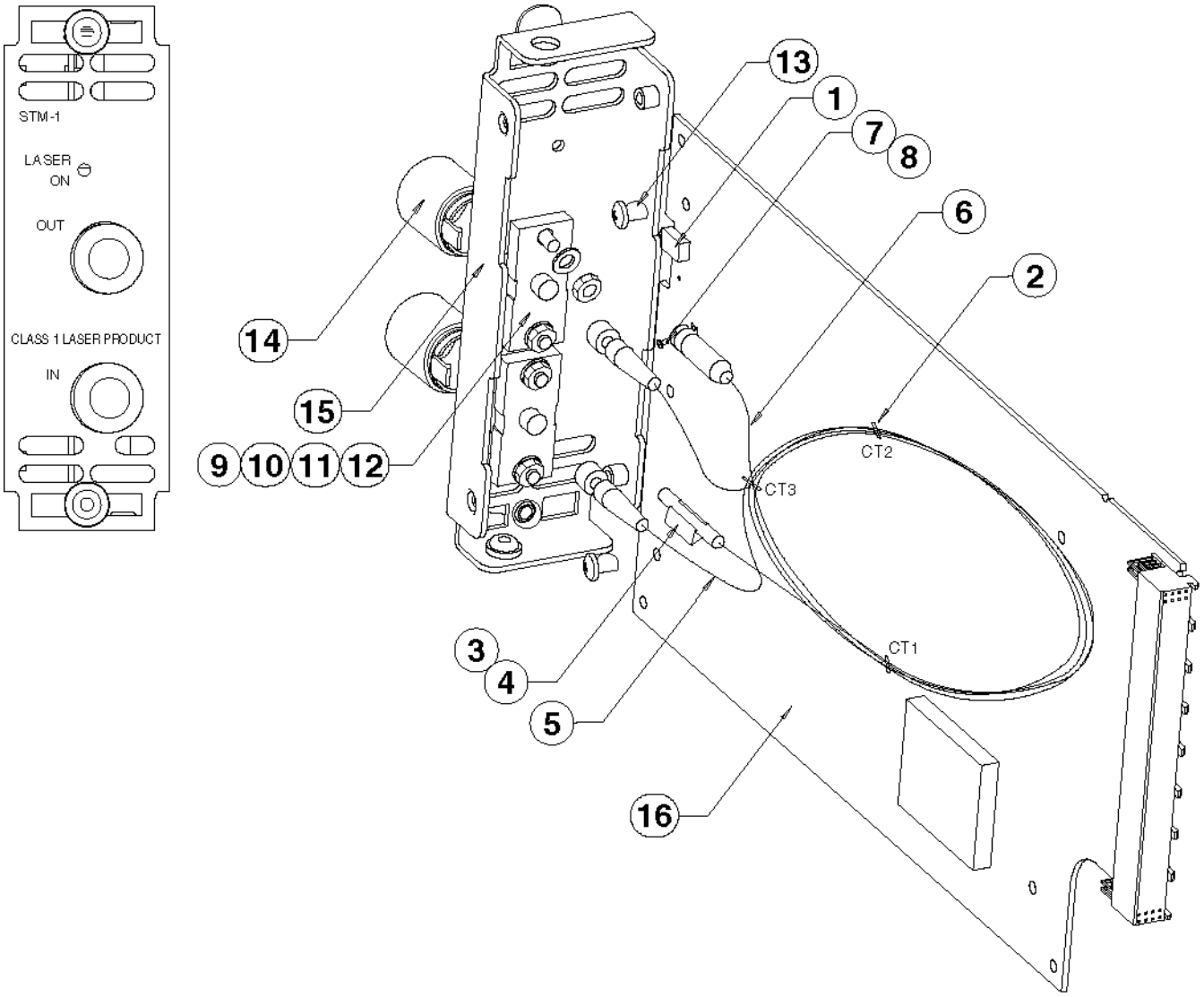


Figure 5-9 1310 nm STM-1/4 Optics Module - Exploded View

Servicing the Module

The single board assembly used in this module can be replaced by following the procedure below.

1. Remove the module from the HP 37717C.
2. Unscrew the two front screws which secure the board to the module metalwork.
3. Unscrew the fibre-optic interface cables from the module metalwork.
4. Remove the board taking care not to damage the fibre-optic cables or lose the screws/ spacers.

1550 nm STM-1 Optical Module (Option URU)

This module has one board assembly, A11.

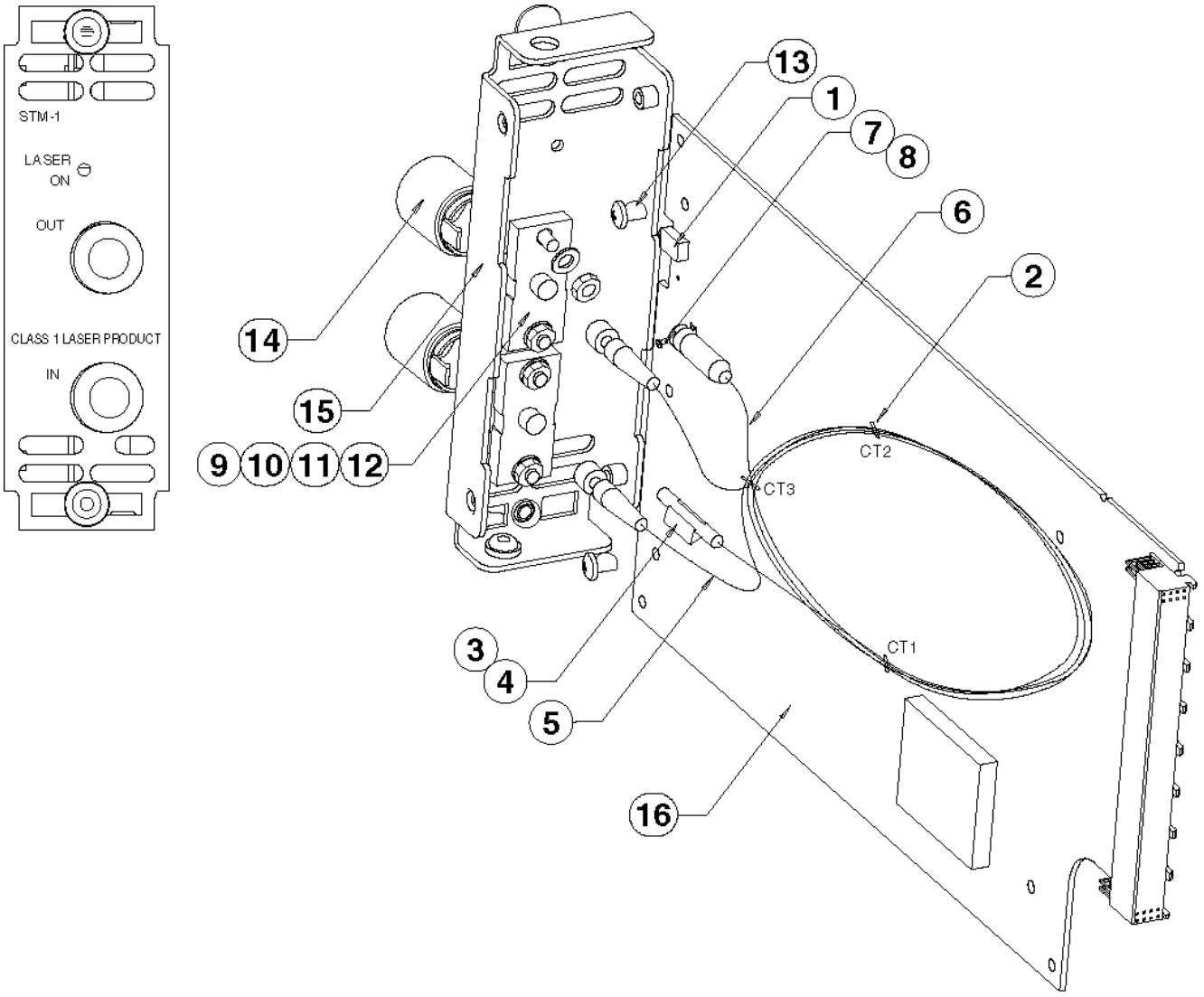


Figure 5-10 1550 nm STM-1 Optics Module - Exploded View

Servicing the Module

The single board assembly used in this module can be replaced by following the procedure below.

1. Remove the module from the HP 37717C.
2. Unscrew the two front screws which secure the board to the module metalwork.
3. Unscrew the fibre-optic interface cables from the module metalwork.
4. Remove the board taking care not to damage the fibre-optic cables or lose the screws/ spacers.

Options UKT/USN/ STM 1/4 Optical Module

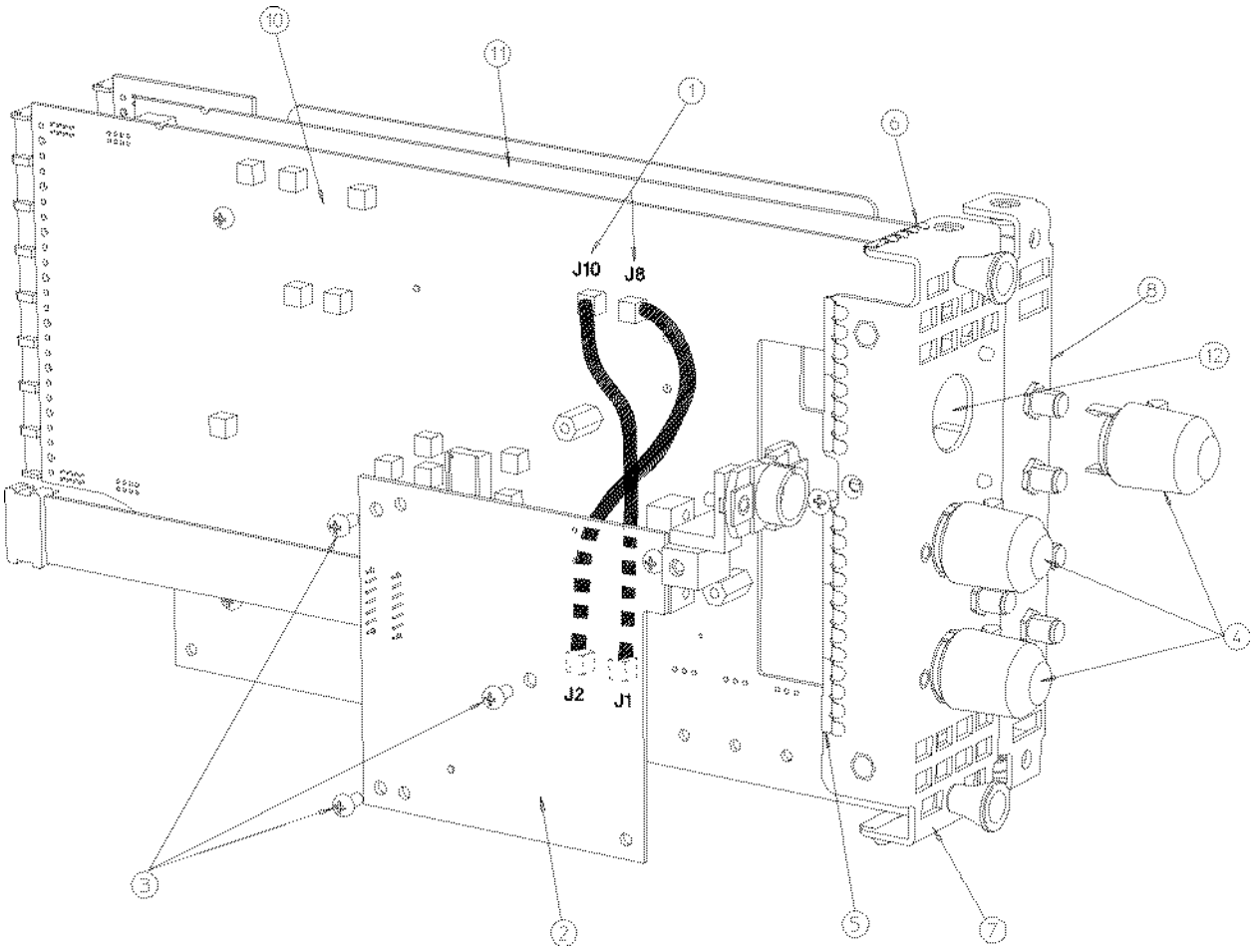


Figure 5-11 Options UKT/USN STM 1/4 Optical Module - Exploded View

Options UKT/USN/ STM 1/4 Optical Module

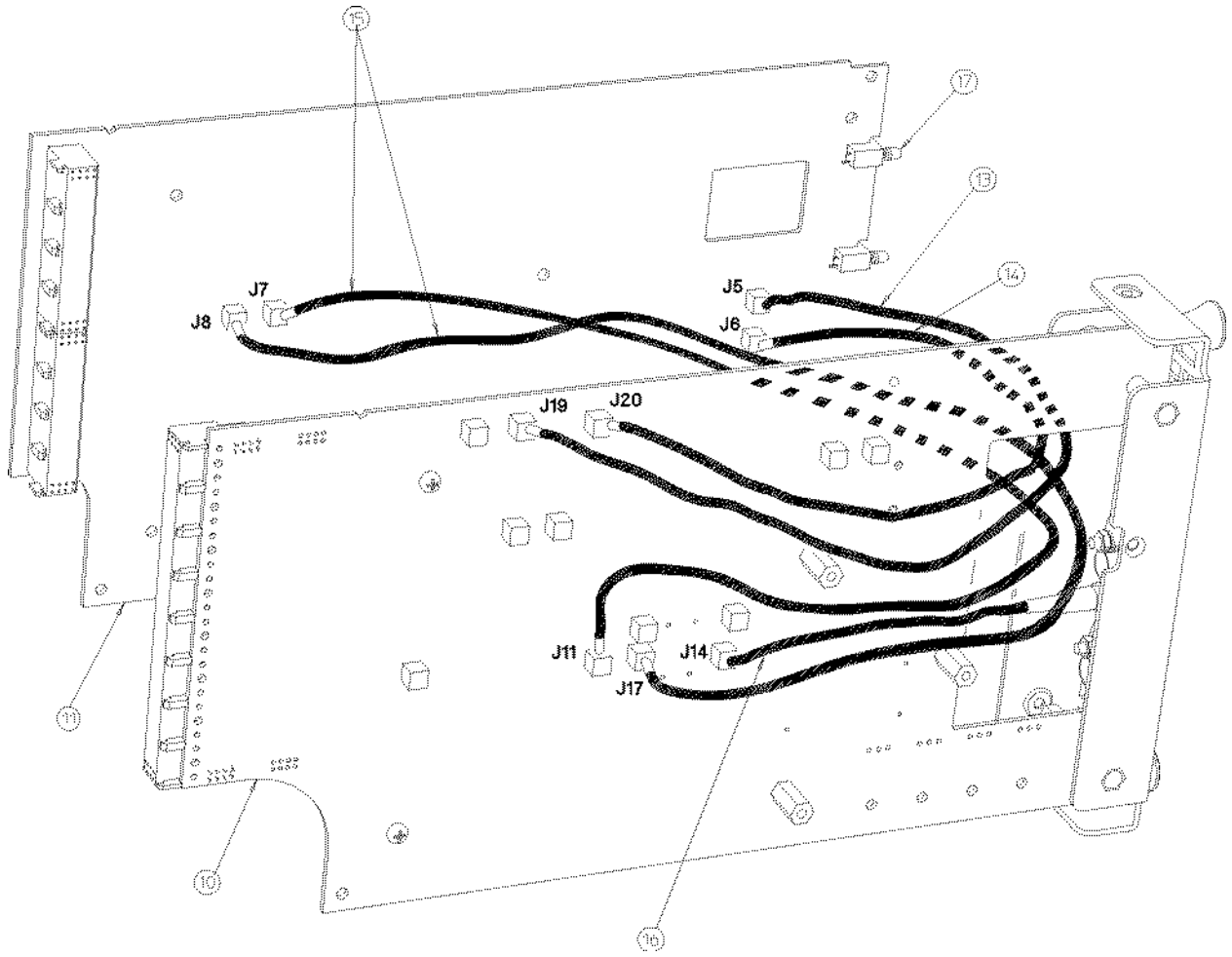


Figure 5-12 Options UKT/USN STM 1/4 Optical Module - Exploded View

SDH Binary Interface Module

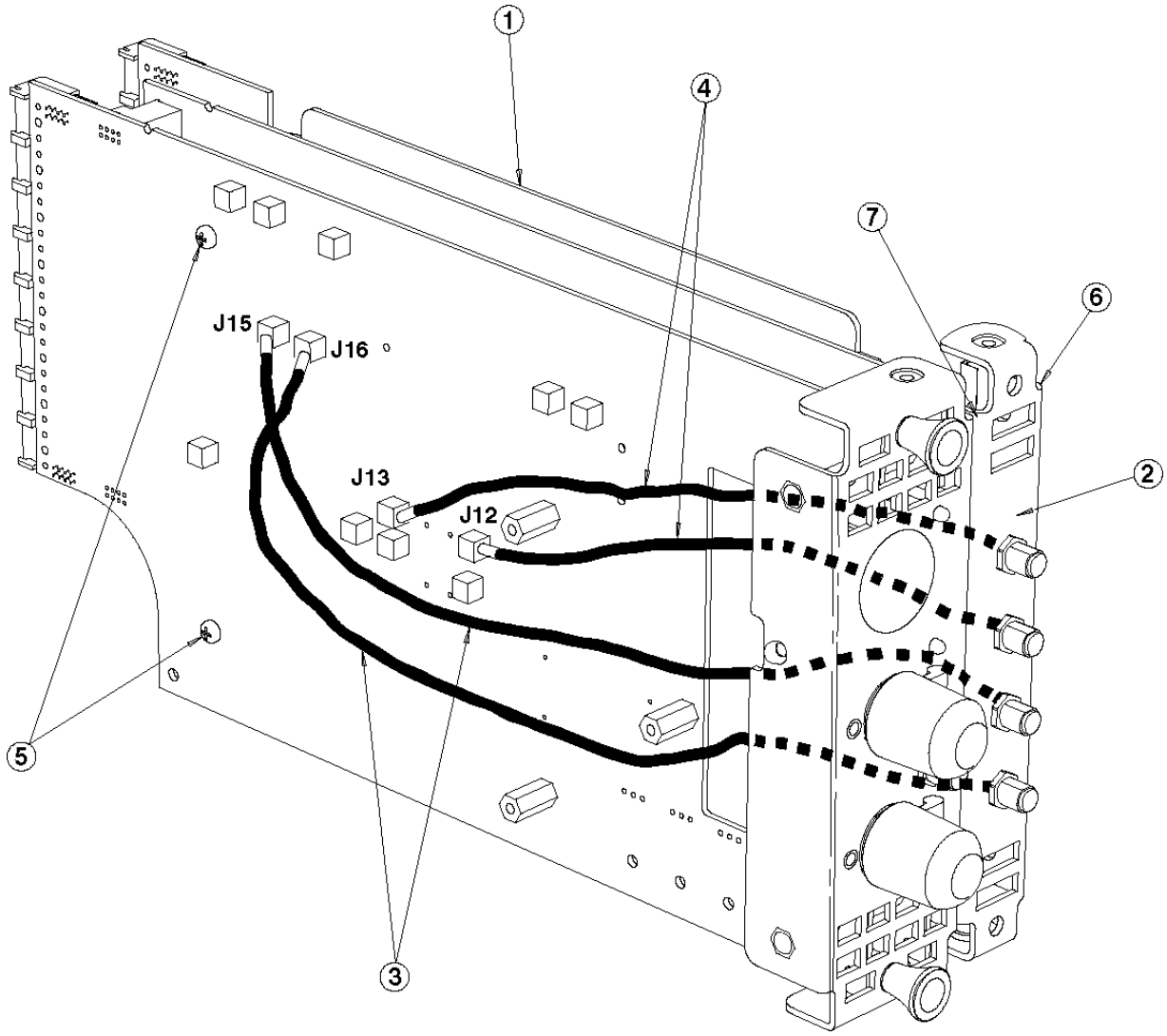


Figure 5-13 SDH Binary Interface Module - Exploded View

PDH Jitter Receiver Module

This module has one board assembly, A13.

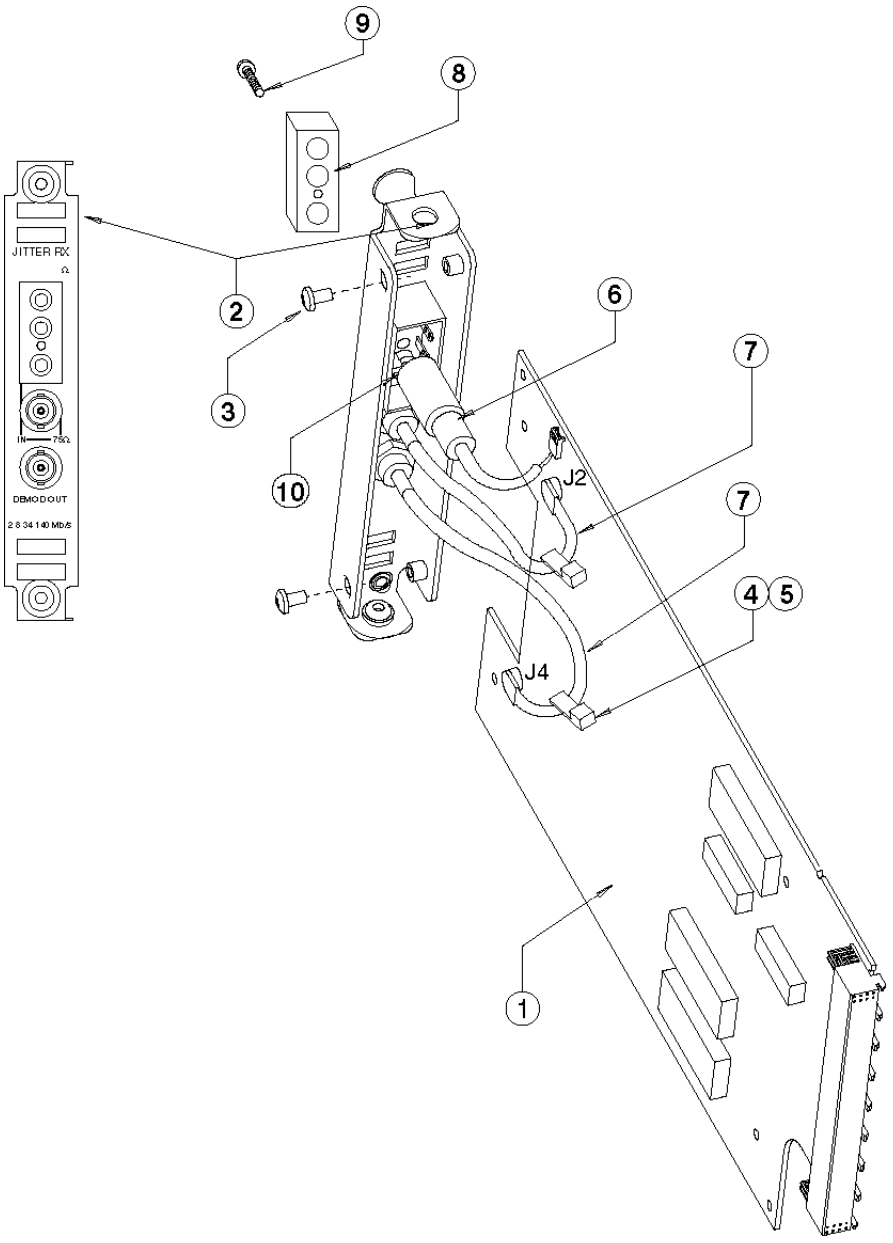


Figure 5-14 Jitter Rx Module - Exploded View

Servicing the Module

The single board assembly can be replaced by following the procedure below.

1. Remove the module from the HP 37717C.
2. Unscrew the two front screws which secure the board to the module metalwork.
3. Unplug any cables from the board assembly.
4. Remove the board taking care not to damage any cables or lose the screws/spacers.

STM-1e Jitter Rx module

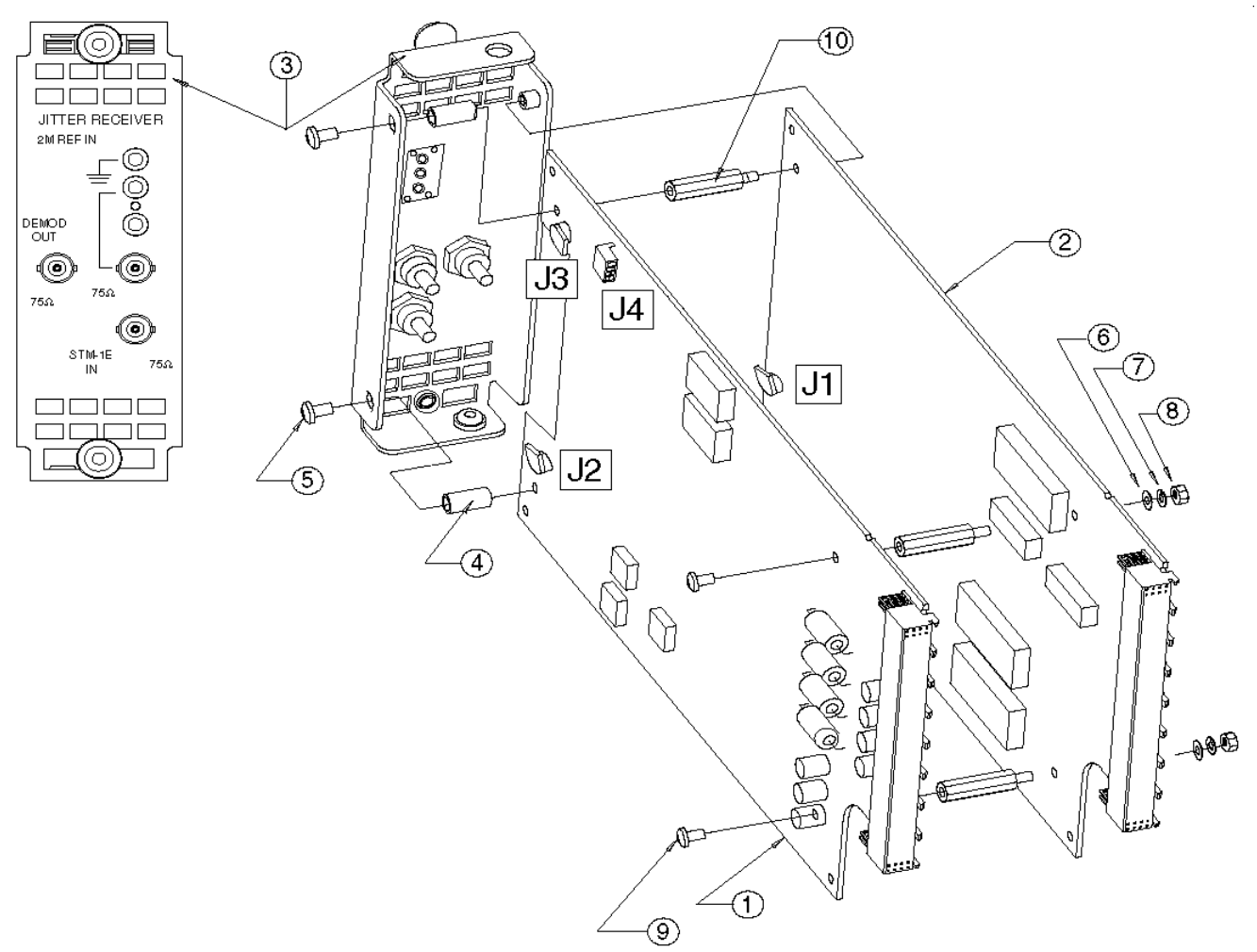


Figure 5-15 STM-1e Jitter Rx Module - Exploded View

STM,1/4-e/o Jitter Rx Module

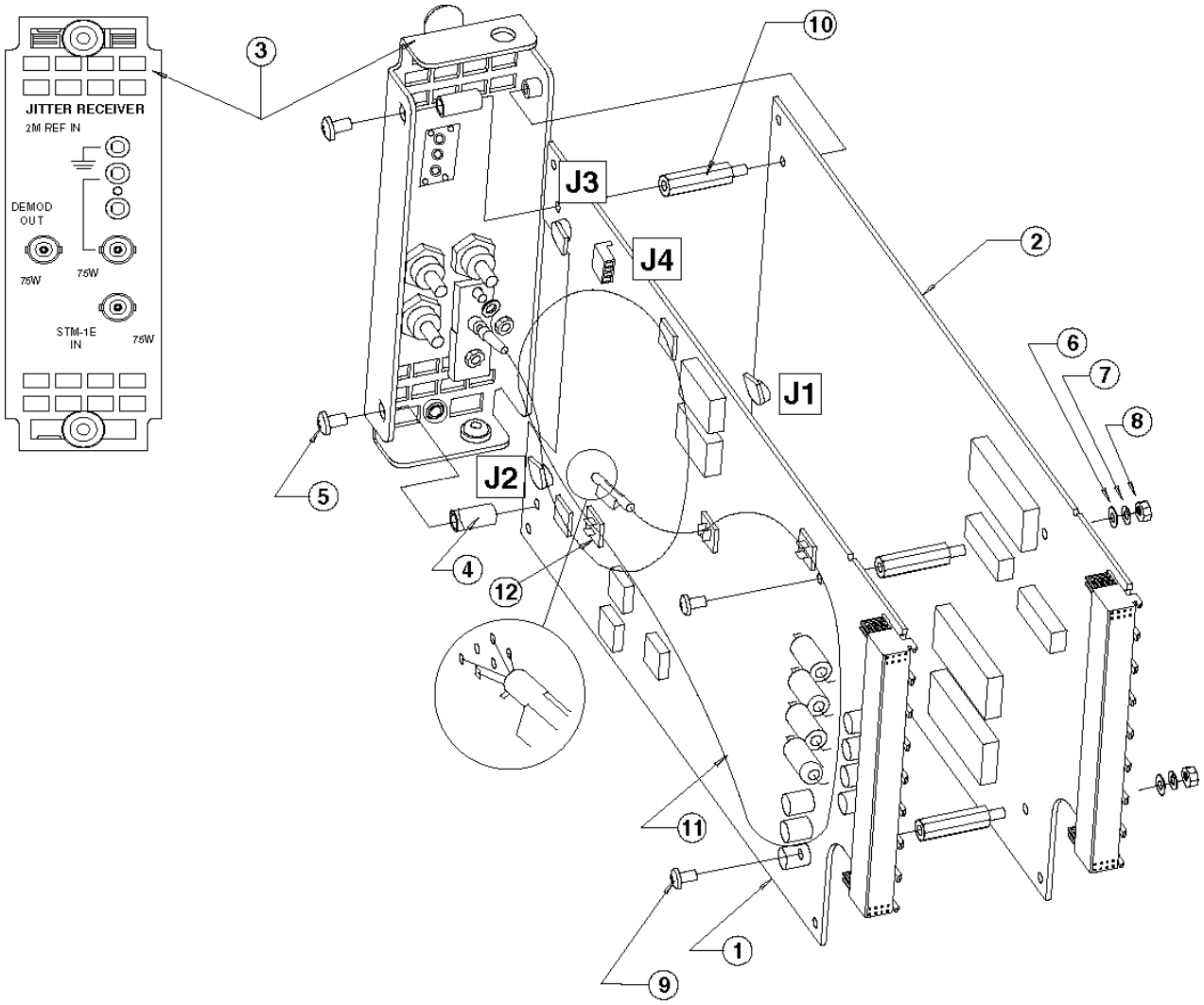


Figure 5-16 STM,1/4-e/o Jitter Rx Module - Exploded View

Jitter Transmitter Module (Option UHK)

This module has one board assembly, A12.

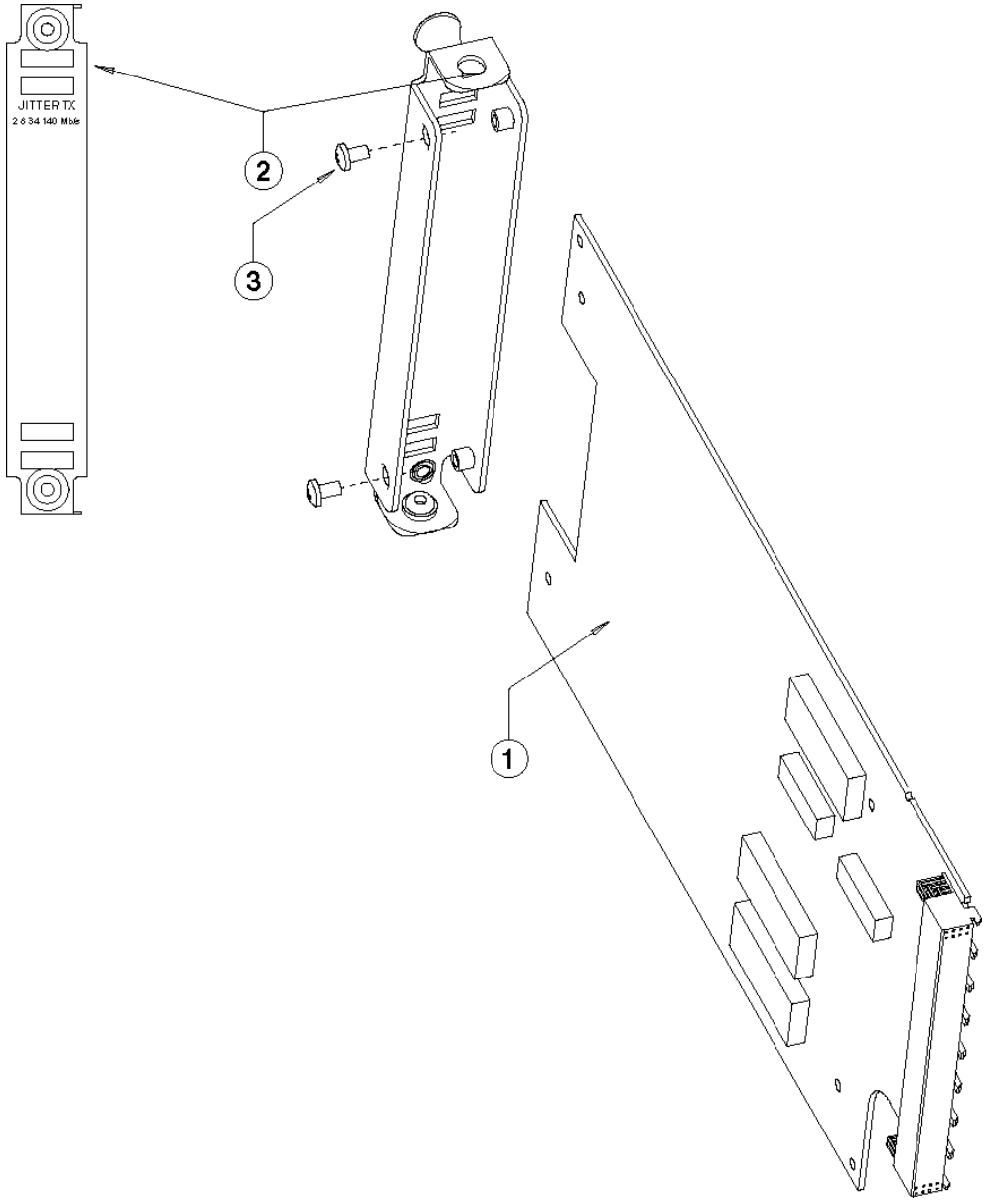


Figure 5-17 Jitter Tx Module - Exploded View

Servicing the Module

The single board assembly can be replaced by following the procedure below.

1. Remove the module from the HP 37717C.
2. Unscrew the two front screws which secure the board to the module metalwork.
3. Unplug any cables from the board assembly.
4. Remove the board taking care not to damage any cables or lose the screws/spacers.

Jitter and Wander Transmitter

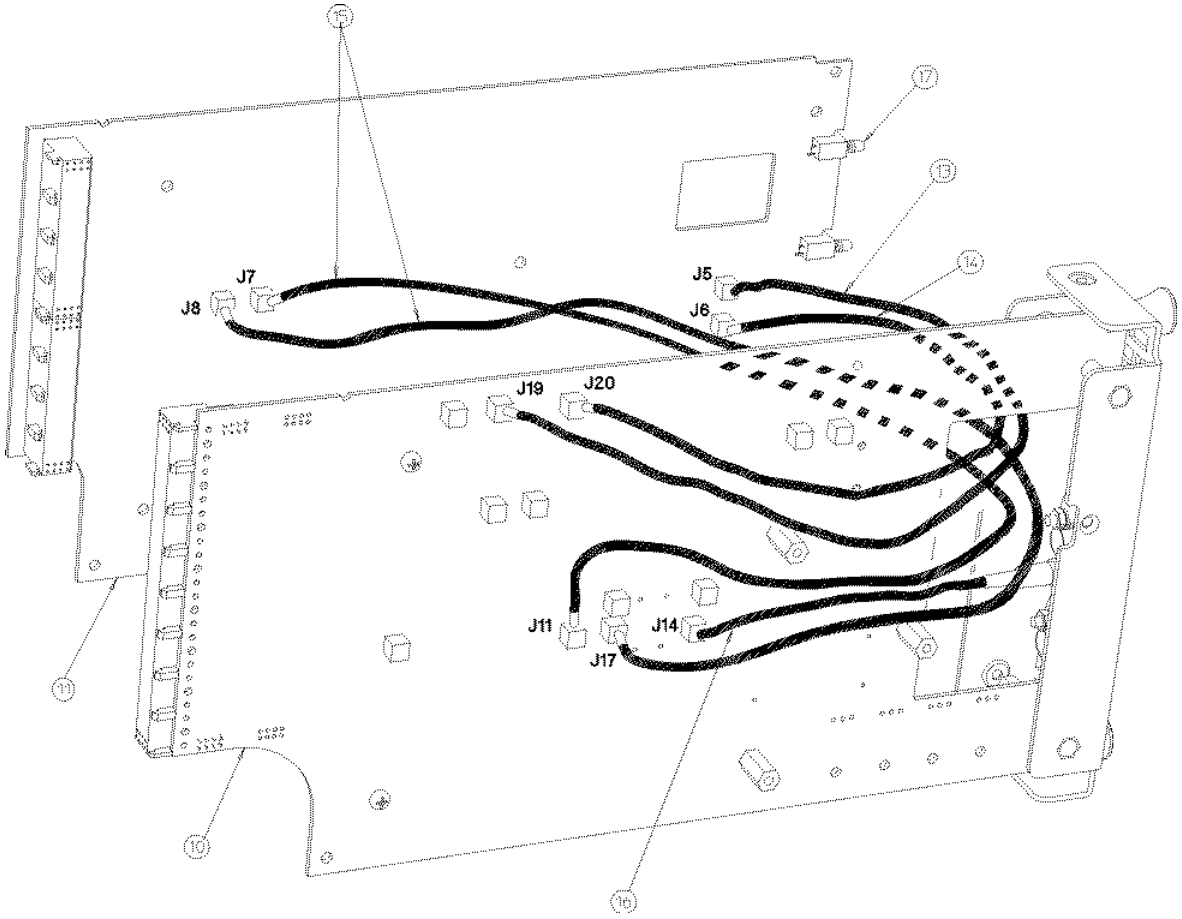


Figure 5-18 Jitter and Wander Transmitter - Exploded View

Multiple Outputs Module

This module has one board assembly, A14.

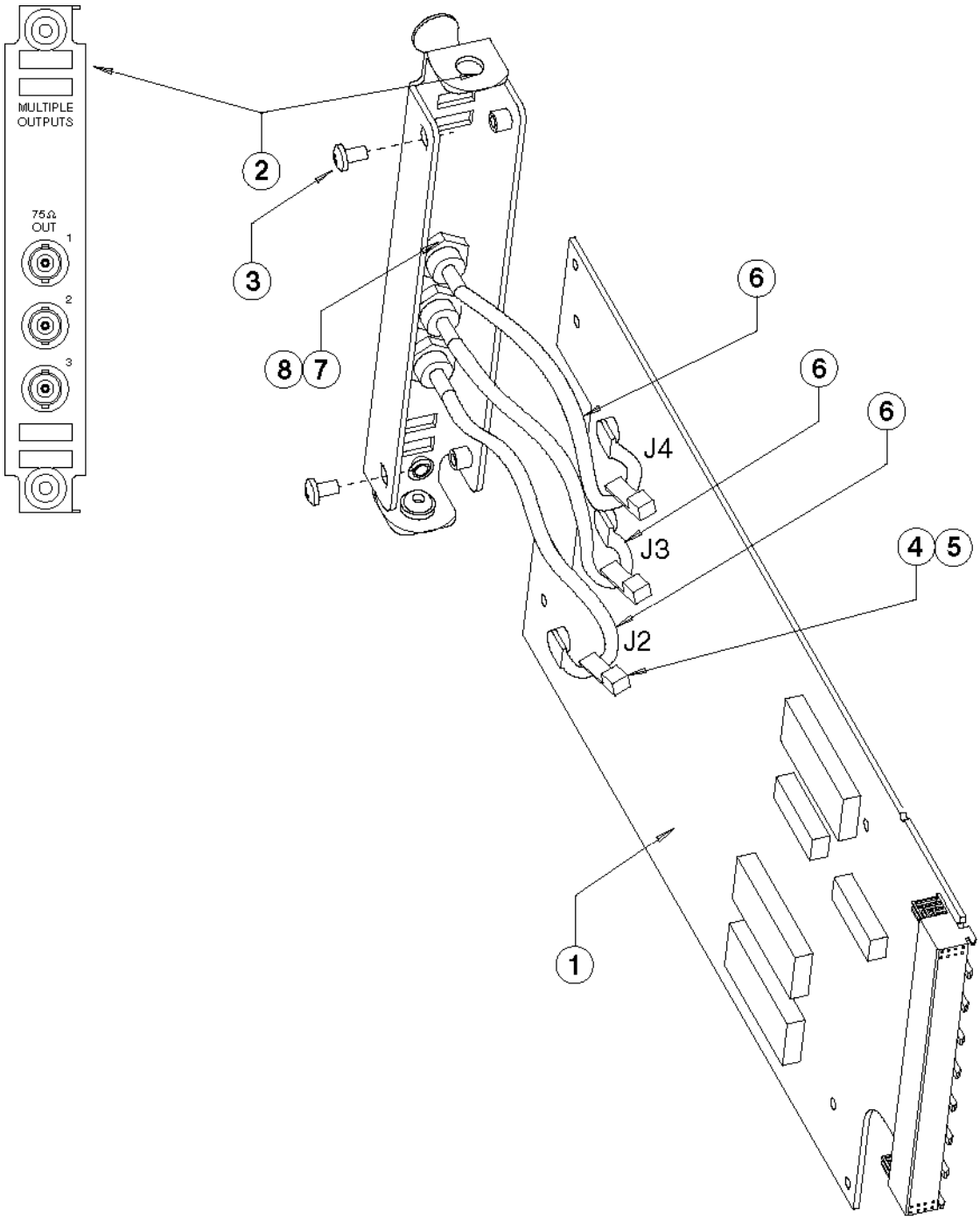
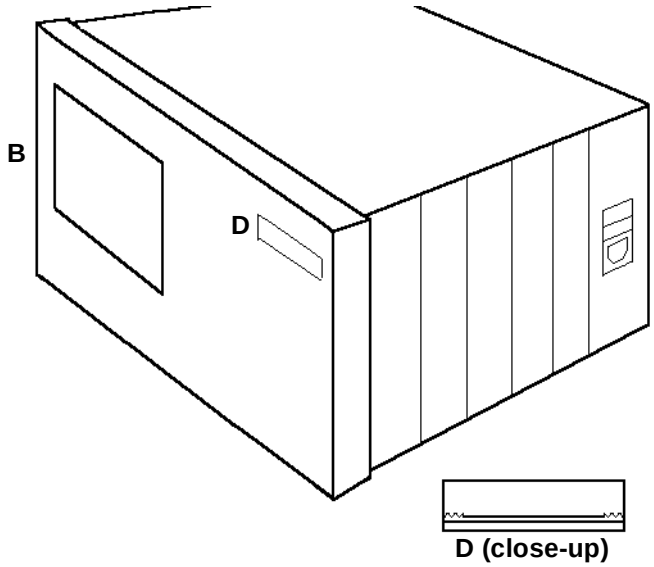


Figure 5-19 Multiple Output Assembly - Exploded View

Front Panel Assembly

The HP 37717C Front Panel Assembly consists of an OEM Colour Display and two board assemblies, A1 and A2. All these assemblies are clamped to the front panel which also contains a membrane keyboard panel.



Servicing the Front Panel Assembly

The Front Panel can be dismantled for servicing by following the procedure below.

1. Remove the power cord and any interconnecting cables. Place the instrument face down on the workbench.
2. Remove the 4 screws securing the rubber feet to the rear panel.
3. If Optical Interface Module is fitted the Input and Output Connector plastic laser shields must be removed. Unscrew the centre knurled nut and pull the shield away from the connector.
4. The instrument case can now be drawn back over the instrument frame and placed to one side.
5. Remove the 4 screws which retain the front panel to the instrument case.
6. Disconnect the 60-Way ribbon cable from the Motherboard and lift the complete Front Panel Assembly out of the instrument.

Removing the A1 Assembly

1. Undo the 5 screws securing this assembly to the Front Panel
2. Unplug the 50-Way ribbon cable and lift the A1 assembly clear of the front panel.

Removing the A2 Assembly

1. Undo the 4 highlighted screws securing this assembly to the Front Panel
2. Unplug the 12-Way ribbon cable and lift the A2 assembly clear of the front panel complete with the ELD Display board assembly.
3. The ELD Display Assembly can be separated from the A2 Assembly by undoing 4 screws and unplugging the 16-Way ribbon cable from A2.

PSU Module

The HP 37717C uses an OEM power supply module.

Servicing the Module

The procedure below should be used to access this module for replacement.

1. Remove all modules from the instrument as described previously.
2. Remove the Front Panel Assembly from the instrument as described previously.
3. Unplug the heavy-duty 5-way and 8-way ribbon cables which interconnect the PSU and the A3 (motherboard) assembly.
4. Unplug the PSU Line Supply cable.
5. Unscrew the 4 screws which secure the PSU Assembly to the instrument Rear Panel.
6. Unscrew the 4 screws which secure the PSU heatsink to the instrument chassis.

CAUTION These screws are Imperial Thread - all others are metric.

7. The PSU Module can now be lifted out of the instrument.

CAUTION Take care when fitting the module line supply cable as this can be fitted back-to-front into the socket on the PSU Assembly with possible damage to the board (supply grounded).

Line Module

The above module contains the Line Filter, Mains Socket with fuse and ON-OFF Switch mounted on a metal plate located on the right-side of the instrument chassis.

1. If a component needs to be replaced the best solution is to replace the complete Line Module as all components are secured by rivets which are difficult to replace.
2. To remove the Line Module, unscrew the six screws which secure it to the chassis and draw it out of the instrument after disconnecting the interconnecting cables.
3. Connect the new Line Module and secure with the six screws.
4. Remove all modules from the instrument as described previously.
5. Line components are now accessible for testing.

Cooling Fans

There are two cooling fans fitted to the HP 37717C. A Rotary Fan attached to the PSU module and a Barrel Fan which is used to cool the modules and Front Panel components. This fan is run from 12 volt DC and is located on the left-side chassis panel.

Accessing Cooling Fans

Use the procedure below if the Barrel fan needs to be accessed for testing or replacement.

NOTE The Rotary fan is part of the PSU Module. If this is not turning, and the supply voltage is good, the complete PSU Module must be replaced (see replacement parts section).

1. Remove all modules from the instrument as described previously.
2. Remove the Front Panel Assembly from the instrument as described previously.
3. Remove the PSU Assembly from the instrument as described previously.
4. Unplug the rotary fan connector from the A3 Assembly.
5. Remove the two screws which secure the rotary fan to the chassis and lift the fan out of the instrument.
6. Unplug the Barrel fan connector from the A3 Assembly.
7. Remove the four screws which secure the Barrel fan to the chassis and lift the fan out of the instrument.
8. The replacement is a reversal of the above.

Appendix A - Default Settings

Default settings

It is often desirable to store measurement settings which are used regularly and be able to recall those settings at a moments notice. This capability is provided in the HP 37717C on the OTHER STORED SETTINGS display.

One preset store is provided which cannot be overwritten, STORED SETTING NUMBER [0], and is used to set the HP 37717C to a known state. The known state is the FACTORY DEFAULT SETTINGS as listed below.

Signal	140 Mb/s	Clock Sync	Internal
Code	CMI	Pattern	2^{23}-1
Termination	75 [ohm] Unbal		

Signal	STM-1	Clock Sync	Internal
Payload	140 Mb/s	Payload Pattern	2^{23}-1
TUG3	1	TUG2	1
TU	1	2 Mb/s Pattern	2^{15}-1

Jitter	OFF	Jitter Mask	OFF
Frequency	1000 Hz	Range	1.0 UI
Amplitude	1.00 UI		

Signal	140 Mb/s	Test Mode	Out of Service
Code	CMI	Pattern	2^{23}-1
Termination	75 [ohm] Unbal		

Signal	STM-1	Payload	140 Mb/s
Payload Pattern	2^{23}-1	TUG3	1
TUG2	1	TU	1

Range	1.6 UI	Hit Threshold	1.00 UI
Filter	OFF	Wander Ref	75 [ohm] Unbal
Ref Format	HDB3 Data		

Results	Trouble Scan	Short Term Period	1 Second
Test Timing	Manual	Single Test Duration	1 Hour
Storage	OFF	SDH Results	Short Term, RS B1 BIP
PDH Results	Short Term	Jitter Results	Cumulative, Hits
Wander Results	Wander		

Stored Setting Lock	On	Stored Setting Number	0
Printer	Internal	Printing	Off
Print Period	OFF	Print Error Seconds	OFF
Print Mode	Normal	Print Speed	9600 Baud
Clock Mode	Run	Keyboard lock	OFF
Beep On Error	OFF	Analysis Display Mode	G.821
Suspend Test on LOS	OFF	Self Test	All Tests
Settings Control	Independent		

Register	+ve Transition	-ve Transition	Enable
ESR	All 1's	All 0's	All 1's
QUES	All 1's	All 0's	All 0's
OPER	All 1's	All 0's	All 0's
INST	All 1's	All 0's	All 1's
DATA	All 1's	All 0's	All 1's
PDH	All 1's	All 0's	All 1's
FAS	All 1's	All 0's	All 1's
SDH	All 1's	All 0's	All 1's
SDH2	All 1's	All 0's	All 1's

Appendix B - Service Notes

SERVICE NOTE 37717C-01A

HP 37717C PDH/SDH/Jitter Test Set

Serial Numbers : N/A
Firmware Revision : Below A.01.05
Title : Upgrading the Instrument Firmware.
To be Performed by : Qualified Service Personnel
Date: August 1996

Parts Required

Description	HP Part Number	Quantity
Set of firmware Upgrade discs	Contact Product Support	01

Situation

A new revision of firmware is available for the HP 37717C.

This revision adds the following new features:

- Full operational capability of the disc-drive.
- Operation of the Centronics Printer Interface (Option A3B or A3D)
- Operation of the LAN Interface where fitted (Option A3B).
- Elimination of a number of minor bugs which were present in earlier versions.

It is recommended that all units with firmware Revision Number below that listed above be upgraded with new firmware.

NOTE If option A3B is fitted, this will need to be enabled after the firmware has been upgraded to get the LAN Interface capability.

ADMINISTRATIVE INFORMATION

Service Note Classification : MODIFICATION RECOMMENDED

Procedure

Before updating the firmware, confirm the Revision fitted to your instrument.
The FIRMWARE REVISION number appears on the [REMOTE/PRINTER] options page.
Access this page as follows;

1. Press the OTHER key then [MORE] softkey until a softkey labeled [OPTIONS] is dis-

played.
2. Press the [OPTIONS] softkey then select [REMOTE/PRINTER] Options. The MAIN and AUX firmware numbers will be displayed at the bottom of this page.
3. Check the Main Firmware Revision Number. If this is in the affected range, use the following upgrade procedure to install the new firmware.

Upgrading the Firmware

Use the following procedure to upgrade the firmware in the HP 37717C.

1. Power on the instrument and check for a valid display.
2. Press OTHER key, then [MORE] softkey then select the [CALIBRATION] function.
3. Select CALIBRATE PASSWORD and using the DECREASE DIGIT and INCREASE DIGIT softkeys set the password to [1243]
4. Select CALIBRATION ITEM : [FIRMWARE UPGRADE].
5. Fit Disc 1 (from the set of discs supplied in this kit) into the disc drive slot with the disc label facing towards the instrument Front Panel.
6. Answer each question displayed on the screen using the appropriate keys. When you have answered all questions, the instrument will commence downloading data from Disc 1. This process will take from 5-10 minutes.

NOTE Select **<Program>** when asked if you want to verify the discs. Verification is **not** required.

When data transfer from Disc 1 is complete, the display will show:

Insert next disc & press any key
Use <single error key> to abort update.

7. Repeat steps 5 to 6 with the other discs supplied in the Retrofit Kit.

When data transfer from the last disc is complete, the display will show:

To use new code press any key
Use <single error key> to abort update.

8. Press TRANSMIT key to initialize the instrument.
9. After initialization. press TRANSMIT key again to restart the instrument.

The firmware upgrade is now complete.

Enabling the LAN Interface (Option A3B)

If an option A3B label is fitted on the instrument rear panel, then the LAN Interface hardware will already be fitted. To use the hardware, you will need to **DISABLE** the option A3D in the instrument memory and **ENABLE** the option A3B instead.
Do this as follows;

Disabling A3D

1. Switch on the instrument.
2. Make the following key sequence to obtain the OPTION ENABLE display.
   Press [OTHER]; [<^]; [MORE]; [<^]; [MORE]; [<^]; [MORE]; [OTHER].
   Press [MORE] until OPTION ENABLE appears in the softkey menu.
3. Press OPTION ENABLE softkey.
4. Move cursor down one place and select the option to be added.
5. Move cursor down one place and select [NOT FITTED].

6. Move cursor to CODEWORD field and insert the special codeword into this field using the [<],[>], and [INCREASE DIGIT], [DECREASE DIGIT] softkeys.

37717C SERIAL NUMBER .....

OPTION TO BE REMOVED ..... A3D .....

CODEWORD .....

NOTE This CODEWORD is unique to every 37717C unit and can only be obtained by contacting the HP QTO Division Product Support Engineer

7. Move the cursor to TOGGLE TO SET OPTION field and enable the option by pressing the [SET OPTION] softkey. The display will flash momentarily and the message "Option Structure Changed" will be displayed. The unit will assume Default Settings.
8. Press the OTHER key then [MORE] softkey until softkey labeled [OPTIONS] is displayed.
9. Press the [OPTIONS] softkey and ensure that A3D has been removed.

Adding A3B

1. Switch on the instrument.
2. Make the following key sequence to obtain the OPTION ENABLE display.
   Press [OTHER]; [<^]; [MORE]; [<^]; [MORE]; [<^]; [MORE]; [OTHER].
   Press [MORE] until OPTION ENABLE appears in the softkey menu.
3. Press OPTION ENABLE softkey.
4. Move cursor down one place and select the option to be added.
5. Move cursor down one place and select [NOT FITTED].
6. Move cursor to CODEWORD field and insert the special codeword into this field using the [<],[>], and [INCREASE DIGIT], [DECREASE DIGIT] softkeys.

37717C SERIAL NUMBER .....

OPTION TO BE ADDED ..... A3B .....

CODEWORD .....

NOTE This CODEWORD is unique to every 37717C unit and can only be obtained by contacting the HP QTO Division Product Support Engineer

7. Move the cursor to TOGGLE TO SET OPTION field and enable the option by pressing the [SET OPTION] softkey. The display will flash momentarily and the message "Option Structure Changed" will be displayed. The unit will assume Default Settings.
8. Press the OTHER key then [MORE] softkey until softkey labeled [OPTIONS] is displayed.
9. Press the [OPTIONS] softkey and ensure that A3B has been added.

Checking the LAN Interface MAC Address (Option A3B only)

Every instrument shipped with Option A3B LAN interface has a unique MAC address associated with it. This address is stored in the instrument memory at the factory and should not require changing during the life of the instrument.
Check the MAC address in memory after enabling option A3B by carrying out the following procedure:

1. Switch on the instrument and press the OTHER key then [MORE] softkey. Select the [CAL-

IBRATION] function.
2. Select CALIBRATE PASSWORD and set to [1243] using the INCREASE DIGIT and DECREASE DIGIT softkeys.
3. Select the calibration item [SET MAC ADDRESS].

The MAC Address is displayed at the bottom of this page.

37717C SERIAL NUMBER .....

MAC ADDRESS .....

If the MAC Address displayed on the instrument is different to that shown here, then you will need to change it as follows;

4. Move the cursor to the [MAC ADDRESS EDIT] field and change the address to that shown above using the INCREASE DIGIT and DECREASE DIGIT softkeys.
5. Move the cursor to the [ACCEPT CHANGES] field and press the ON softkey.
6. Ensure the change is reflected at the bottom of the display.

Testing

1. Power on the instrument and check for a valid display.
2. Obtain a pass on all instrument Selftests.

The instrument is now ready for use.

SERVICE NOTE 37717C-02

HP 37717C PDH/SDH/Jitter Test Set

Serial Numbers : N/A
Firmware Revision : Below 3605 (Main).
Title :Fatal Error 326 When Attempting to Print Graphics.
To be Performed by : Qualified Service Personnel
Date: March 1996

Parts Required : Refer to Service Note 37717C-01

Situation

A firmware bug exists in early revisions which can cause Fatal Error 326 when attempting to print Jitter graphics.

Solution/Action

Confirm the Firmware Revision fitted to the instrument using the following procedure:

1. Press the OTHER key then [MORE] softkey until a softkey labeled [OPTIONS] is displayed.
2. Press the [OPTIONS] softkey then select [REMOTE/PRINTER] Option.

The MAIN and AUX firmware numbers will be displayed at the bottom of this page.
If this is in the affected range, upgrade the firmware to the latest revision by following the procedure in Service Note 37717C-01.

ADMINISTRATIVE INFORMATION

Service Note Classification : MODIFICATION RECOMMENDED

SERVICE NOTE 37717C-03

HP 37717C PDH/SDH/Jitter Test Set

Serial Numbers :GB00000000 to GB99999999
Build Status : 1.00 and above
Title : Replacing the Processor Assembly (CPU)
To be Performed by : Qualified Service Personnel
Date: October 1996

Parts Required

Description	HP Part Number	Quantity
Replacement Processor Kit	37717-60159	01

Situation

This Service Note gives information on parts and instructions required when changing a processor on the HP 37717C

Action

When changing the processor order the appropriate part from the table above and use the following procedure to fit it;.

NOTE If you are unsure what to order, or have problems fitting the above parts, please contact your HP representative or QTO Product Support on +44 131-331-7224.

ADMINISTRATIVE INFORMATION

Service Note Classification : INFORMATION ONLY

Use these instructions when replacing the CPU on a HP 37717C .
The instructions cover the following;

- Correct procedure for removing the old CPU Module from the instrument.
- Procedure for transferring the special Memory IC from the old CPU Assembly.
  This IC stores information on the option structure of the instrument and all soft calibration constants for the instrument. Transferring this IC means that it is not necessary to recalibrate the instrument or replace firmware options.
- Procedure for assembling the new CPU Board into the Module and replacing in the Instrument.
- Checking Options and Calibration Dates.
- Setting the Internal Clock Time and Date.
- Testing the instrument with the New CPU.
- Changing the MAC address Label (applies to option A3B units only).
  Every instrument shipped with Option A3B LAN interface has a unique MAC address associated with it. This address is stored in U15 on the CPU, so will be transferred over with U15 (see above). There is also a label fitted to the old CPU with this unique address which must also be transferred.

WARNING **The CPU board contains a battery. To prevent overheating or an explosion. DO NOT expose to high temperatures or short circuit.**

CAUTION These procedures should only be carried out by qualified Service Personnel. Anti-static precautions must be observed at all times. - Use the anti-static wrist-strap provided in this kit if an anti-static work-area conforming to Corporate Standard 741.808 is unavailable.
Read the anti-static documentation at the end of this procedure.

Removing the old CPU Assembly.

Remove the old CPU Assembly as follows:

1. Switch off the instrument and disconnect the power cord and any interconnecting cables.
2. Place the instrument face down on the workbench.
3. Remove the 4 screws securing the rubber feet to the rear panel.
4. If Optical Modules are fitted, unscrew optical shield from the input and output connectors.
5. Withdraw the outer cabinet sleeve back and out of the instrument.
6. Remove the two clamp screws on the top and bottom right-hand side of the chassis which secure the CPU module.
7. Withdraw the CPU module from the instrument using the two knobs to help with removal.

Transferring the Memory IC from the old CPU Board Assembly

On the old CPU Module

1. Unscrew the posidrive screws which secure the Disk Drive with it's metal shield to the disk-drive supports on the CPU Board.
2. Unscrew the two nuts which secure the PARALLEL Interface Connector to the module Front Panel.
3. Unclip the HP-IB, RS-232 and Disk-Drive ribbon cables from their sockets on the CPU board Assembly.
4. Using a long posidrive screwdriver, unscrew the two screws which secure the module Front Panel to the CPU Board.
5. Remove the module Front Panel together with the disk-drive assembly and metal shield and place to one side in an anti-static bag.
6. Locate U15 (marked on the topside of the board) and carefully remove this IC from it's socket using a Quilext 1 Universal IC Extraction tool or equivalent.

On the new CPU Module

1. Fit U15 from the old CPU into the socket on the new CPU assembly taking great care not to touch any pins on the IC or socket. Ensure correct alignment before pushing firmly home in the socket.

NOTE You MUST discard any IC in the new module fitted into U15 position and replace with the part from the old module. This memory IC contains option and calibration data UNIQUE to your instrument.

NOTE You may need to repeat steps 1 to 6 above to access this IC on the new CPU.

2. Once this IC has been fitted, check the switches on the new CPU Assembly are set as follows:

Assembly Description	Switch Number	Finger Number	Position
A4 Processor Assembly	SW1	1,2 & 4	Closed
A4 Processor Assembly	SW1	3	Open
A4 Processor Assembly	SW2	1,3,4,6,7,8	Closed
A4 Processor Assembly	SW2	2 & 5	Open

Transferring the LAN Interface MAC Address Label (Option A3B only)

1. Check the instrument rear panel to see if option A3B (LAN Interface) is fitted. If it is, there will be a MAC ADDRESS label stuck to the rear of the old CPU board. Write down the number on this label (this will be keyed into the CPU memory later), then remove the label and attach it to the new CPU board in the same position.

Fitting the CPU Module and Re-assembling the Instrument.

1. Replace the CPU module back into the instrument.

IMPORTANT NOTE:

NOTE To prevent removal of, or damage to the metal RFI STRIP on the module next to the CPU, you MUST use special tool hp part number 03776-00016 or a thin LOW-STATIC plastic or fibre card (200mm x 135mm x 0.5mm) when inserting the CPU module back into the instrument. Place this card against the RFI Strip, then slide the CPU Module back into the instrument. Push the CPU Module fully home, then pull out the card - see Figure B-1.

CAUTION Severe damage can result if an RFI Strip is dislodged and falls inside the instrument. Always ensure that RFI strips are securely in position and unbroken.

2. Replace the outer cabinet sleeve, optical module shields and rear panel feet - this is a reversal of the removal procedure.

Downloading New firmware (Option UKZ or USK only)

The new processor has already be loaded with the current revision of firmware. This is applicable to all options **EXCEPT options USK or UKZ**. If either (or both) of these options is fitted to your instrument, you will need to download the new firmware using the disks supplied in this kit Use the procedure described in Service Note 37717C-01 to do this.

Checking Options and Calibration Dates.

1. Switch on the instrument and check for a valid power-up routine.
2. Press the OTHER key, then [MORE] softkey until [OPTIONS] softkey is displayed.
3. Press the [OPTIONS] softkey and select each option type in turn (i.e PDH, SDH, JITTER, ATM etc).
4. Ensure that the options shown as FITTED on the display agree with the options listed on the instrument rear panel.
5. Press the [MORE] softkey until [CALIBRATION] softkey appears at the bottom of the display.
6. Enter the Calibration password [1243].
7. Select each Calibration Item and ensure the calibration dates are valid.

NOTE An annual Calibration cycle is recommended for the HP 37717C

Setting the Internal Clock Date and Time

You will need to set the internal clock to the correct time and date as this will be incorrect after changing the CPU.

1. Switch on the instrument.
2. Press OTHER key, then [MORE] softkey until [TIME & DATE] softkey is displayed.
3. Press [TIME & DATE] softkey then move the cursor to CLOCK MODE.
4. Select [SETUP] then move the cursor to TIME. Set the clock to the correct time using [<],[>], and [INCREASE DIGIT], [DECREASE DIGIT] softkeys.
5. Move the cursor to DATE. Set the clock to the correct date using [<],[>], and [INCREASE DIGIT], [DECREASE DIGIT] softkeys.
6. Return the cursor to CLOCK MODE and press [RUN].

The internal clock is now set.

Checking the LAN Interface MAC Address (Option A3B only)

Check the MAC address in memory after ensuring option A3B is enabled (see above) by carrying out the following procedure:

1. Switch on the instrument and press the OTHER key then [MORE] softkey. Select the [CALIBRATION] function.

2. Select CALIBRATE PASSWORD and set to [1243] using the INCREASE DIGIT and DECREASE DIGIT softkeys.
3. Select the calibration item [SET MAC ADDRESS].

The MAC Address is displayed at the bottom of this page. If it is different to that on the label which you transferred from the old CPU, then you will need to change it as follows;

4. Move the cursor to the [MAC ADDRESS EDIT] field and change the address to that shown above using the INCREASE DIGIT and DECREASE DIGIT softkeys.
5. Move the cursor to the [ACCEPT CHANGES] field and press the ON softkey.
6. Ensure the change is reflected at the bottom of the display.

Testing

Perform all the instrument selftests.

NOTE It is very important to cable the instrument correctly when running the selftests. Cabling depends on options fitted - see Calibation or Service Manual for this information.

When a pass has been obtained on all selftests the instrument is ready for use.

Important Operational Note

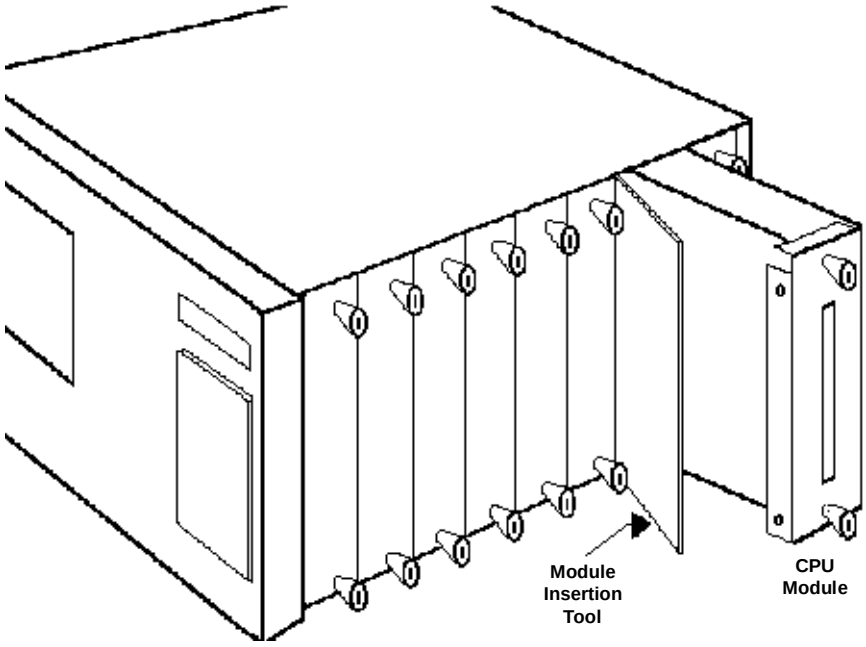


Figure B-1 Position of Processor Module and Insertion Tool

If the new CPU is pre-loaded with firmware version A.01.62 **AND** .....
Your instrument contains options A1M,A1N,A1P (or the equivalent options with small siemens connectors), you will find the Jitter receive menu contains a selectable HP2 filter on SDH rates.
This filter should always be set OFF in the menu as the filter hardware is NOT fitted.
This inappropriate selection is due to a firmware bug in version A.01.62 ONLY.

SERVICE NOTE 37717C-04

HP 37717C PDH/SDH/Jitter Test Set

Serial Numbers : GB00000000 to GB99999999
Title : Swapping Modules Between Instruments
To be Performed by : Qualified Service Personnel
Date: December 1996

Situation

Use the following information if you need to swap one or more modules from an HP 37714A, HP 37717A, HP 37717B or HP 37717C instrument into an HP 37717C instrument.

Action

Confirm the module(s) you want to swap and check for any problems and all other relevant information from the list below.

NOTE Modules must be fitted in the positions shown in Table B-1 and Figure B-2.

CAUTION To prevent removal or damage of the metal RFI strips fitted on the side of each module you must remove all the modules in front of the one to be swapped, then replace the modules working from the back of the instrument to the front.
Severe damage can result if an RFI Strip is dislodged and falls inside the instrument. Always ensure that RFI strips are securely in position and unbroken.

ADMINISTRATIVE INFORMATION

Service Note Classification : INFORMATION ONLY

Optical Modules (Option UH1, UH2, URU, UKT, USN, A3T, A3U)

Remember, when testing Option URU and also the 1550 nm transmit port from Option USN or A3T, you will need to attenuate the output signal with an optical attenuator when running the back-to-back tests. You do not need the attenuator with UH1 or UH2. Information on this is in the Service Manual and Calibration Manual.

SDH Modules (Option US1, US9, A1T, A1U, A3R)

If the later Jitter Transmit module (Option A3K) is fitted, unmodified US1 or A1T Modules will limit SDH Jitter transmit frequency to 4MHz (5MHz is required for G825 testing).
If the earlier Jitter Transmit module (Option UHK) is fitted, modified US1 or A1T Modules may not operate correctly. These modifications were introduced at Build Status
Also note that a special RS449 looping link is required when running the INDIVIDUAL A1T selftest but NOT the ALL TESTS.

Unstructured PDH Modules (Option UKK, USB)

No problems in swapping any of these modules between instruments but you should check the RECOVERED CLOCK CALIBRATION is OK - see Service Manual.

Structured PDH Modules (Option UKJ, USA)

No problems in swapping any of these modules between instruments but you should check the

RECOVERED CLOCK CALIBRATION is OK - see Service Manual.

ATM Modules (Option UKN)

ATM HAS THE SAME HARDWARE AS Structured PDH, so check on the options page that UKN is fitted. If not, you will need to contact the factory for the special Retrofit Kit to enable ATM firmware features. - there is a charge for this kit.

Services Module (Option USK)

Currently, this has a unique revision of firmware, so will not operate in an instrument without updating the firmware. Currently, it will not operate along with Jitter Transmit or Receive modules. Both these limitations are expected to be resolved early 1997.

Binary Interface Module (Option UH3)

You should check the binary levels and mark to space ratios are within specification - there is a procedure in the latest calibration manual. A modification was introduced to the PDH Module from Build Status 1.21 to ensure all Binary Interfaces met specification.

ETSI/ANSI Module (Option UKZ)

Currently, this has a unique revision of firmware, so will not operate in an instrument without updating the firmware. Currently, it will not operate along with Jitter Transmit or Receive modules. Both these limitations are expected to be resolved early 1997.

Jitter Modules (Option UHK, UHN, A1M, A1N, A1P, A1Q, A1R, A1S)

CAUTION Swapping Jitter Transmit and Receive modules is not recommended.

Jitter Tx and Rx calibration data is unique and is held in the Processor Module (CPU Module). If you swap ONLY the jitter Transmitter module to another unit, the Transmit calibration data will be wrong so you will need to perform Jitter Transmitter Calibration -takes between 30 minutes and 1 hour and needs a Spectrum Analyzer.

If you swap ONLY the jitter Receiver module to another unit, the Receive calibration data will be wrong so you will need to perform Jitter Receiver Calibration - this will take between 30 minutes and 1.5 hours (depending on jitter options fitted) but needs no external equipment - it's fully automatic. If STM-1/4 optical Jitter is fitted (Option A1N, A1P,A1R,A1S), you must also check/set the STM-1 and STM-4 Optical Recovered Clock free-run frequencies.
If you swap BOTH the jitter Tx and Rx Modules, all jitter calibration data will be wrong so you will need to perform both Tx and Rx cal - **always perform the Jitter Transmitter Calibration first.**

NOTE If you do not want to do the calibrations, you can swap the CPU Module and the Jitter Tx/Rx Modules AS A MATCHED SET. but you will now need to recalibrate the 10MHz Reference, and the PDH VCXO,s/ Recovered Clocks (if PDH/ATM fitted). You will also need to check the option structure is the same and enable disable any missing options. To do this, you will need to contact the factory for the special codeword(s)

Jitter Modules (Option A3K, A3L, A3M, A3N, A3P, A3Q, A3V, A3W)

CAUTION Swapping jitter Transmit and Receive modules is not recommended.

The same problems apply as for UHK/A1S.

Processor (CPU) Module

CAUTION Swapping the Processor module is not recommended.

As explained above, all unique calibration data is held in the Processor Module (CPU Module) for Jitter Tx/Rx, Recovered Clocks, VCX0's and all firmware options fitted.
If you swap ONLY the CPU to another unit, all the above cal data will be wrong so you will need to perform a FULL INSTRUMENT CALIBRATION.

Also note that the non disc drive CPU fitted in early versions of the HP 37717B (and Option 705) and the HP 37714A and HP 37717A will not operate in the HP 37717C.

Table B-1 Configurations for the HP 37717C Modules

Module Description	Available Options	Module Width	Fitting Instructions
Optics	UH1,UH2, URU, USN,UKT A3T, A3U	2-slot 2-slot 2-slot	Always Slot 1 - this is a dedicated Optics slot, so cannot be occupied by any other type of module.
SDH Binary In/face	0YH	1-slot	Attached to Option UKT or USN in slot 2
SDH	US1,US5 A1T,A1U A3R	2-slot 2-slot	Immediately to the right ofOptics Module
PDH Multiple Outputs	UHC,US6	1-slot	To right of SDH Module (or Optics if no SDH fitted)
Jitter Transmitter	UHK,A3K A3Q	1-slot 1-slot	To right of PDH Multiple Outputs To right of SDH (if no PDH Multiple Outputs) To right of Optics (if no SDH or PDH Multiple Out)
Unstructured PDH. (single Tx/Rx module) Structured PDH or ATM. (one Tx & one Rx Module)	UKK,USB UKJ, USA	2-slot 1-slot each	To right of Jitter Transmitter, PDH Multiple Outputs, SDH or Optics (see above). As Unstructured PDH - Tx Module is always on left
Services module	USK,USL 0YK	2-slot 1-slot	Between Structured PDH Tx and Rx modules
ETSI/ANSI ATM Tx/Rx	UKZ	1-slot each	Replaces PDH Module(s)
PDH Binary In/face	UH3	1-slot	Immediately to the right of PDH Rx Module
Jitter Receiver	UHN,US9, A1M,A1N A1P,A1Q, A1R,A1S A3L,A3M, A3N,A3P A3V,A3W	1-slot 2-slot 2-slot 2-slot 2-slot 2-slot 2-slot	If Option UH3 fitted, to right of it. If Option UH3 not fitted, to right of PDH Rx Module If PDH not fitted, to right of SDH Module
Blanking Plates -part no. 37714-00013 (single) 37714-00014 (double)	N/A	1 or 2-slot	Fit Blanking Plates at rear (CPU end) to fill any gaps left after fitting all required modules - **there must be no gaps between modules or at instrument front.**

Note 1 : All Options listed in each row of the table are **mutually exclusive** (i.e only one to be

fitted in an instrument).
Note 2 : Optical options need SDH option to operate.
Note 3 : Jitter transmit/receive needs PDH or SDH option to operate.
Note 4 : Jitter transmit option is needed to calibrate Jitter Receiver.
Note 5 : Services Option needs **structured** PDH to operate.
Note 6 : PDH Binary Interface option needs PDH to operate.
Note 7 : SDH Binary Interface is attached to USN/UKT module and needs SDH to operate.

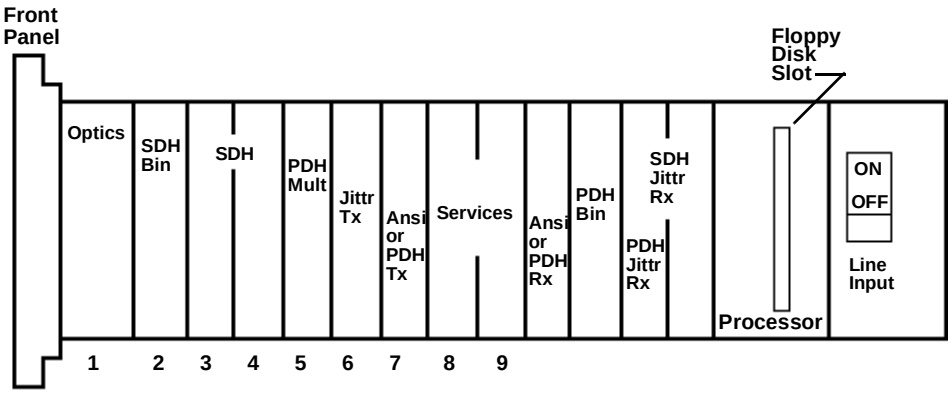


Figure B-2 Location of Modules in HP 37717CMainframe

Rules for Fitting modules

- Left-justify all modules when fitting - i.e. if one or more shown above is not fitted, move others as far left as possible to fill any gaps (EXCEPT for Slot 1 which must only have OPTICS module).
- Modules are 1-slot or 2-slots wide (see Table 2)
- Total module width must not exceed 9 slots.
- If total module width is less than 9 slots, fill gap at right side with Blanking Plates.

Anti-Static Precautions

Watch out for Static Zap !!!
The smallest static voltage which most people can feel is around 3500 volts. It takes less than one tenth of this (about 300 volts) to destroy or severely damage static-sensitive circuits such as those found in the HP 37717C Often, static damage is not sufficient to cause an immediate malfunction. Instead, it can seriously damage a component, resulting in premature failure often at a critical moment when the instrument is most in demand.

The modules fitted to the HP 37717C contain assemblies and components which are sensitive to electrostatic discharge and are not fully screened against this when removed from the instrument. For this reason, you must always follow recommended static-handling procedures when upgrading your HP 37717C with parts from this kit.
By taking the simple precautions below, you can significantly reduce the risk of instrument failure or malfunction caused by static damage.

- Before installing the parts from this retrofit kit, set up a suitable working area where potential static sources are minimised. Avoid working in low-humidity and carpeted areas. Avoid wearing nylon or static-inducing clothing and keep body movement to a minimum.
- Treat all assemblies, components and interface connections as static-sensitive.

- When you unpack this retrofit kit, keep all boards and accessories in their conductive anti-static bags until you are ready to install them.
- Always use the two knobs on the module front panel when removing and installing modules in the instrument. After removal, immediately place the module into a conductive anti-static bag.
- Never touch the module edge connector or any exposed circuitry on the module.
- If possible, wear anti-static clothing and use a controlled-static work station which includes instrument and personnel grounding provisions (HP 9300-0933 or equivalent).
  A typical Workstation will consist of a Table Mat and Floor Mat grounded to a suitable earth in the building, a Wrist Strap attached to the operator's wrist and connected by a flexible cable to the Table Mat and a Heel Strap which should be attached to the operator's foot. A supply of various sized anti-static bags should be on hand and any unprotected assembly should be placed in one of these immediately upon removal.

If a static-controlled workstation is unavailable, minimum protection will be obtained by using the special anti-static wrist strap provided in this upgrade kit. Instructions for using this strap are provided with it.

SERVICE NOTE 37717C-05

HP 37717C PDH/SDH/Jitter Test Set

Serial Numbers : N/A
Options : All
Build Status : 1:14 to 2:64
Title : Instrument Fails to Download Firmware via Floppy disk
To be Performed by : Qualified Service Personnel
Date: March 1997

Parts Required

Description	HP Part Number	Quantity	Build Status Affected
Screened disk-drive Kit	**37717-60190**	**01**	**1:14 to 1:31 (inc)**
Insulated Wire		**0.25 Metre**	**2:41 to 2:64(inc)**

Situation

Problems may be encountered when downloading firmware via disks on HP 37717C units with **Build Status Number** in the above range (the instrument Build Status is recorded on a label attached to the rear panel). Typically a FATAL ERROR may occur during the downloading process.
These problems are due to insufficient RFI screening on the new version of disk drive introduced at BS2:23. Improved screening was introduced into production units at BS2.41.
A wire-link modification to the processor PCB to improve the stability of the disk-drive supply voltage should also be done on these units. This modification was introduced at BS 2:65.

ADMINISTRATIVE INFORMATION

Service Note Classification : MODIFICATION RECOMMENDED

Solution/Action

If any HP37717C unit with Build Status between 1:14 and 2:64 (inclusive) is encountered, carry out the wire-link modification to the processor PCB as described below.
In addition, if the Build Status is between 1:14 and 1:31 (inclusive), order the special **Screened disk-drive Assembly Kit** and fit this by following the procedure below. This specially screened disk drive is more resistant to PSU generated RFI and will prevent the corruption of data which causes the downloading problem to occur.

Procedure

Removing the Processor (CPU) Module

1. Switch off the HP 37717C **and DISCONNECT THE POWER CORD.**
2. Remove the rear panel feet.
3. If Optical Modules are fitted, unscrew the optical shield from the input and output connectors.
4. Withdraw the outer cabinet sleeve back and out of the instrument.
5. Remove the clamp screws on the top and bottom right-hand side of the chassis which secure the CPU Module (see Figure B-3).
6. Withdraw the CPU module from the instrument.

CAUTION Never use a screwdriver or other sharp implement to lever the module as circuit tracks may be cut or the module metalwork irrepairably damaged.

Adding the Wire-Link

1. Remove the processor module as described above.
2. Remove L1 and discard - see Figure B-4.
3. Solder a wire link on the topside of the board as shown in Figure B-4.
4. Using an epoxy resin glue, support the wire link at the points shown in Figure B-4.

The wire link modification is now complete.

Fitting the New Disk Drive Assembly.

If the Build Status is in the affected range, use the following procedure to remove the suspect disk-drive assembly and fit the new Disk-Drive Assembly from the kit.
The old disk-drive is replaced together with the processor front panel as this makes for easier dismantling and assembly procedures and removes the requirement for precision alignment. Follow the steps below;

Dismantling the Processor.

1. Unscrew the four posidrive screws which secure the Disk Drive with it's metal shield to the disk-drive supports on the CPU Board (Figure B-5 item A).
2. Unscrew the nut which secures the Disk Drive to the CPU module front panel (Figure B-5 item B).
3. Unclip the HP-IB and RS-232 ribbon cables from their sockets on the CPU board. Feed the HP-IB ribbon cable out through the slot in the disk drive metal shield.
4. Unclip the disk-drive ribbon cable from it's socket on the CPU board and place the disk-drive and metal shield to one side in an anti-static bag.
5. Unscrew the two nuts which secure the PARALLEL Interface Connector to the module Front Panel (Figure B-5 item C).
6. Using a long posidrive screwdriver, unscrew the two screws which secure the module Front Panel to the CPU Board (Figure B-5 item D).
7. Remove the module Front Panel and place to one side.
8. Unscrew the nuts (Figure B-5 item E) securing the four disk-drive supports to the CPU Board.
   Discard these supports (Figure B-5 items F and G).
9. Fit the two new supports from the kit in the **rear two support holes only** (Figure B-5 item G).

Fitting the New Disk-Drive/Front Panel

1. Clip the HP-IB ribbon cable from the new Front Panel into it's socket on the CPU board.
2. Clip the new disk-drive ribbon cable into it's socket on the CPU board.
3. Align the CPU Board with the holes in the new front panel and secure using the original two screws.
4. Clip the RS232 ribbon cable from the new Front Panel into J2 socket on the CPU board.
5. Secure the new Disk Drive to the new rear disk-drive supports on the CPU Board using two of the original screws.
6. Replace the two nuts which secure the PARALLEL Interface Connector to the new Front Panel.

Fitting the CPU Module and Re-assembling the Instrument

1. Replace the CPU module back into the instrument.

VERY IMPORTANT NOTE

To prevent removal of, or damage to the metal RFI STRIP on the module next to the CPU, you MUST use special tool hp part number 03776-00016 or a thin LOW-STATIC plastic or fibre card (200mm x 135mm x 0.5mm) when inserting the CPU module back into the instrument. Place this card against the RFI Strip, then slide the CPU Module back into the instrument. Push the CPU Module fully home, then pull out the card - see Figure B-3.

CAUTION Severe damage can result if an RFI Strip is dislodged and falls inside the instrument. Always ensure that RFI strips are securely in position and unbroken.

2. Replace the outer cabinet sleeve, optical module shields and rear panel feet - this is a reversal of the removal procedure.

Testing

1. Switch on the instrument and check for a sensible display.
2. Carry out the procedure for downloading the new firmware described in Service Note 37717C-01. Ensure the new firmware upgrade has completed successfully.
3. Obtain a pass on all instrument Selftests.

The instrument is now ready for use.

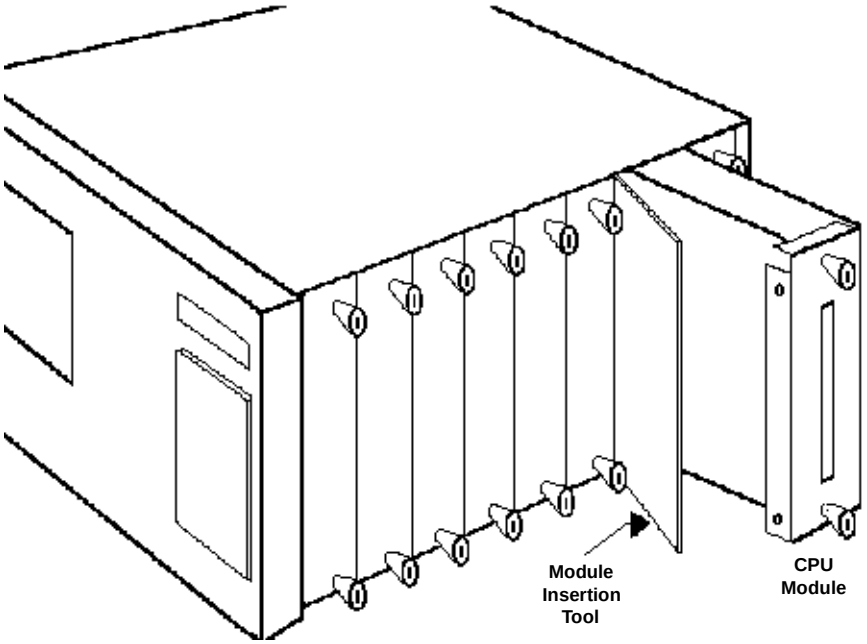


Figure B-3 Position of Processor Module and Insertion Tool

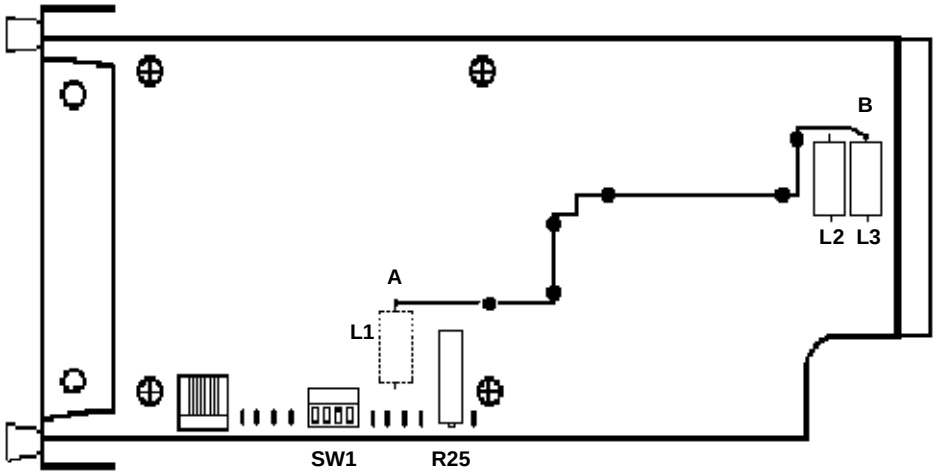


Figure B-4 Showing the Wire-Link modification to the Processor Board

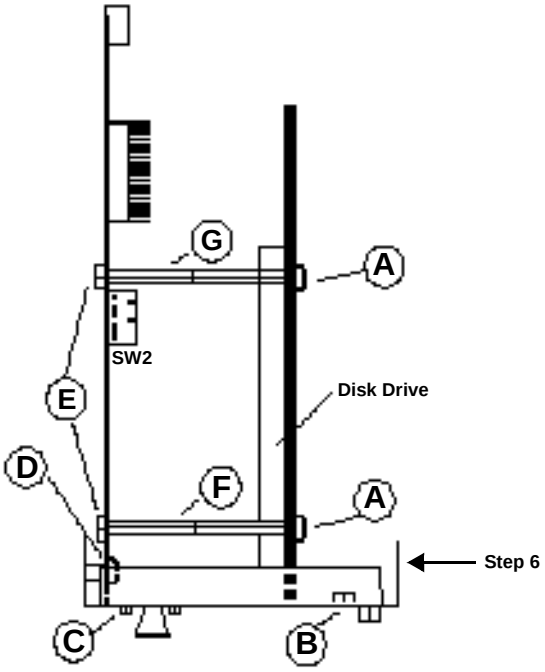


Figure B-5 Processor Module (viewed from top)

SERVICE NOTE 37717C-06

HP 37717C PDH/SDH/Jitter Test Set

Serial Numbers : N/A
Options : All
Build Status : All
Title : Premature Failure of NVM Battery
To be Performed by : Qualified Service Personnel
Date: April 1997

Parts Required

Description	HP Part Number	Quantity
Battery 3.6 Volts Lithium	**1420-0380**	**1**
Intergrated Circuit MAX695	**1820-8403**	**1**

Situation

The lithium battery fitted to the HP 37717C Processor Module is designed to last in excess of five years under all operating conditions specified for the instrument. If the NVM battery fails (i.e is fully discharged) within this period, then the NVM standby current should be checked at the same time as the battery is replaced. If the standby current is outwith specification, the NVM standby IC must be replaced.

ADMINISTRATIVE INFORMATION

Service Note Classification : INFORMATION ONLY

Solution/Action

If there is an "NVM Failure" message on the instrument display immediately after switch-on and the instrument has assumed DEFAULT SETTINGS (see Operating or Service Manual), then suspect NVM battery failure (i.e fully discharged). Use the following procedure to check the NVM battery voltage and standby current. If the standby current is excessive, U16 on the processor board should be replaced.

NOTE This IC is a 16 pin Surface Mount component. If facilities for replacement are unavailable, contact your local HP Service Center for assistance.

Procedure

Removing the Processor (CPU) Module

1. Switch off the HP 37717C **and DISCONNECT THE POWER CORD.**
2. Remove the rear panel feet.
3. If Optical Modules are fitted, unscrew the optical shield from the input and output connectors.
4. Withdraw the outer cabinet sleeve back and out of the instrument.
5. Remove the clamp screws on the top and bottom right-hand side of the chassis which secure the CPU Module (see Fig 1).
6. Withdraw the CPU module from the instrument.

Hint: If this module is difficult to remove, insert an 8mm (5/16AF) open-ended spanner under one of the module knobs and lever out against the knob on the adjacent module.

CAUTION Never use a screwdriver or other sharp implement to lever the module as circuit tracks may be cut or the module metalwork irrepairably damaged.

Checking the NVM Battery Current

1. With the processor module on the bench, connect a DVM between battery POSITIVE and NEGATIVE terminals.
2. If the measured voltage is less than 3.4Volts the battery should be replaced. (follow the procedure in the Service Manual when replacing this battery).
3. With a good battery fitted, connect the DVM between battery NEGATIVE terminal and TP13 (ground).
4. The measured voltage on the DVM should be less than 20mV.

NOTE This equates to a drain current of less than 20uA, as the measured voltage is across a 1000 ohm resistor in series with the battery.

5. If the measured voltage is greater than 20mV, replace U16 on the CPU board (this is a 16 pin surface-mount IC - see Table 1).
6. Repeat steps 1 to 4 and ensure the current is within specifications.

Fitting the CPU Module and Re-assembling the Instrument.

1. Replace the CPU module back into the instrument.

VERY IMPORTANT NOTE

To prevent removal of, or damage to the metal RFI STRIP on the module next to the CPU, you MUST use special tool hp part number 03776-00016 or a thin LOW-STATIC plastic or fibre card (200mm x 135mm x 0.5mm) when inserting the CPU module back into the instrument. Place this card against the RFI Strip, then slide the CPU Module back into the instrument. Push the CPU Module fully home, then pull out the card - see Figure B-6.

CAUTION Severe damage can result if an RFI Strip is dislodged and falls inside the instrument. Always ensure that RFI strips are securely in position and unbroken.

2. Replace the outer cabinet sleeve, optical module shields and rear panel feet - this is a reversal of the removal procedure.

Testing

1. Switch on the instrument and check for a sensible display.
2. Ensure there is no "NVM Failure" message on the instrument display immediately after switch-on and that the instrument has not assumed DEFAULT SETTINGS. (check this by changing any paramenter on the transmit or receive menu and ensuring the new setting is maintained after power has been cycled).
3. Obtain a pass on all instrument Selftests.

The instrument is now ready for use.

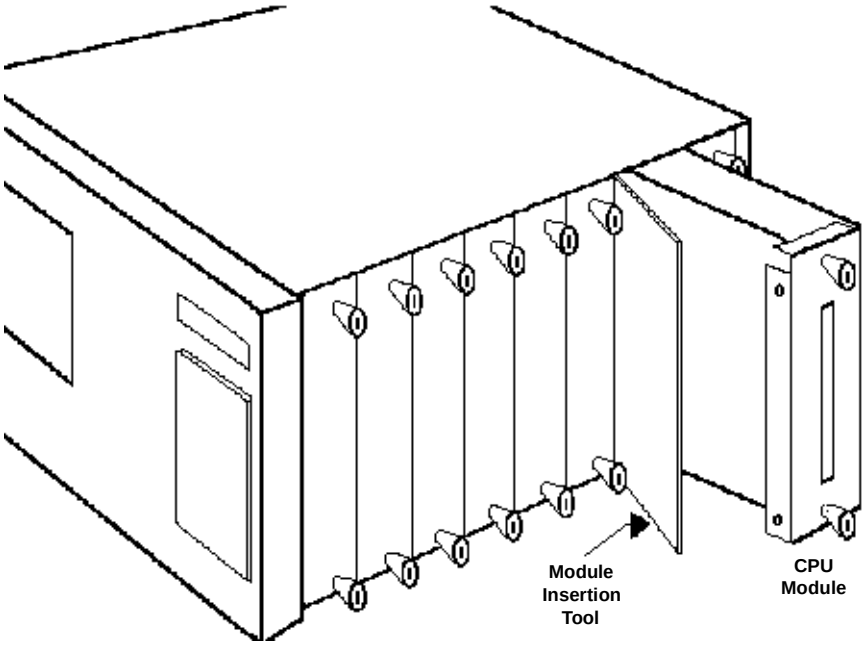


Figure B-6 Position of Processor Module and Insertion Tool

SERVICE NOTE 37717C-07

HP 37717C PDH/SDH/Jitter Test Set

Serial Numbers : GB00000000 to GB99999999
Build Status : 1.00 and above
Title : Replacing the Processor Assembly (CPU)
To be Performed by : Qualified Service Personnel
Date: August 1997

Parts Required

Description	HP Part Number	Quantity
Replacement Processor Kit	37717-60xxx	1

Situation

This Service Note gives information on parts and instructions required when changing to a new processor with greater memory on the HP 37717C

Action

When changing the processor order the appropriate part from the table above and use the following procedure to fit it.

NOTE If you are unsure what to order, or have problems fitting the above parts, please contact your HP representative or QTO Product Support on +44 131-331-7532.

ADMINISTRATIVE INFORMATION

Service Note Classification : INFORMATION ONLY

Use these instructions when replacing the CPU on a HP 37717C .
The instructions cover the following;

- Correct procedure for removing the old CPU Module from the instrument.
- Procedure for transferring the special Memory IC from the old CPU Assembly.
  This IC stores information on the option structure of the instrument and all soft calibration constants for the instrument. Transferring this IC means that it is not necessary to recalibrate the instrument or replace firmware options.
- Procedure for assembling the new CPU Board into the Module and replacing in the Instrument.
- Checking Options and Calibration Dates.
- Setting the Internal Clock Time and Date.
- Testing the instrument with the New CPU.
- Changing the MAC address Label (applies to option A3B units only).
  Every instrument shipped with Option A3B LAN interface has a unique MAC address associated with it. This address is stored in U15 on the CPU, so will be transferred over with U15 (see above). There is also a label fitted to the old CPU with this unique address which must also be transferred.

CAUTION These procedures should only be carried out by qualified Service Personnel .
Anti-static precautions must be observed at all times. - Use the anti-static wrist-strap provided in this kit if an anti-static work-area conforming to Corporate Standard 741.808 is unavailable.
Read the anti-static documentation at the end of this procedure.

Removing the old CPU Assembly.

Remove the old CPU Assembly as follows:

1. Switch off the instrument and disconnect the power cord and any interconnecting cables.
2. Place the instrument face down on the workbench.
3. Remove the 4 screws securing the rubber feet to the rear panel.
4. If Optical Modules are fitted, unscrew optical shield from the input and output connectors.
5. Withdraw the outer cabinet sleeve back and out of the instrument.
6. Remove the two clamp screws on the top and bottom right-hand side of the chassis which secure the CPU module.
7. Withdraw the CPU module from the instrument using the two knobs to help with removal.

Transferring the Memory IC from the old CPU Board Assembly

On the old CPU Module

1. Unscrew the posidrive screws which secure the Disk Drive with it's metal shield to the disk-drive supports on the CPU Board.
2. Unscrew the two nuts which secure the PARALLEL Interface Connector to the module Front Panel.
3. Unclip the HP-IB, RS-232 and Disk-Drive ribbon cables from their sockets on the CPU board Assembly.
4. Using a long posidrive screwdriver, unscrew the two screws which secure the module Front Panel to the CPU Board.
5. Remove the module Front Panel together with the disk-drive assembly and metal shield and place to one side in an anti-static bag.
6. Locate U15 (marked on the topside of the board) and carefully remove this IC from it's socket using a Quilext 1 Universal IC Extraction tool or equivalent.

On the new CPU Module

1. Fit U15 from the old CPU into the socket on the new CPU assembly taking great care not to touch any pins on the IC or socket. Ensure correct alignment before pushing firmly home in the socket.

NOTE You MUST discard any IC in the new module fitted into U15 position and replace with the part from the old module. This memory IC contains option and calibration data UNIQUE to your instrument.

NOTE You may need to repeat steps 1 to 6 above to access this IC on the new CPU.

Once this IC has been fitted, check the switches on the new CPU Assembly are set as follows:

Assembly Description	Switch Number	Finger Number	Position
A4 Processor Assembly	SW1	1,2 & 4	Closed
A4 Processor Assembly	SW1	3	Open
A4 Processor Assembly	SW2	1,3,4,6,7,8	Closed
A4 Processor Assembly	SW2	2 & 5	Open

Transferring the LAN Interface MAC Address Label (Option A3B only)

1. Check the instrument rear panel to see if option A3B (LAN Interface) is fitted. If it is, there will be a MAC ADDRESS label stuck to the rear of the old CPU board. Write down the number on this label (this will be keyed into the CPU memory later), then remove the label and attach it to the new CPU board in the same position.

Fitting the CPU Module and Re-assembling the Instrument.

1. Replace the CPU module back into the instrument.

VERY IMPORTANT NOTE

To prevent removal of, or damage to the metal RFI STRIP on the module next to the CPU, you MUST use special tool hp part number 03776-00016 or a thin LOW-STATIC plastic or fibre card (200mm x 135mm x 0.5mm) when inserting the CPU module back into the instrument. Place this card against the RFI Strip, then slide the CPU Module back into the instrument. Push the CPU Module fully home, then pull out the card - see Figure B-7.

CAUTION Severe damage can result if an RFI Strip is dislodged and falls inside the instrument. Always ensure that RFI strips are securely in position and unbroken.

2. Replace the outer cabinet sleeve, optical module shields and rear panel feet - this is a reversal of the removal procedure.

Downloading New firmware (Option UKZ or USK only)

The new processor has already be loaded with the current revision of firmware. This is applicable to all options **EXCEPT options USK or UKZ**. If either (or both) of these options is fitted to your instrument, you will need to download the new firmware using the disks supplied in this kit Use the procedure described in Service Note 37717C-01 to do this.

Checking Options and Calibration Dates.

1. Switch on the instrument and check for a valid power-up routine.
2. Press the OTHER key, then [MORE] softkey until [OPTIONS] softkey is displayed.
3. Press the [OPTIONS] softkey and select each option type in turn (i.e PDH, SDH, JITTER, ATM etc).
4. Ensure that the options shown as FITTED on the display agree with the options listed on the instrument rear panel.
5. Press the [MORE] softkey until [CALIBRATION] softkey appears at the bottom of the display.
6. Enter the Calibration password [1243].
7. Select each Calibration Item and ensure the calibration dates are valid.

NOTE An annual Calibration cycle is recommended for the HP 37717C

Setting the Internal Clock Date and Time

You will need to set the internal clock to the correct time and date as this will be incorrect after changing the CPU.

1. Switch on the instrument.
2. Press OTHER key, then [MORE] softkey until [TIME & DATE] softkey is displayed.
3. Press [TIME & DATE] softkey then move the cursor to CLOCK MODE.
4. Select [SETUP] then move the cursor to TIME. Set the clock to the correct time using [<],[>], and [INCREASE DIGIT], [DECREASE DIGIT] softkeys.
5. Move the cursor to DATE. Set the clock to the correct date using [<],[>], and [INCREASE DIGIT], [DECREASE DIGIT] softkeys.
6. Return the cursor to CLOCK MODE and press [RUN].

The internal clock is now set.

Checking the LAN Interface MAC Address (Option A3B only)

Check the MAC address in memory after ensuring option A3B is enabled (see above) by carrying out the following procedure:

1. Switch on the instrument and press the OTHER key then [MORE] softkey. Select the [CALIBRATION] function.
2. Select CALIBRATE PASSWORD and set to [1243] using the INCREASE DIGIT and DECREASE DIGIT softkeys.
3. Select the calibration item [SET MAC ADDRESS].

The MAC Address is displayed at the bottom of this page. If it is different to that on the label which you transferred from the old CPU, then you will need to change it as follows:

4. Move the cursor to the [MAC ADDRESS EDIT] field and change the address to that shown above using the INCREASE DIGIT and DECREASE DIGIT softkeys.
5. Move the cursor to the [ACCEPT CHANGES] field and press the ON softkey.
6. Ensure the change is reflected at the bottom of the display.

Testing

Perform all the instrument selftests.

NOTE It is very important to cable the instrument correctly when running the selftests. Cabling depends on options fitted - see Calibation or Service Manual for this information.

When a pass has been obtained on all selftests the instrument is ready for use.

Important Operational Note

If the new CPU is pre-loaded with firmware version A.01.62 AND .....
Your instrument contains options A1M,A1N,A1P (or the equivalent options with small siemens connectors), you will find the Jitter receive menu contains a selectable HP2 filter on SDH rates. This filter should always be set OFF in the menu as the filter hardware is NOT fitted.
This inappropriate selection is due to a firmware bug in version A.01.62 ONLY.

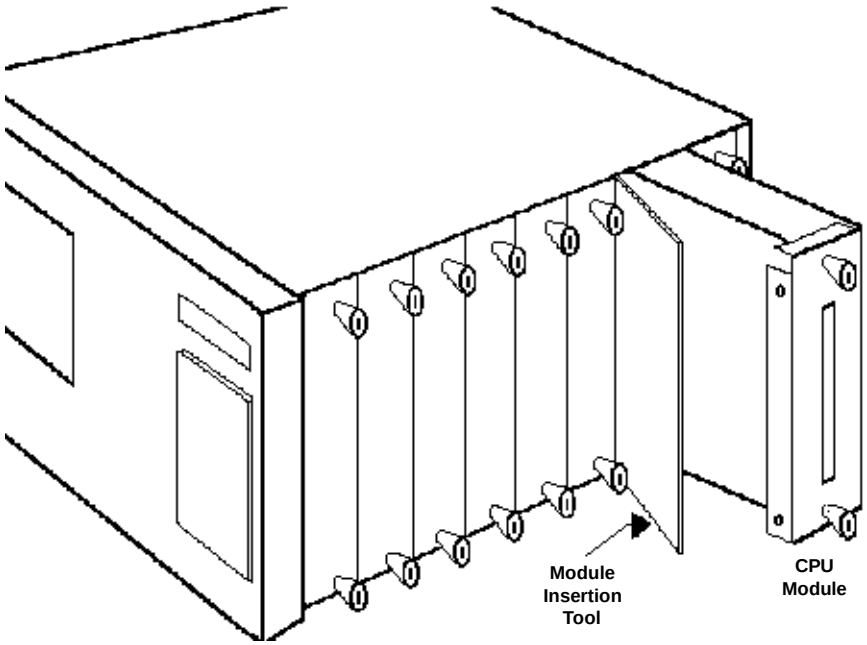


Figure B-7 Position of Processor Module and Insertion Tool

SERVICE NOTE 37717C-08

HP 37717C PDH/SDH/Jitter Test Set

Serial Numbers : Below GB00000825 (nominal) and if Firmware Revision fitted is A.01.49 or A.01.62
Title : Display Blank and/or Instrument Hung
To be Performed by : Qualified Service Personnel
Date: December 1997

Parts Required

Contact Division Product Support, quoting model number, serial number, options fitted and current firmware revision

Situation

A firmware bug exists in firmware revisions A.01.49 and A.01.62 (main) which can cause a blank display and/or the instrument to be hung-up. This can occur if the instrument is power cycled when it has 1sec resolution gating , the SMG is enabled and the instrument is switched off for a long time.

Solution/Action

If any of the above symptoms are shown by the instrument, the short term solution to get the instrument back into working order is to leave the instrument powered on for at least 24 hours. If the instrument remains in the hung-up state, please contact Division Product Support for further instructions.

A **free** firmware upgrade is available but the branch of firmware is dependant on a number of factors, contact Division Product Support with model number, serial number, options fitted, and current firmware revision.

If there are more instruments of the same age and revision every effort should be made to upgrade these instruments as well.

ADMINISTRATIVE INFORMATION

Service Note Classification : MODIFICATION RECOMMENDED

SERVICE NOTE 37717C-09

HP 37717C PDH/SDH/Jitter Test Set

Serial Numbers : N/A
Build Status : Below 2. 96
Title : Fix to the Processor chip
To be Performed by : Qualified Service Personnel
Date: March 1998

Parts Required
Double sided tape 0460-2159

Situation

If the CPU assembly, A3D or A3B, is subjected to mechanical shock, this can cause the processor chip to jump out of its socket.

Solution/Action

1. Remove CPU from 37717C
2. Cut two strips of double sided tape approx 40mm long
3. Press the tape to both faces of the processor chip and socket (see Figure B-8)
4. Remove protective paper from both sides of the tape.

ADMINISTRATIVE INFORMATION

Service Note Classification : MODIFICATION RECOMMENDED

PROCESSOR MODULE A3B
PROCESSOR MODULE A3D

PARTS LIST A3B	HP PART No	QTY	ITEM
PANEL PROCESSOR MODULE	37714-00031	1	1
A3B PROC + LAN PCA	37714-60054	1	2
STUD 4-40 UNCH3.5	0380-2072	2	3
STDFHX M3 X 45 M/F	0380-4629	2	4
SCREW M/C M3 x 8MM	0515-0897	2	5
FLAT WASHER	3050-0891	4	6
WASHER LK M3	2190-0584	2	7
NUT M3	0535-0025	2	8
SCREW M/C M3 x 6MM	0515-0886	2	9
PROM ASSEMBLY	37714-80032	1	10
CONT PROM ASSEMBLY	37714-80028	1	11
CABLE RIBBON	37714-60058	1	13
CABLE RIBBON	37717-60017	1	14
CABLE RIBBON	37717-60002	1	15
LABEL LICENSE	5002-1117	1	16
DISIDED TAPE 40mm L15	0460-2159	2	16

PARTS LIST A3D	HP PART No	QTY	ITEM
SAME AS ABOVE EXCEPT			
A3D PROC + LAN PCA	37714-60028	1	2

OPERATION SEQUENCE

1. PLACE DISIDED TAPE (ITEM 16) ON TOP AND BOTTOM FACES. PRESS DOWN FIRMLY ON THE TAPE FOR BETTER ADHESION.
2. FIT PROM ASSEMBLY (ITEM 10) TO POSITION U15 ON P.C. BOARD (ITEM 2).
3. FIT PROM ASSEMBLY (ITEM 11) TO POSITION U43 ON P.C. BOARD (ITEM 2).
4. FIT STANDOFF (ITEM 4) TO P.C. BOARD (ITEM 2) USING 2 FLAT WASHERS (ITEM 6), 2 LOCK WASHERS (ITEM 7) AND 2 NUTS (ITEM 8).
5. FIT RIBBON CABLE END (ITEM 12) TO POSITION J2 ON P.C. BOARD.
6. FIT RIBBON CABLE END (ITEM 13) TO POSITION J5 ON P.C. BOARD.
7. FIT RIBBON CABLE END (ITEM 14) TO POSITION J7 ON P.C. BOARD.
8. PLACE P.C. BOARD ASSEMBLY (ITEM 2) IN PLACE AND SECURE USING STUD (ITEM 3).
9. FIT SCREW (ITEM 9) AND WASHER (ITEM 6) THROUGH DISC DRIVE ASSEMBLY AND TIGHTEN STANDOFF (ITEM 4) ON P.C. BOARD.
10. FIT SCREW (ITEM 9) THROUGH P.C. BOARD AND TIGHTEN INTO PANEL ASSEMBLY (ITEM 1).
11. FIT LABEL (ITEM 15) ONTO CIRCUIT SIDE OF P.C. BOARD (ITEM 2).

NOTES

1. TORQUE ITEM 3 TO 3lb-ins.
2. TORQUE ITEMS 5, 8 AND 9 TO 6lb-ins.

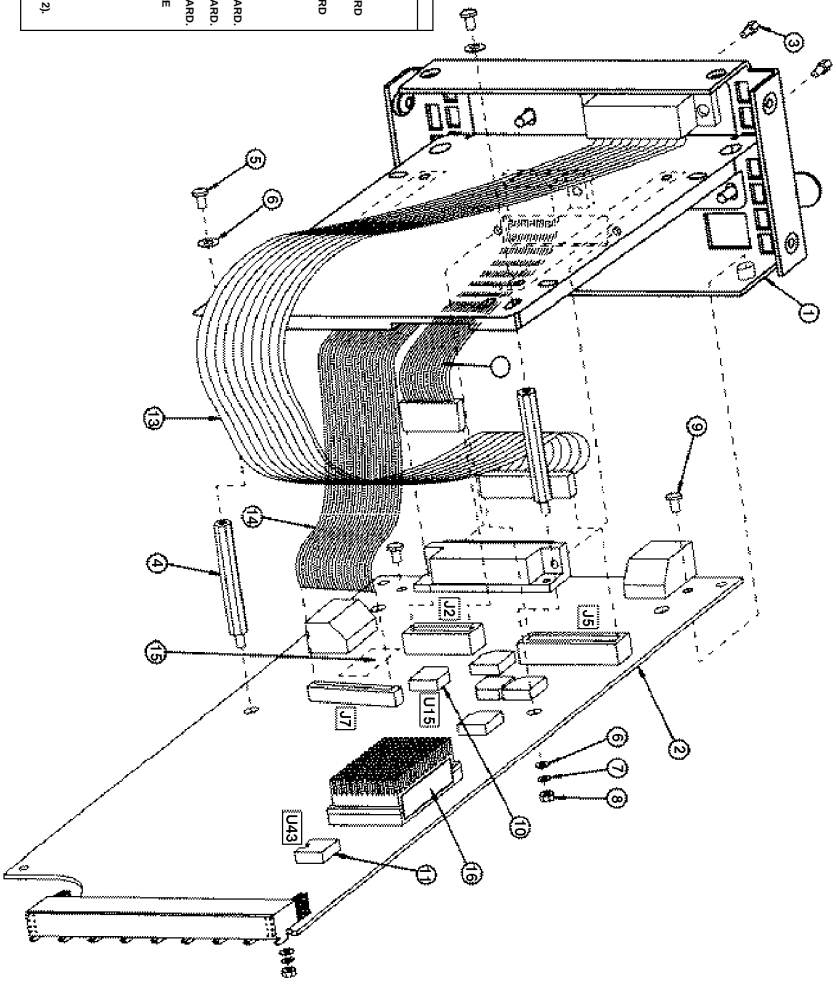


Figure B-8

SERVICE NOTE 37717C-10

HP 37717C PDH/SDH/ATM Test Set

Serial Numbers : GB00000100 to GB00009999
Build Status : n/a
Title : Cleaning Optical Surfaces
To be Performed by : Qualified Service Personnel
Date: March 98

Parts Required

ITEM	HP Part Number
Isopropyl alcohol	**8500-5344**
Cotton swabs	**8520-0023**
Small foam swabs	**9300-1223**
Compressed dust remover (non-residue)	**8500-5262**

Action

If the following procedures are followed this could save expensive repairs on lightwave equipment, and it will reduce downtime and loss of productivity caused by the repairs.

ADMINISTRATIVE INFORMATION

Service Note Classification : INFORMATION ONLY

CLEANING

Two cleaning processes are provided. The first process describes how to clean non-lensed lightwave connectors. The second process describes how to clean lightwave adapters.

CAUTION These cleaning processes apply only when dry connections are used (no index matching compounds). Hewlett-Packard strongly recommends against the use of index matching compounds, particularly gels, as they may be difficult to remove and can contain damaging particulates. If an index matching compound is used, contact the compound manufacturer for specific information about recommended solvents and cleaning procedures.

Cleaning Non-Lensed Lightwave Connectors

Equipment. The following is a list of the items that should be used to clean non-lensed lightwave connectors.

ITEM	HP Part Number
Isopropyl alcohol	**8500-5344**
Cotton swabs	**8520-0023**
Compressed air	**8500-5262**

CAUTION Hewlett-Packard recommends that you do not use any type of foam swab to clean optical fiber ends. Foam swabs can leave filmy deposits on fiber ends that can degrade performance.

Process. Before cleaning the fiber end, clean the ferrules and other parts of the connector. Use isopropyl alcohol, clean cotton swabs, and clean compressed air. Then use alcohol to clean the fiber end. Some amount of wiping or mild scrubbing of the fiber end can help remove particles when application of alcohol alone will not remove them. This can be done by applying the alcohol to a cotton swab and moving it back and forth across the fiber end several times. This technique can help remove or displace particles smaller than one micron.
Allow the connector to dry (about 1 min) or dry it immediately with clean compressed air. Compressed air lessens the chance of deposits remaining on the fiber end after the alcohol evaporates. It should be blown horizontally across the fiber end. Visually inspect the fiber end for stray cotton fibers. As soon as the connector is dry, the connection should be made.

CAUTION Inverting the compressed air cannister while spraying will produce residue on the sprayed surface. Refer to instructions provided on the compressed air cannister.

Cleaning Lightwave Adapters

Equipment. All of the items listed above for cleaning connectors may be used to clean lightwave adapters. In addition, small foam swabs (HP part number 9300-1270) may be used along with isopropyl alcohol and compressed air to clean the inside of lightwave connector adapters.

NOTE As noted in a previous caution statement, the foam swabs can leave filmy deposits. These deposits are very thin however, and the risk of other contamination build upon the inside of adapters greatly outweighs the risk of contamination of foam swab deposits left from cleaning the inside of adapters.

Process. Clean the adapter by applying isopropyl alcohol to the inside of the connector with a foam swab. Allow the adapter to air dry, or dry it immediately with clean compressed air.

Cleaning Lensed Connections

Some instruments may have a connector that is "lensed." In other words: the connection does not provide a physically contacting connection, but the light is received into a lens rather than into a connecting fiber. These receiving lenses usually have an anti-reflective coating that is very easily damaged. Therefore, these connectors should *never* have cleaning solutions or any other substance applied to them unless it is specifically recommended by the manufacturer. You may wish to use clean compressed air to rid them of dust from time to time.

SERVICE NOTE 37717C-11

HP 37717C PDH/SDH/ATM Test Set

Serial Numbers : GB00000100 to GB00009999
Build Status : n/a
Title : Handling Lightwave Connectors
To be Performed by : Qualified Service Personnel
Date: March 98

Parts Required

Item	HP Part No.	Connector Option
Laser shutter cap	**08145-64521**	**All options**
FC/PC dust cap	**08154-44102**	**opt 012**
Biconic dust cap	**08154-44105**	**opt 015**
DIN dust cap	**5040-9364**	**opt 013**
HMS10/HP dust cap	**5040-9361**	**opt 011**
ST dust cap	**5040-9366**	**opt 014**

Action

Proper cleaning and handling of lightwave connectors is imperative for achieving accurate and repeatable measurements with your Hewlett-Packard lightwave equipment. Lightwave interfaces should be cleaned before each measurement using the techniques described in service note 37717C-10. Information on protecting and storing your connectors/cables and tips on how to properly mate connectors are included in this service note.

ADMINISTRATIVE INFORMATION

Service Note Classification : INFORMATION ONLY

HANDLING

Always handle lightwave connectors and cable ends with great care. Fiber ends should never be allowed to touch anything except other mating surfaces or cleaning solutions and tools.

CAUTION Hewlett-Packard strongly recommends that index matching compounds NOT be applied to their instruments and accessories. Some compounds, such as gels, may be difficult to remove and can contain damaging particulates. If you think the use of such compounds is necessary, refer to the compound manufacturer for information on application and cleaning procedures.

STORAGE

All of Hewlett-Packard's lightwave instruments are shipped with either laser shutter caps or dust caps on the lightwave adapters that come with the instrument. Also, all of the cables that are shipped have covers to protect the cable ends from damage or contamination. These dust caps and protective covers should be kept on the equipment at all times except when in use.

The adapters that were shipped on your instrument can be removed from the connectors on the instrument. **If** you remove these adapters you should keep the exposed connector of your instrument covered until the next use. Protective covers for these exposed connectors are not

provided with the instruments, so it is best to keep the adapters on the instrument with the dust covers on.

MAKING CONNECTIONS

When you insert the ferrule into a connector or adapter, make sure that the fiber end does not touch the outside of the mating connector or adapter. In this way, you will not rub the fiber end against any undesirable surface. Many connectors have a keyed slot provided for optimum measurement repeatability that also helps to align and seat the two connectors. After the ferrule is properly seated inside the other connector, use one hand to keep it straight, rotate it to align the key, and tighten it with the other hand.

Most connectors using springs to push fiber ends together exert one to two pounds of force. Over-tightening or under-tightening these connectors can result in misalignment and non-repeatable measurements. Always finger tighten the connector in a consistent manner. Refer to the manufacturer's data sheet for any torque recommendations.

SUMMARY

When making measurements with lightwave instruments or accessories, the following precautions will help to insure good, reliable, repeatable measurements:

- Use extreme care in handling all lightwave cables and connectors.
- Be sure the connector interfaces are clean before making any connections.
- Use the cleaning methods described in the service note 37717C-10.
- Keep connectors and cable ends covered when not in use.

SERVICE NOTE 37717C-12

HP 37717C PDH/SDH/Jitter Test Set

Serial Numbers :GB00000000 to GB99999999
Build Status : 1.00 and above
Title : Self Test Fail 1052
To be Performed by : Qualified Service Personnel
Date: January 99

Parts Required None

Situation

Fail 1052 can occur during self test, if the Remote Control port is set to RS-232 and not HP-IB

Action

Before running self tests ensure that the Remote Control Port is set to HP-IB.

ADMINISTRATIVE INFORMATION

Service Note Classification : INFORMATION ONLY

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Hewlett-Packard Sales and Service Offices

If you need technical assistance with a Hewlett-Packard test and measurement product or application please contact the Hewlett-Packard office or distributor in your country.

Asia Pacific:

Hong Kong:

Tel: (852) 2599 7889

India:

Tel: (91-11) 682-6000

Japan:

Hewlett-Packard Japan Ltd.

Measurement Assistance Center

9-1, Takakura-Cho, Hachioji-Shi,

Tokyo 192, Japan

Tel: (81) 426-56-7832/Fax: (81) 426-56-7840

Korea:

Tel: (82-2) 769 0800

Malaysia:

Tel: (60-3) 291 0213

Philippines:

Tel: (63-2) 894 1451

People's Republic of China:

Tel: (86-10) 6505 0149

Singapore:

Tel: (1800) 292 8100

Taiwan:

Tel: (886-3) 492 9666

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Blackburn, Victoria 3130

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Tel: (90) 88 721

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Tel: (0)1 69.82.60.60

Germany:

Tel: (0180) 532 62-33

Greece:

Tel: (1) 7264045

Hungary:

Tel: (1) 252 4705

Ireland:

Tel: (01) 284 4633

Israel:

Tel: (03) 5380 333

Italy:

Tel: 02 - 92 122 241

Netherlands:

Tel: (020) 547 6669

Norway:

Tel: (22) 73 57 50

Poland:

Tel: (22) 608 7700

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